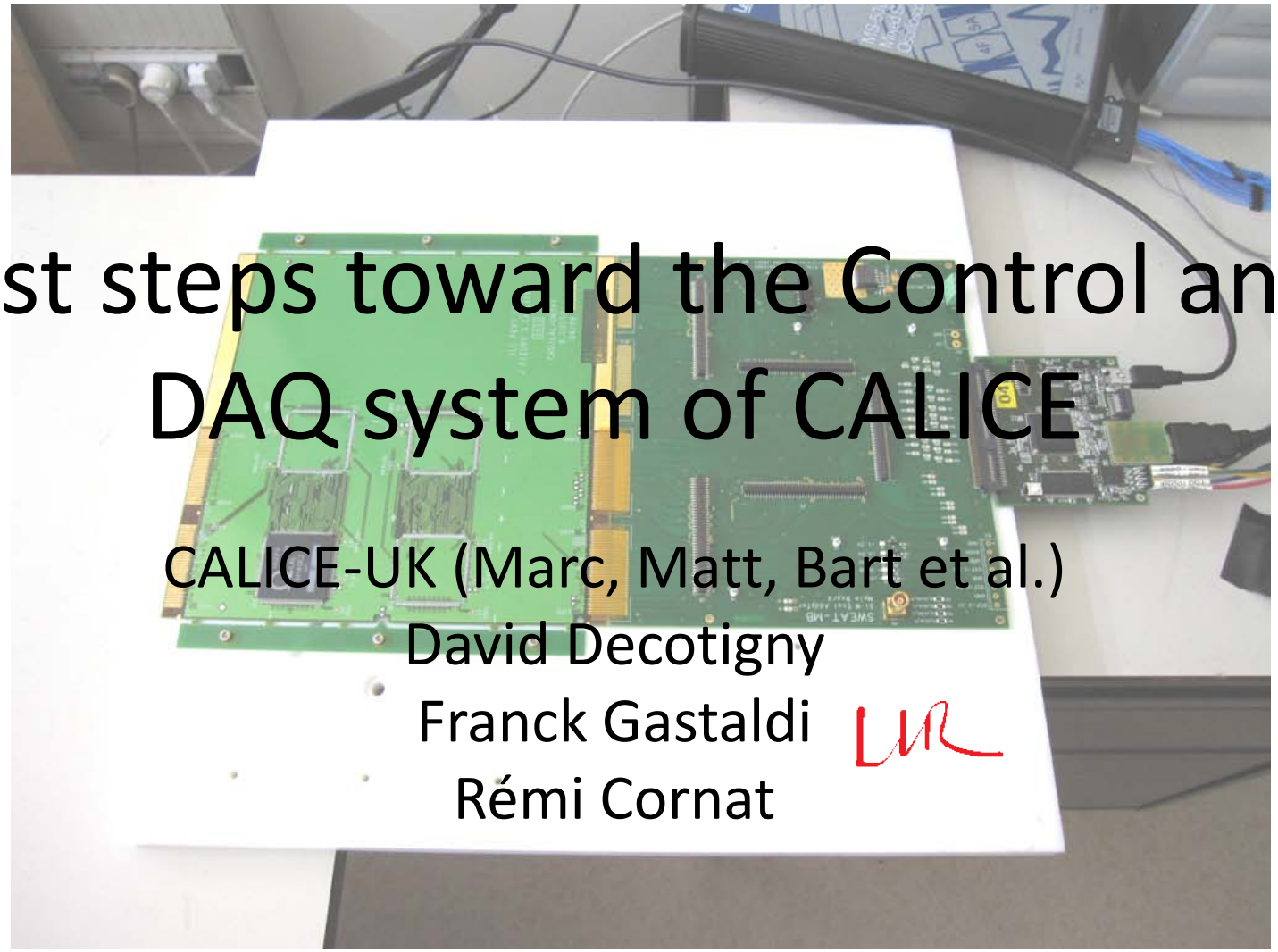


First steps toward the Control and DAQ system of CALICE

CALICE-UK (Marc, Matt, Bart et al.)
David Decotigny
Franck Gastaldi
Rémi Cornat

Previously announced (ecal) DIF development

- March'10 : DIF working with a DCC board
  - Serial link tested and validated
  - Part of specifications of the hdmi side implemented
  - USB I/O of the DCC
- June'10 : DIF working with a DCC + LDA
  - (almost) full specifications implemented
  - Including ROC chips functions (from Guillaume/Mathias)
  - Ethernet I/O of the LDA
  - SW for debug & Test
- September'10 : more than 1 DIF working with a DCC + LDA
  - Synchronization with "final" DAQ SW
- Later on : to be discussed

---- Done ----

And even with a LDA !

---- In good progress ----

Update
OK this afternoon

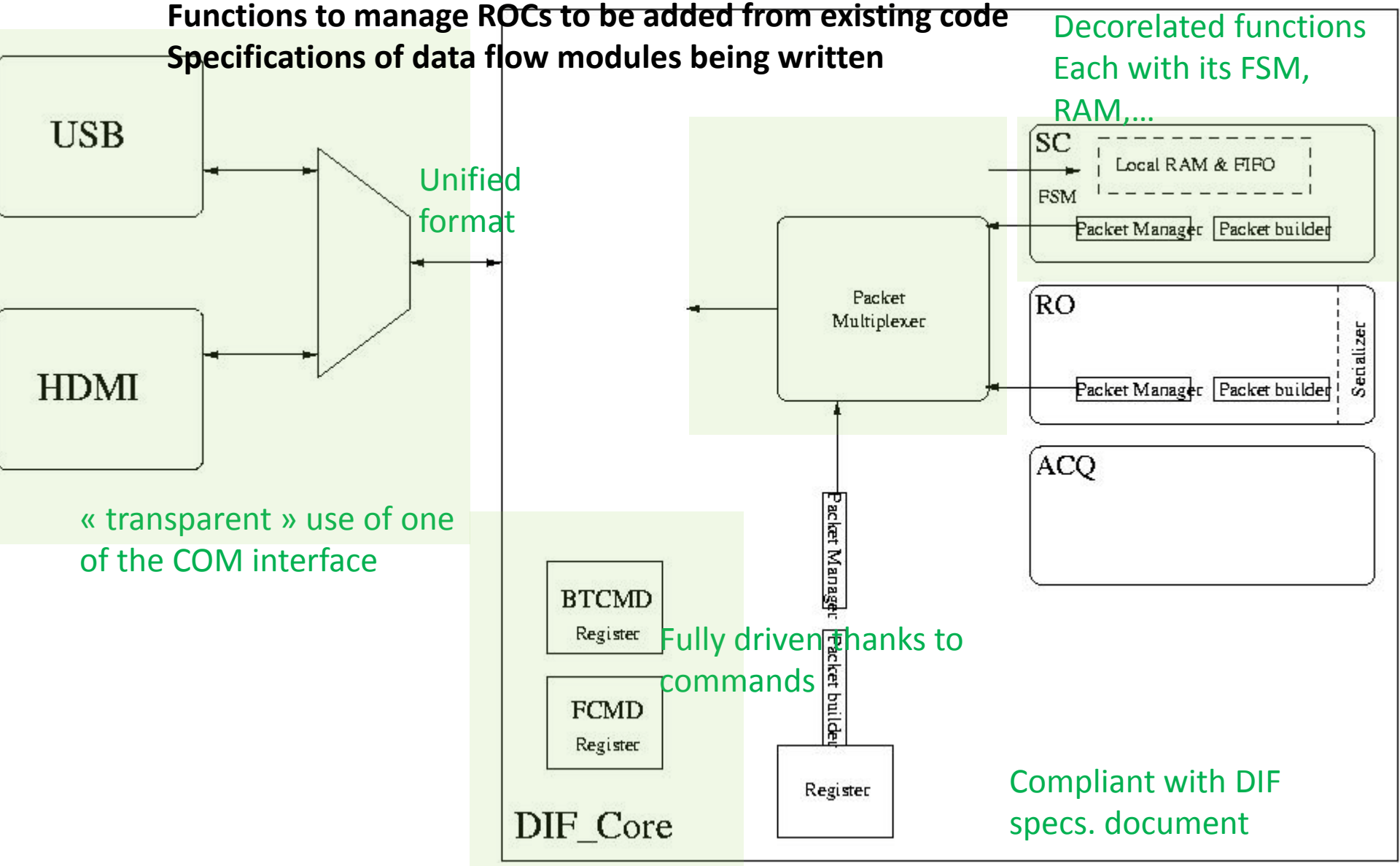
---- Done ----

Not before

Our planning remains unchanged

DIF : basic version

Functions to manage ROCs to be added from existing code
Specifications of data flow modules being written

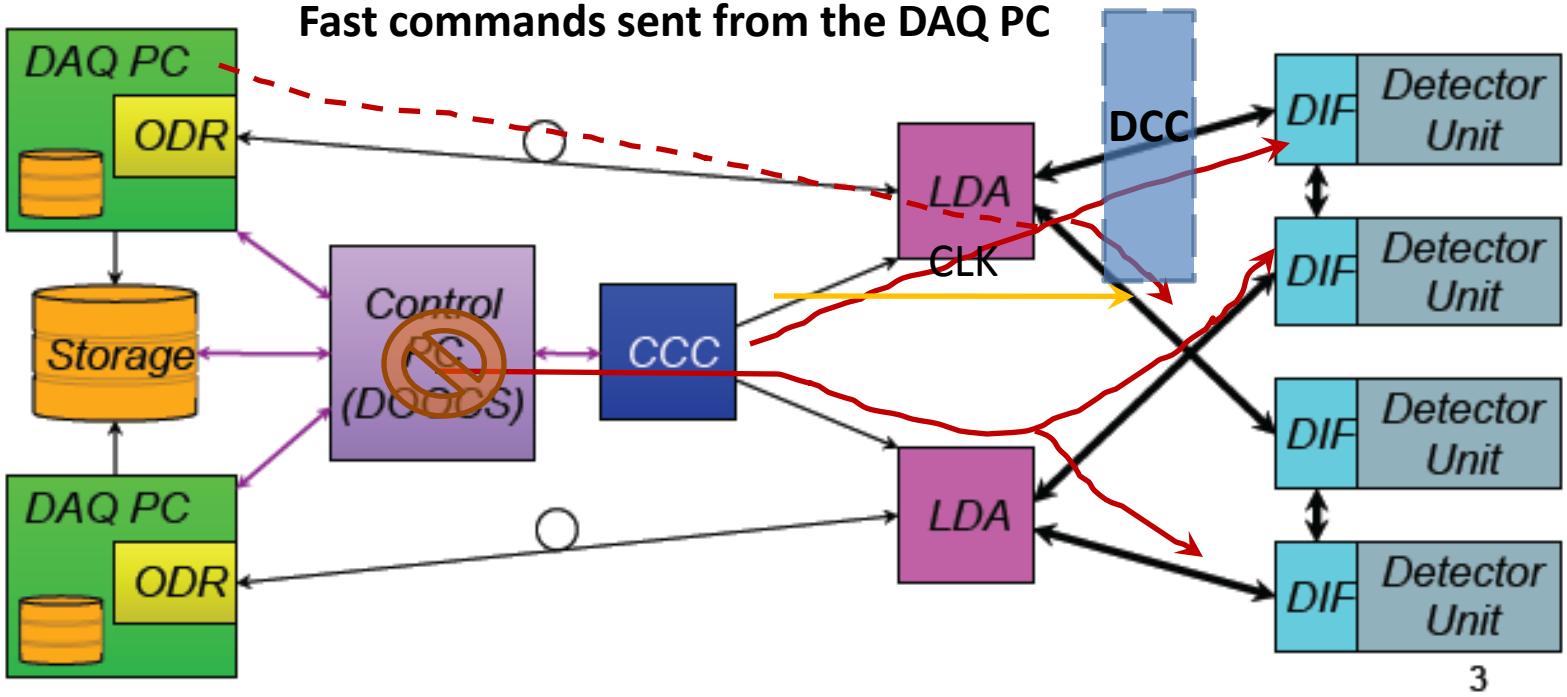


TFC

- Clock distribution (+ ext trig, + ram full)

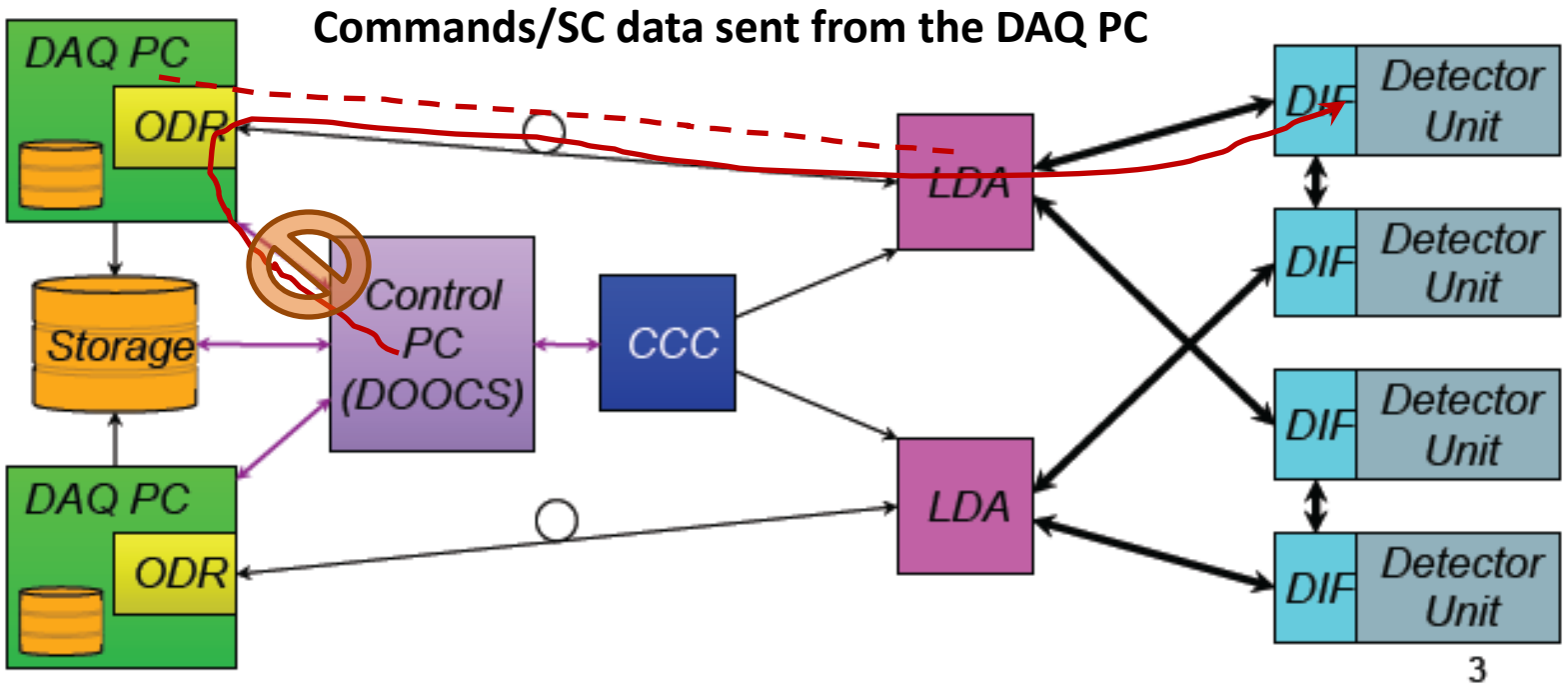
Clock at 50 MHz

- Machine interface (trains, BX)
- Fast Commands (isochronous) : reset, arm chips



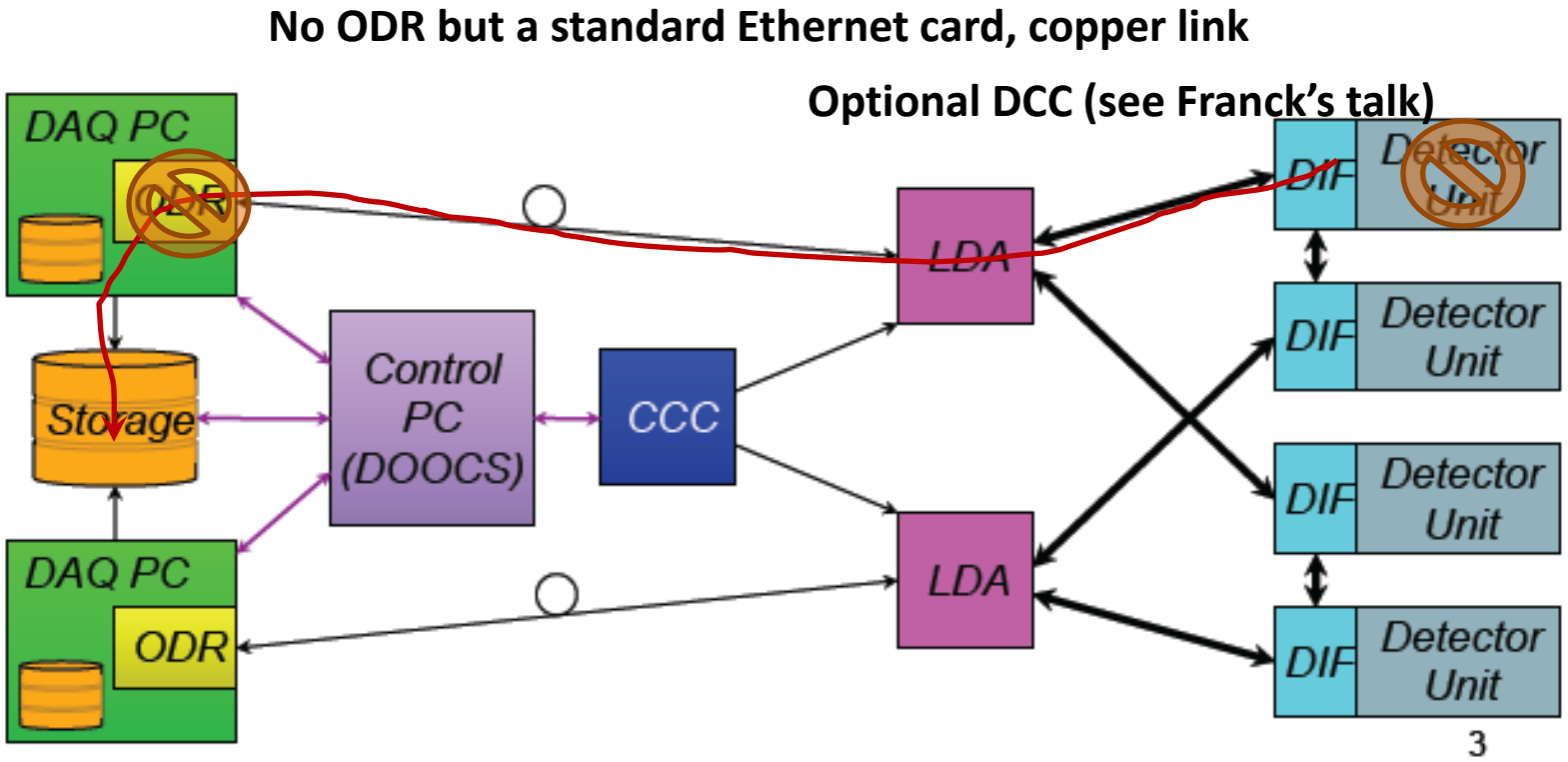
Slow Control / Commands

- Detector (DIF & VFE) configuration
- Simple orders (not timmed, broadcast possible)

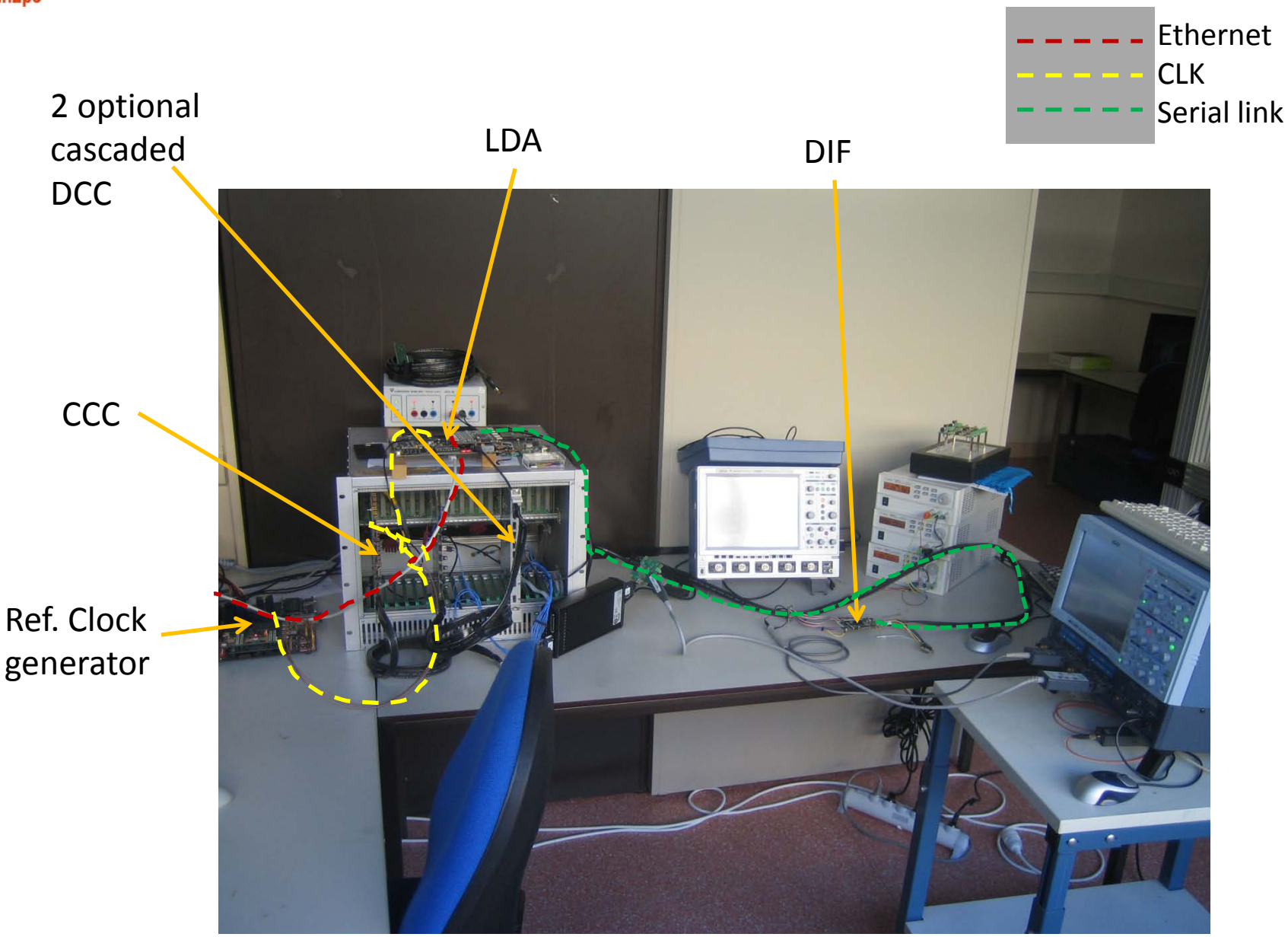


DAQ

- (Detector) Read Out emulated at DIF level
- Command triggered

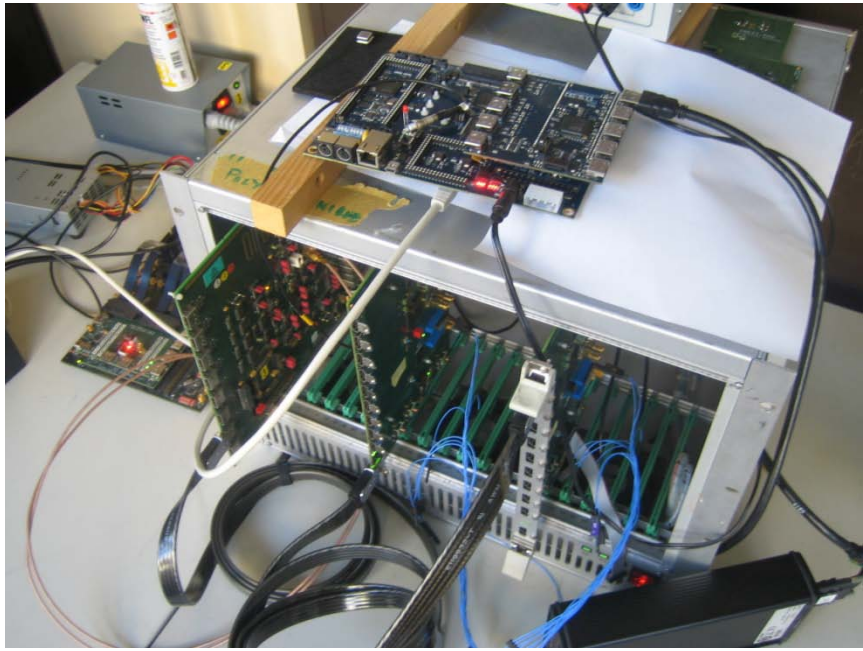


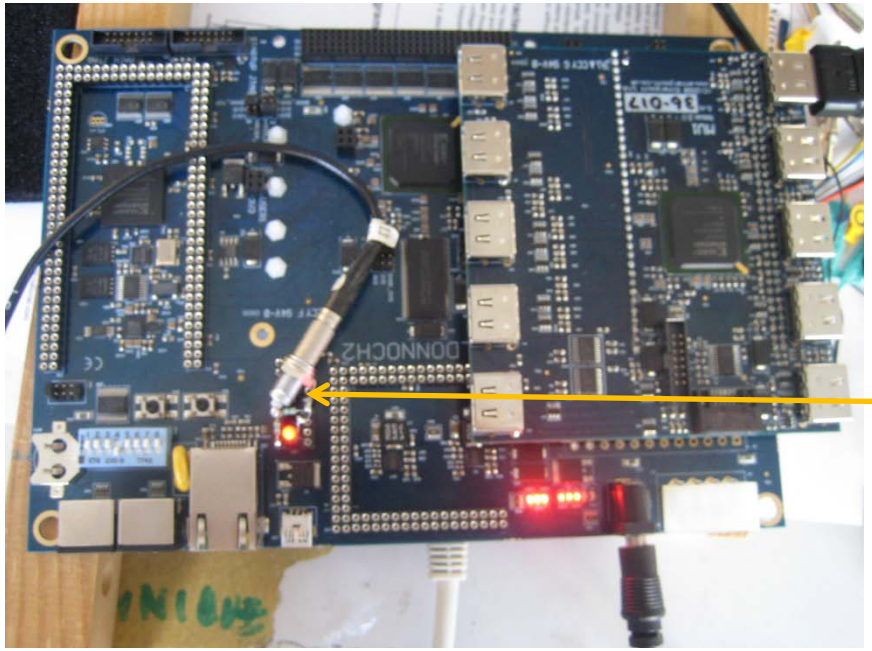
Test setup at LLR



Test setup at LLR (cont.)

Tested data paths:
PC(Ethernet) – LDA – DIF : 1x serial link
PC(USB) – DCC – DIF : 1x serial link
PC(USB) – DCC – DCC –DIF : 2x serial link
PC(Ethernet) – LDA – DCC – DIF : 2x serial link





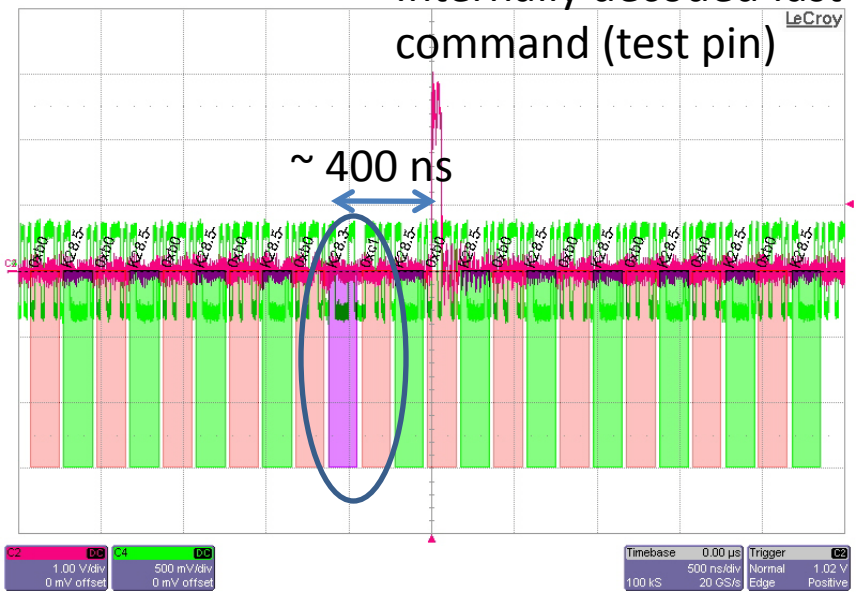
Clock from CCC replacing the local oscillator (TTL adapt.)

Fast commands

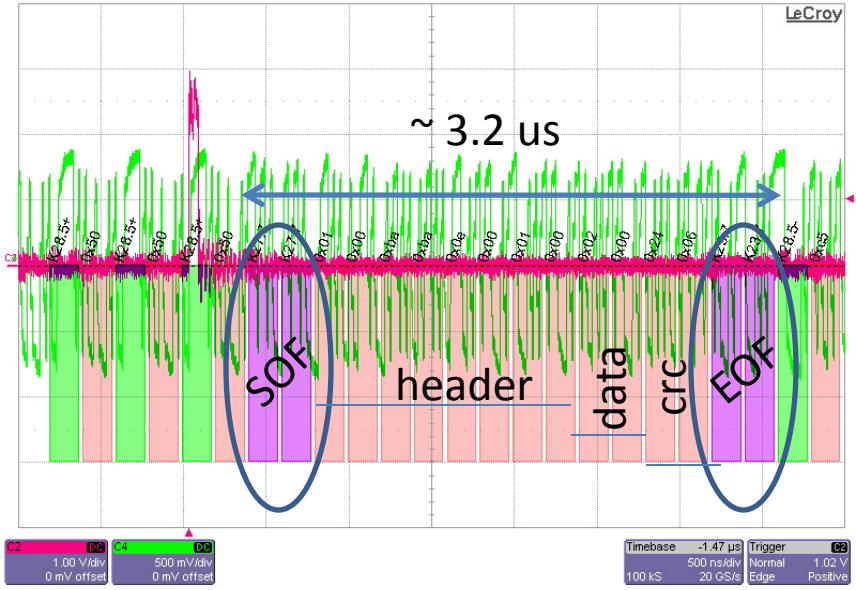
Sent from the DAQ/Control PC as a special ethernet frame triggering the fast command generator of the LDA

DIF input:
Special K character + 8b data

Internally decoded fast command (test pin)



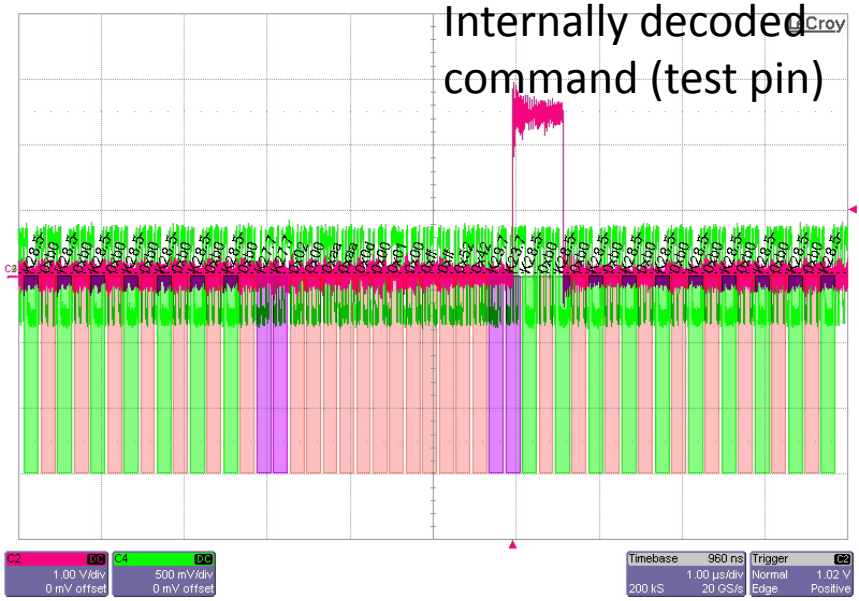
DIF output:
Standard packet as an echo
(arbitrary behavior for test&debug)



Commands

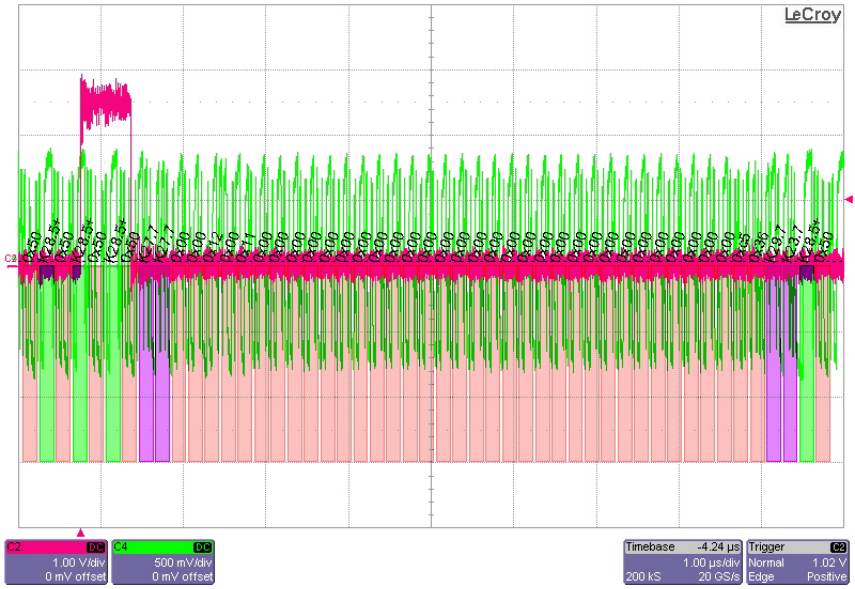
Sent from the DAQ/Control PC
as a normal ethernet frame
passed to the DIF by the LDA

Internally decoded
command (test pin)



DIF input:
Standard packet

DIF output:
Standard packet due to the execution of
the command
(here: read out of 13x16b status
registers)

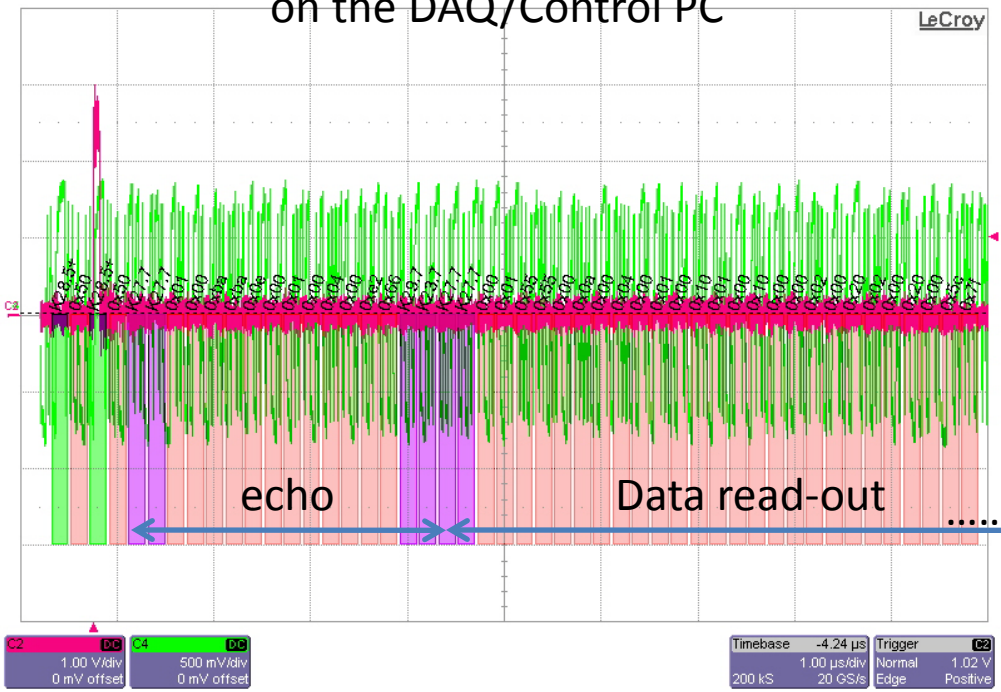


DAQ

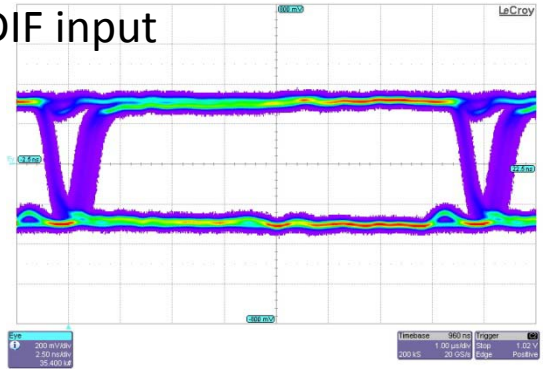
Sent from the DIF as serial link packets converted by the LDA as ethernet frames received on the DAQ/Control PC

DIF output:
here: read out of a fifo emulating physics data, triggered by a fast command
2 Standard packets due to the execution of the command: the echo of the fast command and the encapsulated physics data

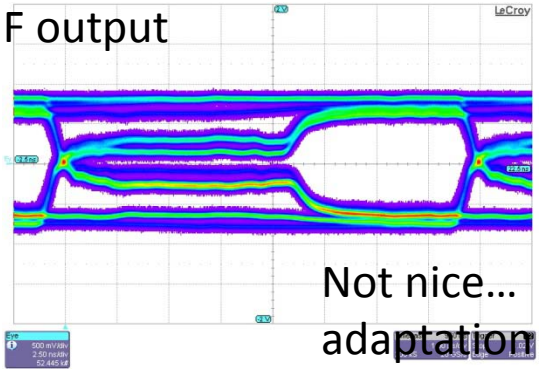
Data integrity has not been checked yet, problems expected



DIF input



DIF output



Not nice…
adaptation ?

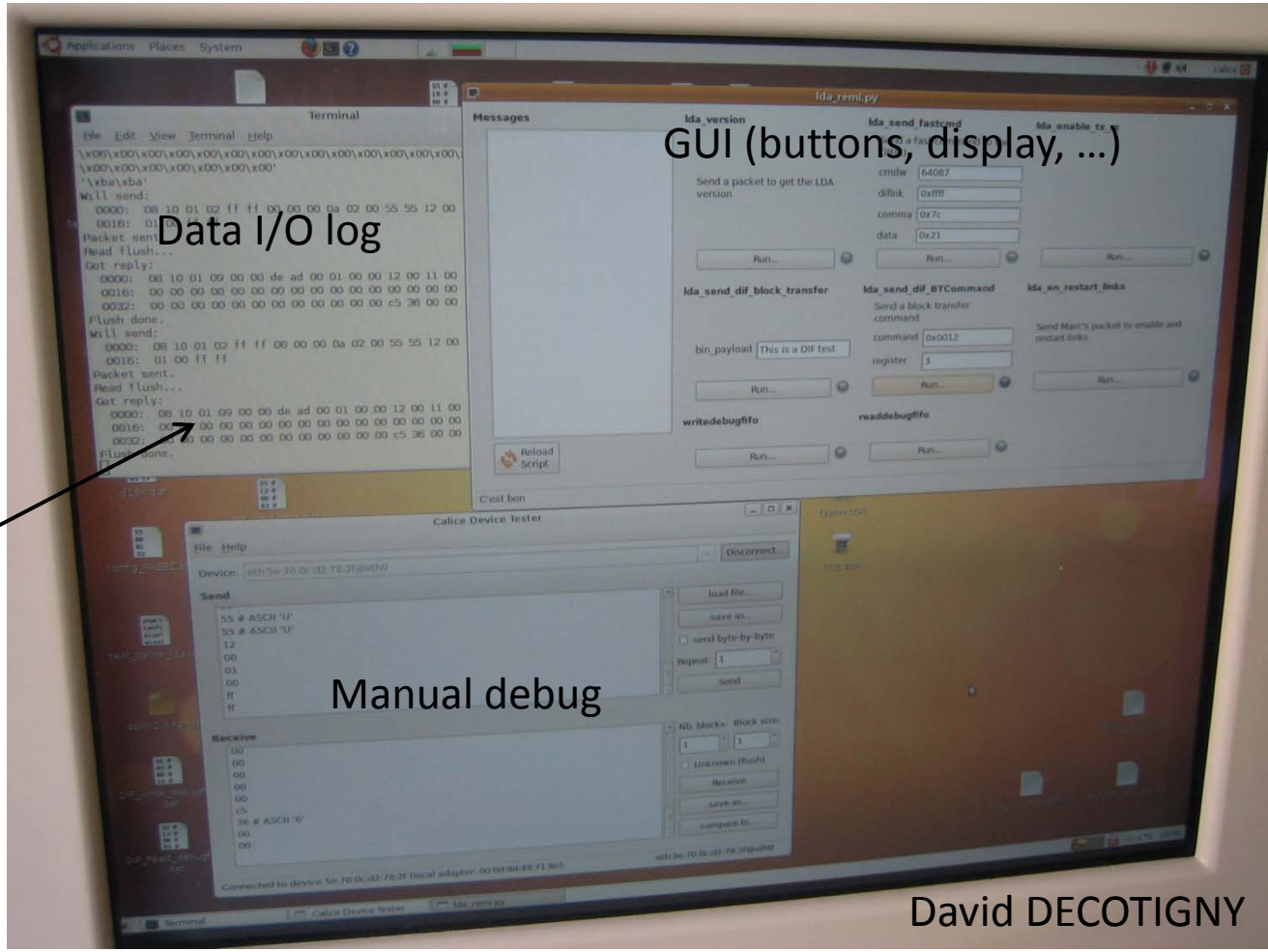
Old screen but new firmware for tests&debug

Some standard procedures are defined

Sripting

Basic interpretation of data

Data received and displayed



Outcome

- Firsts steps toward the CALICE DAQ
  - Thanks to our colleagues from UK
  - Main mechanisms of data exchange were tested a few times
  - 50 MHz clock
- Firmware is being developed
  - Functions to store SC data and manage ROCs
  - Common work done within the DIF task force
- System tests needed
  - Data integrity
- First detector operation foreseen on June on Si-W ECAL prototype (1 ASU, 1 chip)
- Could be extended to other detectors
  - Please wait until September for the system to be fully debugged (validation phase with system level tests)
  - Support from LLR possible