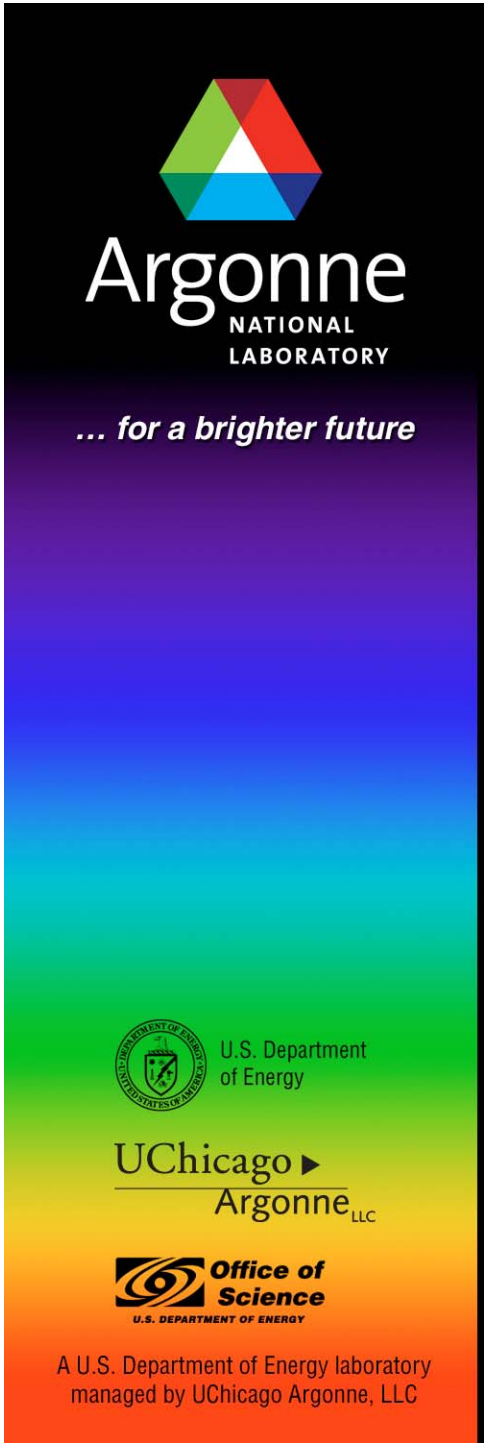


Digital HCAL Electronics
Status of Electronics Production

Gary Drake

Argonne National Laboratory

CALICE Collaboration Meeting

Arlington, TX

Mar. 10-12, 2010

RPC DHCAL Collaboration: → 36 People, 7 Institutions

Argonne National Laboratory

Carol Adams
Mike Anthony
Tim Cundiff
Eddie Davis
Pat De Lurgio
Gary Drake
Kurt Francis
Robert Furst
Vic Guarino
Bill Haberichter
Andrew Kreps
Zeljko Matijas
José Repond
Jim Schlereth
Frank Skrzecz
(Jacob Smith)
(Daniel Trojand)
Dave Underwood
Ken Wood
Lei Xia
Allen Zhao

Boston University

John Butler
Eric Hazen
Shouxiang Wu

Fermilab

Alan Baumbaugh
Lou Dal Monte
Jim Hoff
Scott Holm
Ray Yarema

IHEP Beijing

Qingmin Zhang

University of Iowa

Burak Bilki
Ed Norbeck
David Northacker
Yasar Onel

McGill University

François Corriveau
Daniel Trojand

UTA

Jacob Smith
Jaehoon Yu

RED = Electronics Contributions
GREEN = Mechanical Contributions
BLUE = Students
BLACK = Physicists

Brief Overview of System

General Electronics System Specifications

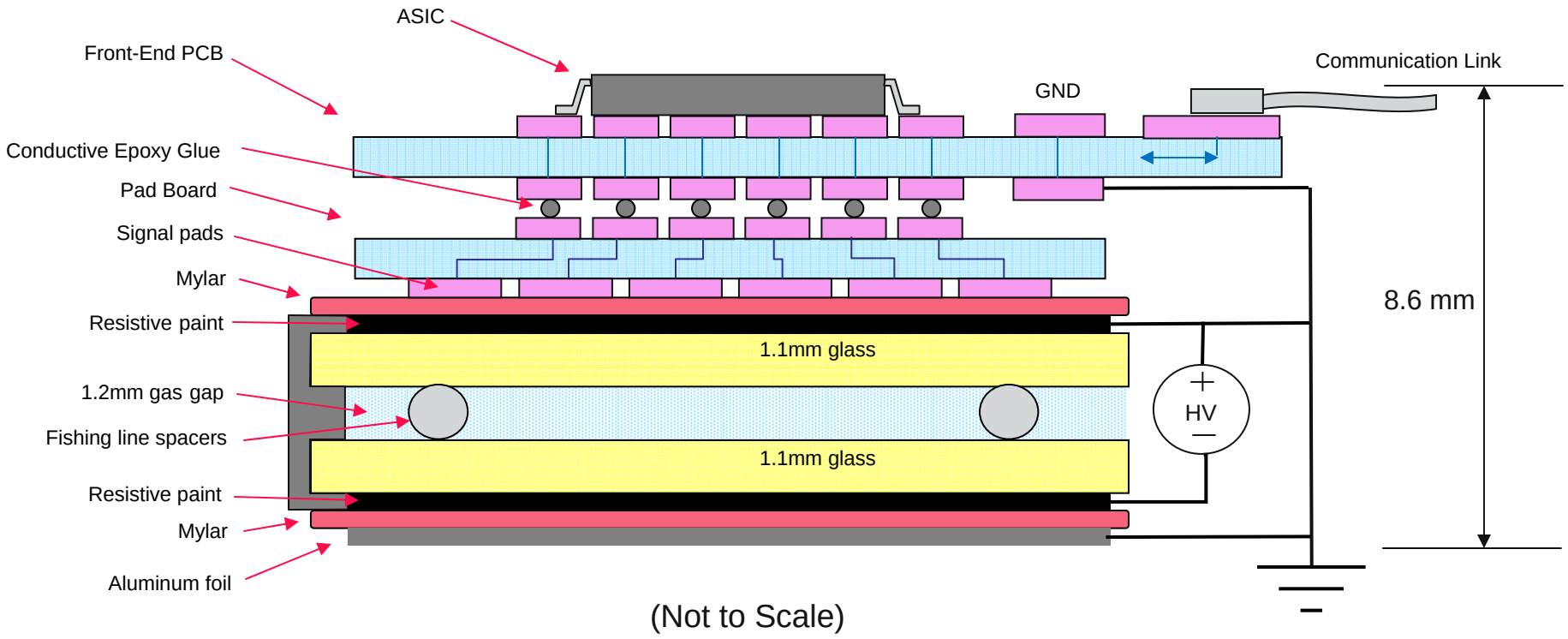
- Front-end instrumentation to use 64-channel custom ASIC
  - 1 cm^2 pads, 1 $meter^2$ planes, 40 planes, → ***400,000 channels***
- Front-end channel consists of amplifier/shaper/discriminator
- ***Single programmable threshold*** → 1 bit dynamic range
  - Threshold DAC has 8-bit range
  - Common threshold for all 64 channels per ASIC
- ***2 gain ranges***
  - High gain for GEMs (10 fC - ~200 fC signals)
  - Low gain for RPCs (100 fC - ~10 pC signals)
- 100 nSec time resolution
- ***Timestamp each hit***
  - 1 second dynamic range → 24 bits @ 100 nSec
  - Synchronize timestamps over system
- ***Data from FE consists of hit pattern in ASIC + timestamp***
  - 24 bit timestamp + 64 hit bits = 88 bits (+ address, error bits, etc.)
  - Readout format: 16 bytes per ASIC

General Electronics System Specifications (Continued)

- Capability for ***Self Triggering*** → Noise, Cosmic rays, ***Data errors***
- Capability for **External Triggering** → Primary method for beam events
  - 20-stage pipeline → 2 μSec latency @ 100 nSec
- Capability of FE to source prompt Trigger Bit (simple OR of all disc.)
- Capability to store up to 7 triggers in ASIC output buffer (FIFO)
- Design for 100 Hz (Ext. Trig) nominal rate
- ***Deadtimeless Readout*** *(within rate limitations)*
- Zero-suppression implemented in front-end
- On-board charge injection with programmable DAC
- Design for 10% occupancy
- Concatenate data in front-ends
- Use serial communication protocols
- Slow controls separate from data output stream
- Compatibility with CALICE DAQ

Detector Configuration

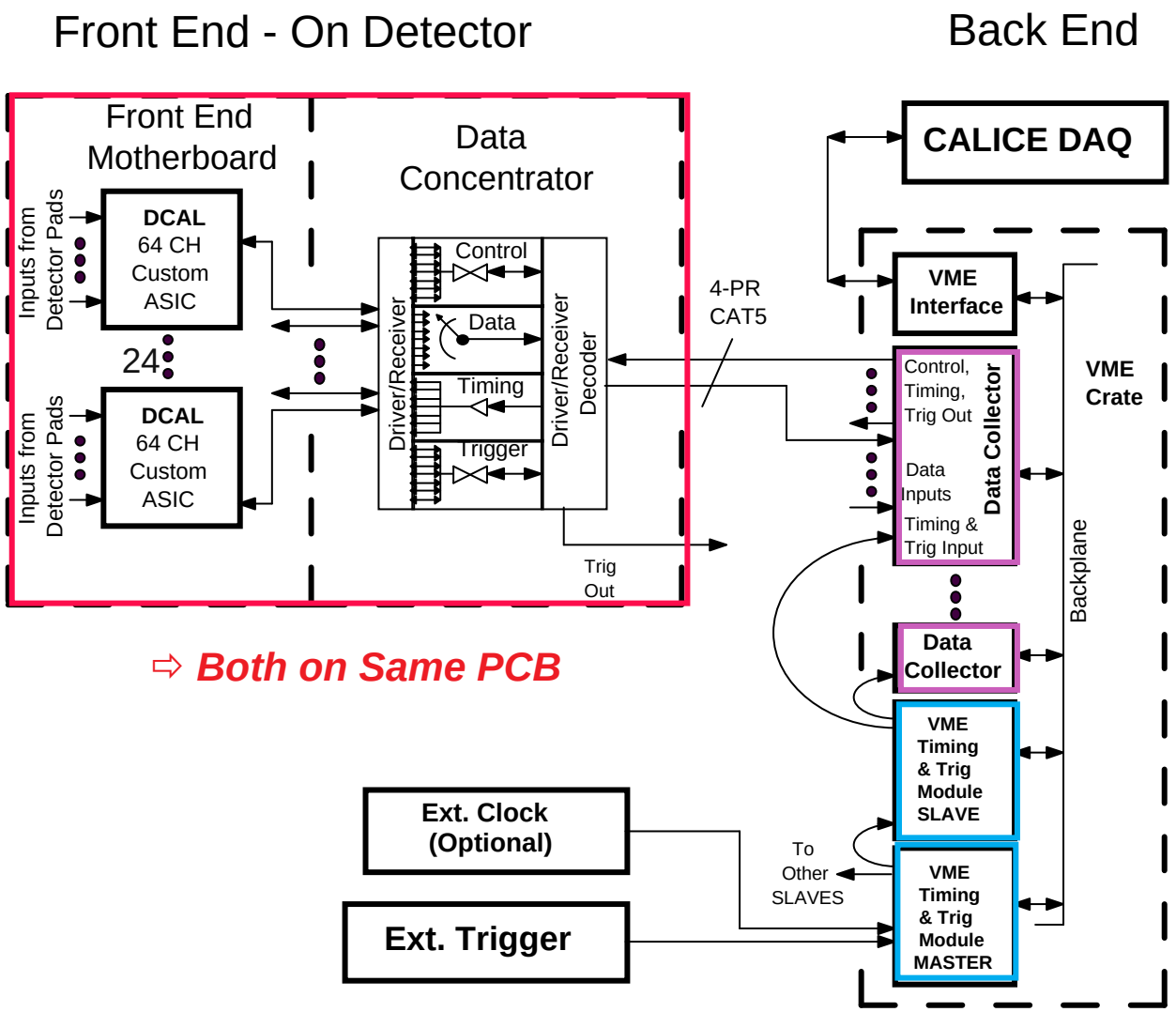
Chamber Construction with Electronics:



(Not to Scale)

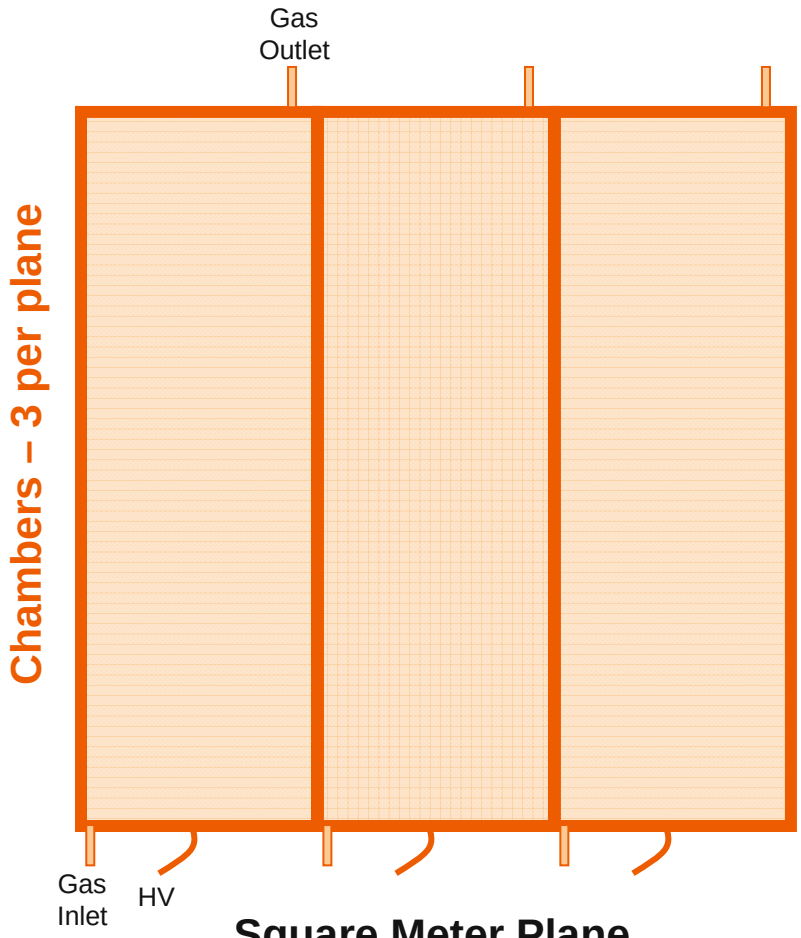
Grounding is important…

System Block Diagram



⇨ ***Both on Same PCB***

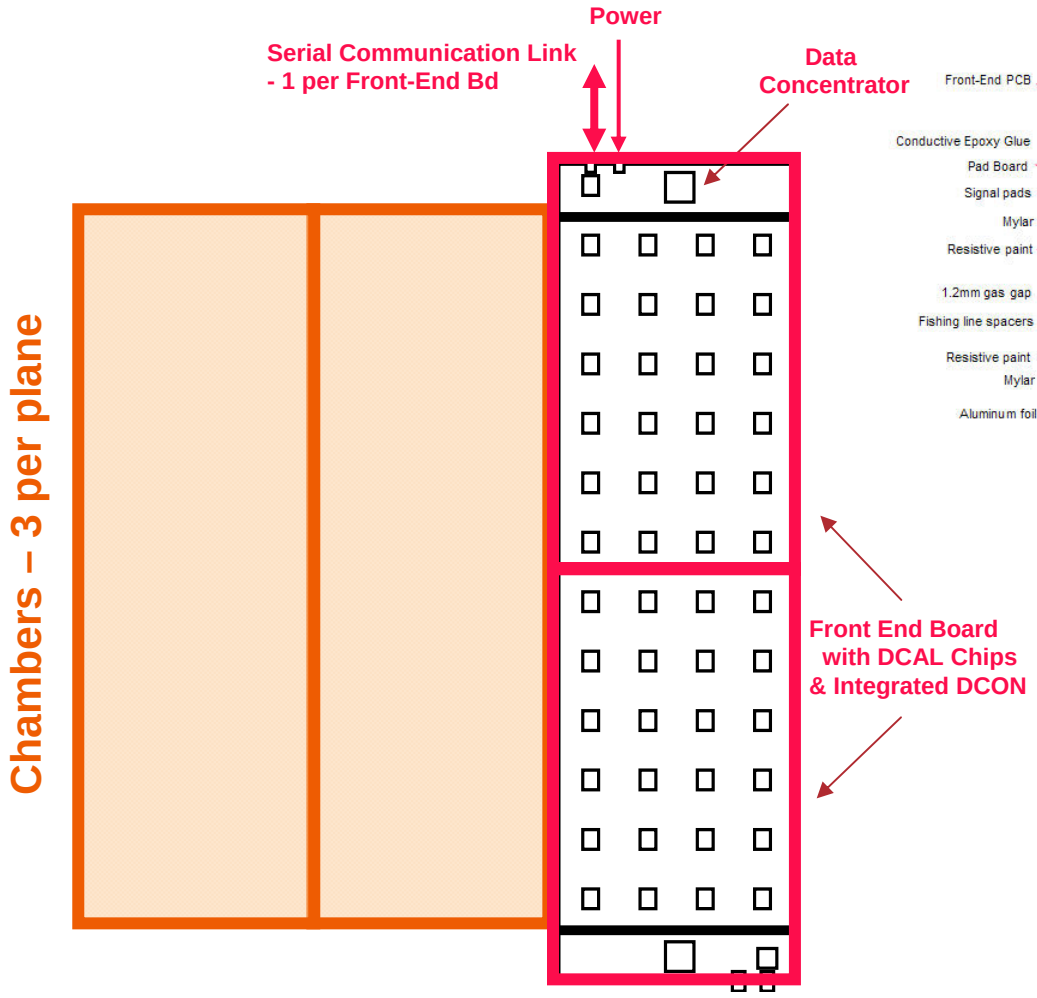
System Physical Implementation

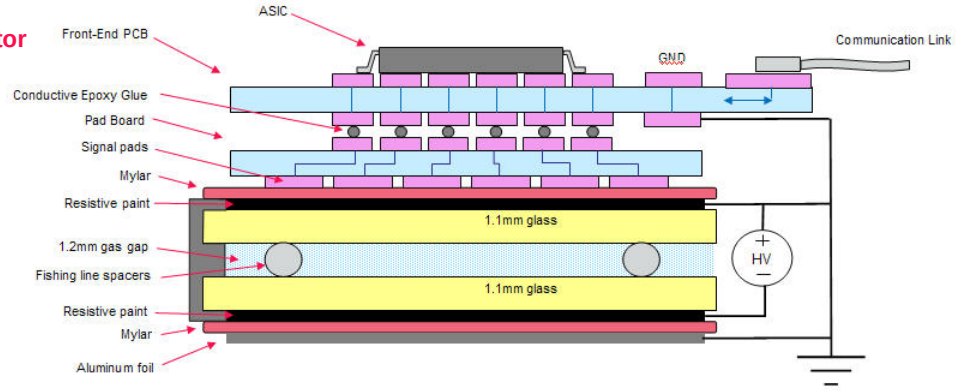


Square Meter Plane
(3) 32 cm X 96 cm chambers

- Plane Construction
  - A plane consists of 3 independent chambers
  - → See Lei Xia's talk Friday

System Physical Implementation (Cont.)



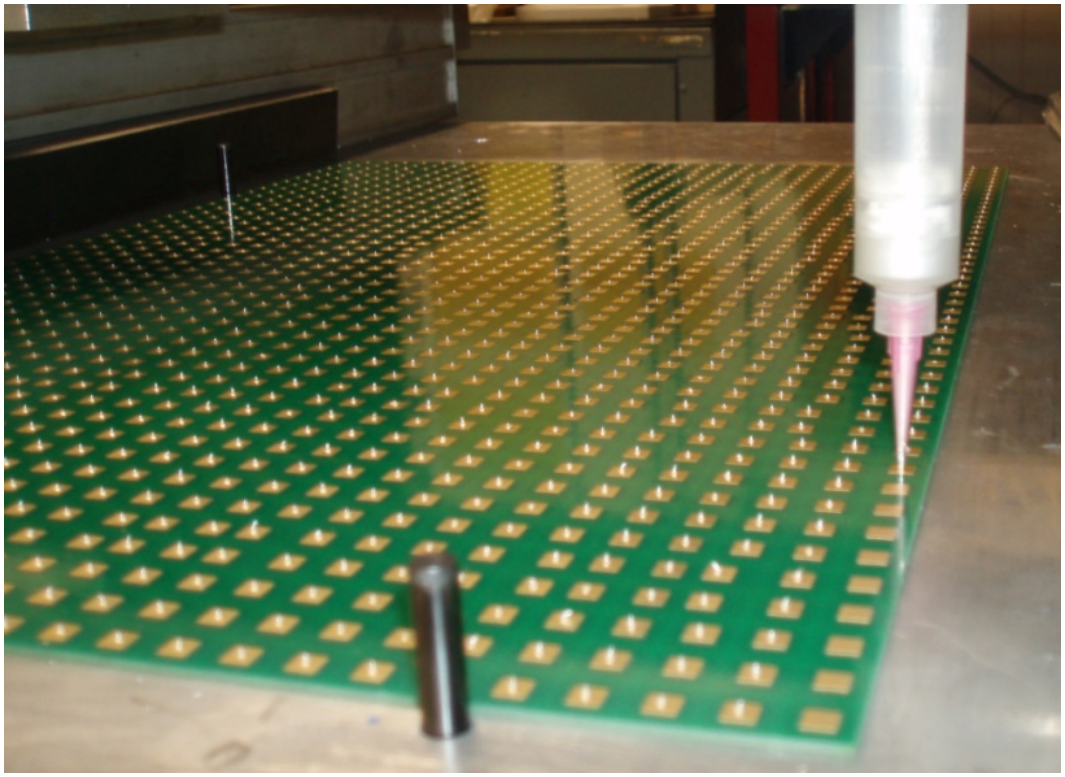


Square Meter Plane
(2) 32 cm X 48 cm Front End Boards per Chamber

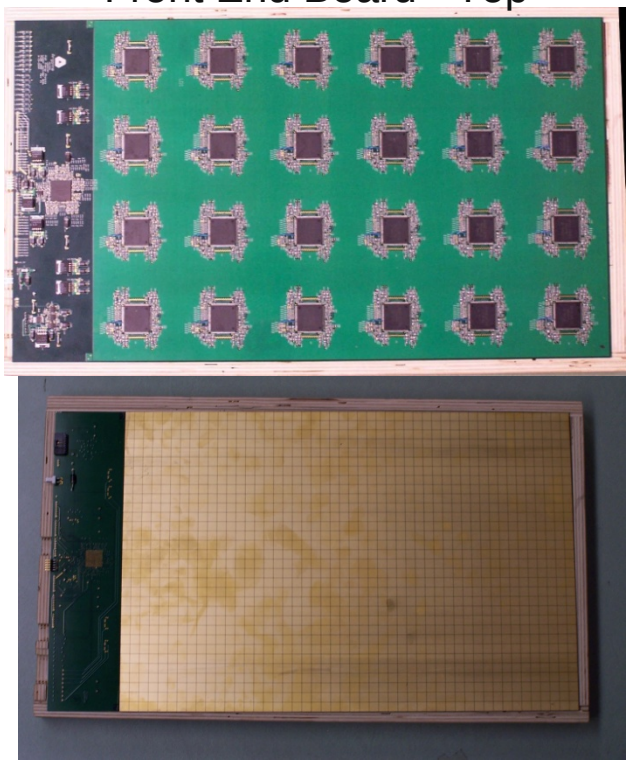
- Front End Board
  - (24) 64-Ch Chips / Bd
  - 1536 Channels / Bd

System Physical Implementation (Cont.)

- Pad Boards
  - Glued to Front End Board using Conductive Epoxy
  - Gluing done by robot, after FEB assembly and check out
  - More in Lei Xia's Talk on Friday

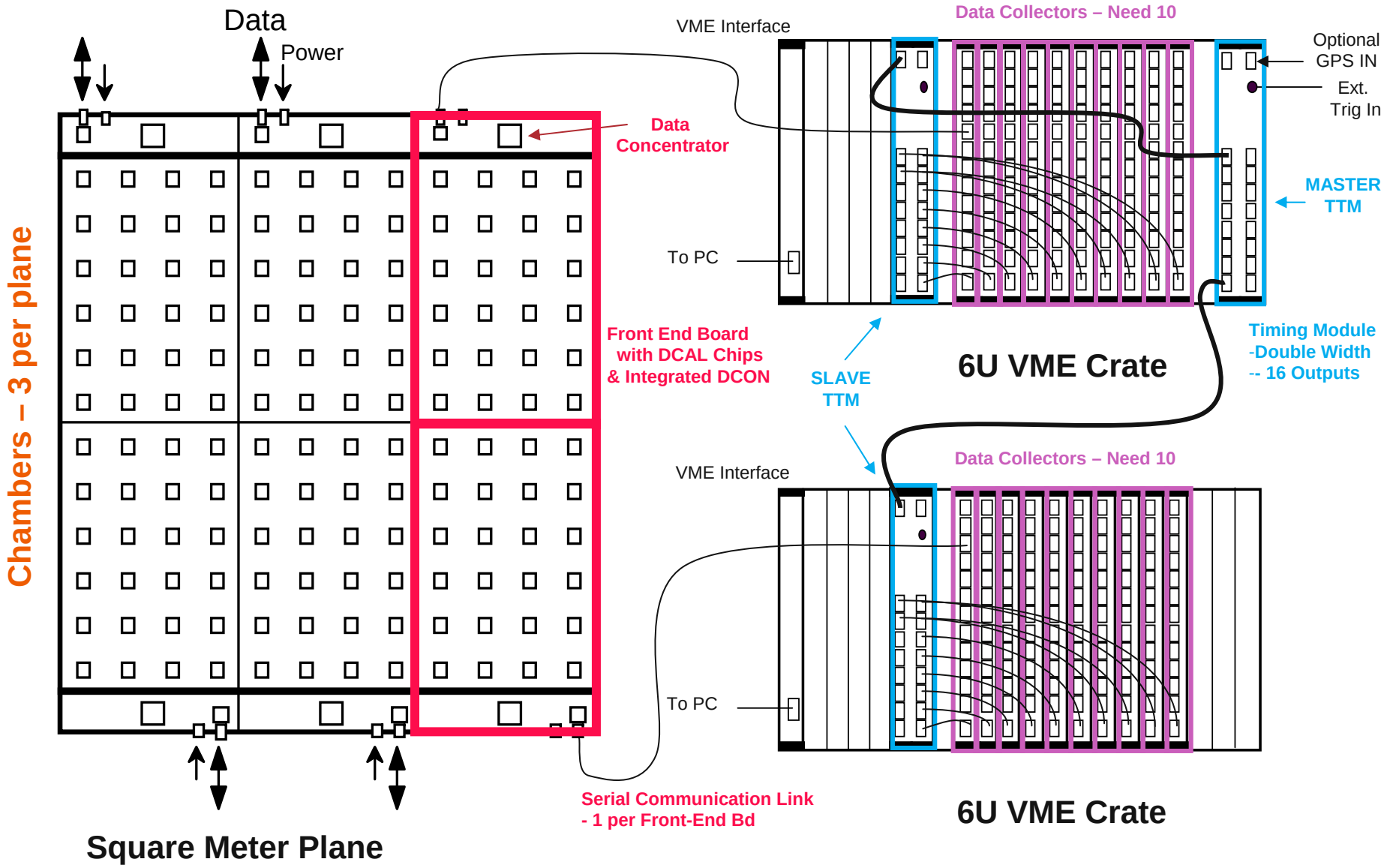


Front End Board - Top



Pad Board - Bottom

System Physical Implementation (Cont.)



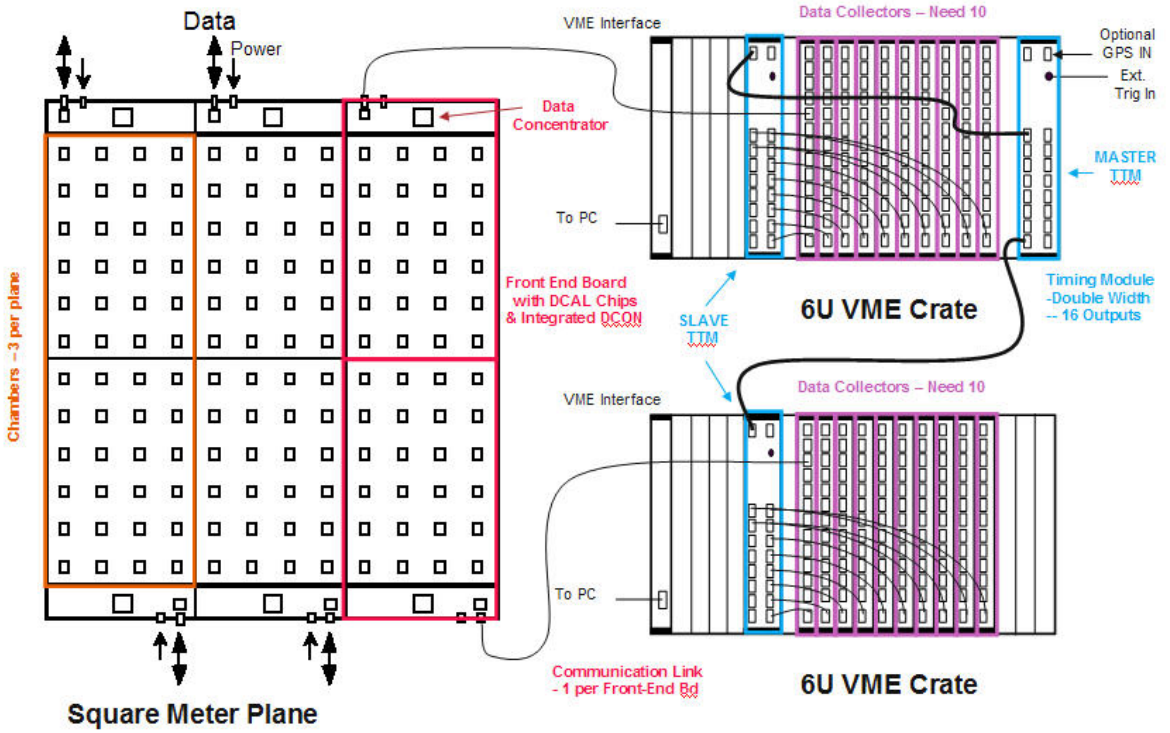
System Physical Implementation (Cont.)

- Square meter plane mounted on cassette using prototype Front End Boards

Plane #1 !!!

Some Numbers

- Planes
  - 38 planes in m^3
- Detector Granularity
  - 1 cm^2 pads
  - 10,000 pads/plane
  - **380,000 ch total**
- Front End Boards
  - 6 per plane
  - **228 total (+ spares)**
- Chips
  - 64 ch/chip
  - 24 chips/FEB
  - **5472 chips total**
- Data Collectors
  - 12 FEB/Data Coll.
  - **20 Data Coll. total**
- VME Crates
  - **2 crates total (1 per side)**



- **Chip Rates (@ 1 TS/trig)**
  - 1 bit/100 nSec out of chips
  - 121 bits/TSlice
    - *64 hit bits → 8 bytes*
    - *24 bits timestamp → 3 bytes*
    - *3 ctrl bit/byte*
  - 12.1 uSec/TS/Chip
  - 24 chips operate in parallel
  - **→ 82.6 KHz max average event rate**
  - Use Zero Suppression…

- **DCON Output Rates**
  - 16 bytes/TSlice/chip
  - 25 nSec/nibble
  - → 12.8 uSec/TSlice/chip
  - **78 K Tslices/sec max rate**
  - Zero Suppression helps
  - Example:
    - *4 chips hit/event avg*
    - *Max event rate: 19KHz*
  - **WC: 78 K / 24 = 3.2 KHz**

Power Distribution System

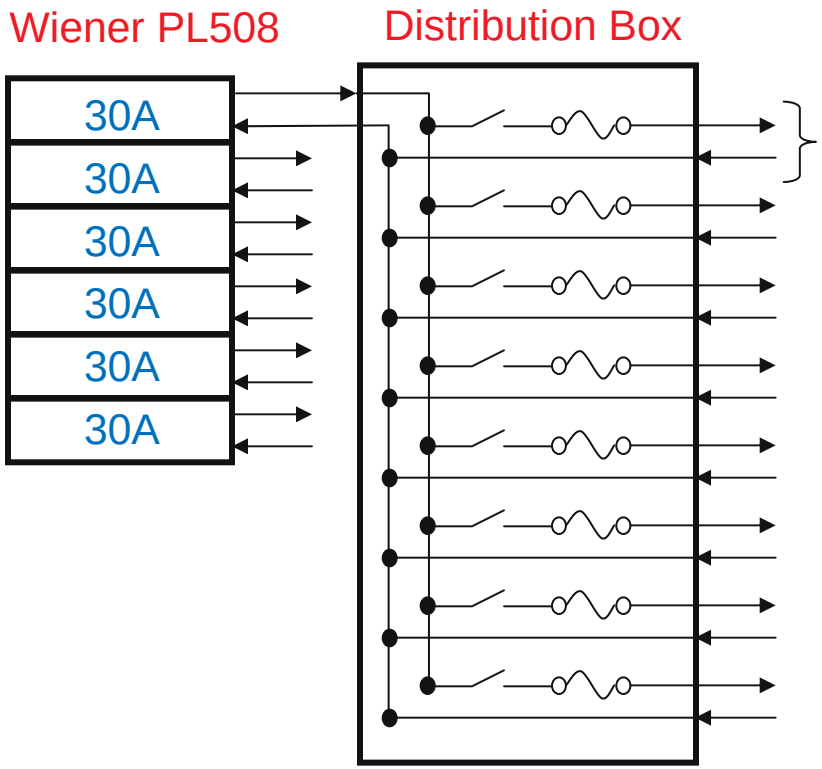
- **Cubic meter detector power requirements:**
  - 3A / FEB @ 5V
  - 40 planes * 6 FEBs/plane * 3.0 amps/FEB = 720 amps at 5V
- **Solution:**
  - 5 Wiener PL508 chassis
  - Each PL508 has six independent 5V at 30 amp supplies
  - 5 PL508 * 6 PS/PL508 * 30 amps/PS = 900 amps total ampacity
  - Operate at ~80% of capacity
  - 1 Wiener supply powers 8 Front End Boards

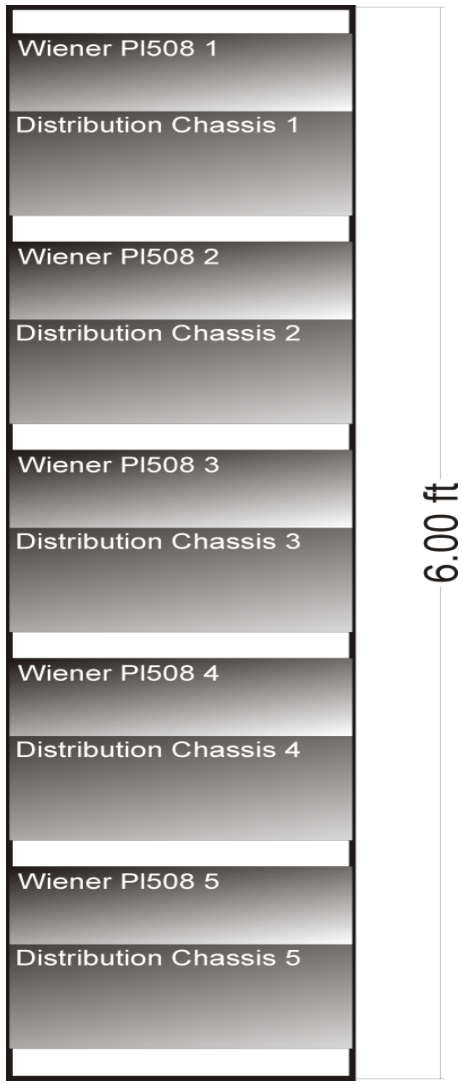
- **Power Numbers**
  - 100 mA/ASIC @ 2.5V
  - 3.9 mW/ch
  - 3A/FEB @ 5V (ASICs run at 2.5V)
  - 15W/FEB
  - 90W/plane
  - 3.6 KW/cubic meter

⇨ *Not designed for Low Power…*

Power Distribution System (Cont.)

- Need Power Dist. Box to distribute voltages to Front End Boards
- Rack Configuration
  - Power supplies will fit into one rack
- Power Distribution
  - Custom distribution boxes, with fuses, safe wiring, etc.





Production Quantities

Item	Needed for Detector	Possible Tail Catcher	Spares	Teststands	Total
DCAL Chips	5472	1008	2164	0*	8644
Front End Bds	228	42	10	0*	280
Data Collectors	20	4	3	1	28
VME Crates	2	0	1	2	5
VME Processors	2	0	1	1	4
Timing Module	3	0	2	3	8
Wiener Power Supplies	5	2	1	0	8
Power Dist. Boxes	5	2	1	0	8

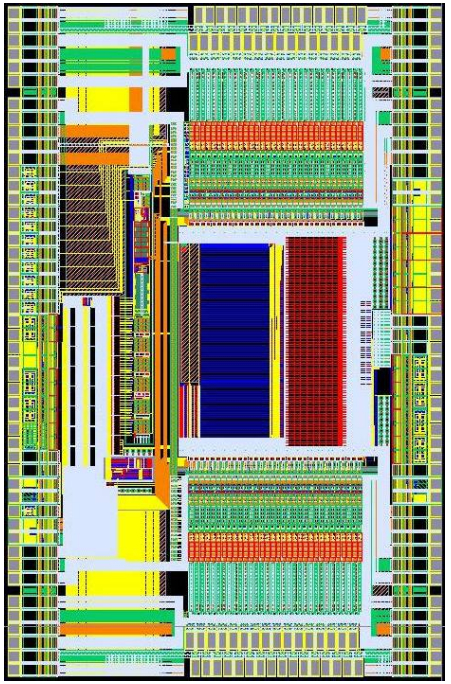
* Use Prototypes

Status of System Components to Date

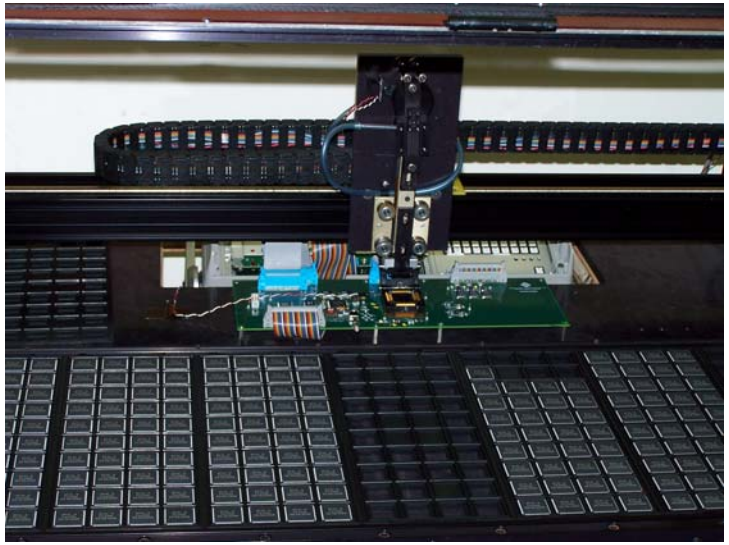
Status of DCAL3 Production

- **Chip Fabrication:**
  - 11 wafers, 10,300 chips, fabricated, packaged, in-hand
- **Chip Testing**
  - All chips tested using robot at Fermilab
  - Results:
    - *8644 good parts → 84% yield → Average*
    - *1 bad wafer → 25% yield → Did not use*

⇨ ***Complete***



DCAL3 Layout



Robotic Chip Tester

Chip Storage (~1/2 total)

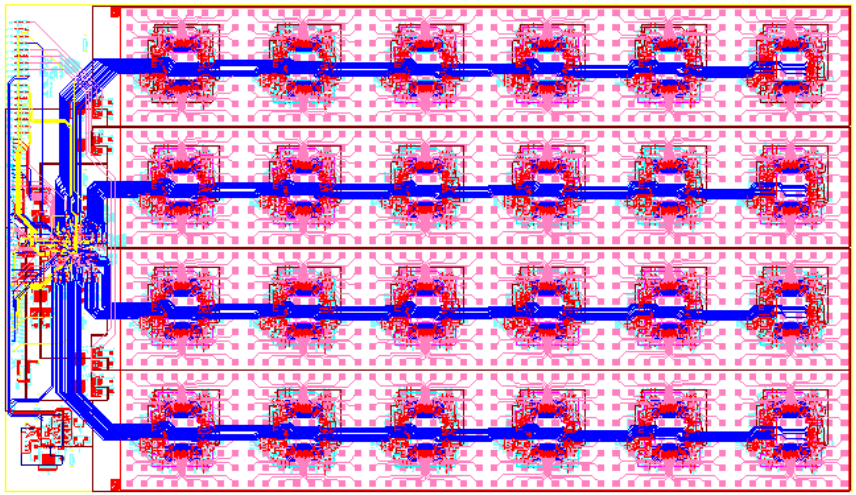
Fermilab

Status of Front End Board Production

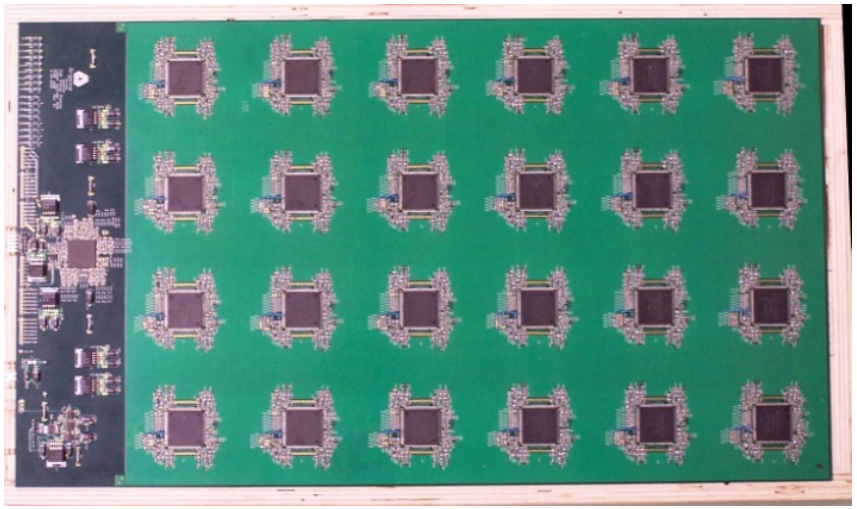
- **Progress since Lyon**
  - Found 3 problems with prototype FEB
    - *LVDS outputs of DCON FPGA not true LVDS → had common mode component*
    - *We had a single-ended clock line between receiver & FPGA, ~10 cm*
    - *We found a stability problem with the PLL in the FPGA*

    ⇨ ***Caused relatively rare errors in data collection - ~1E-8***

    ⇨ ***Required additional iterations in design of prototype to find & fix***
  - We also found a susceptibility for damage to FEB from Chamber Sparking
    - *Fixed using grounding and shielding techniques → System Grounding Plan*

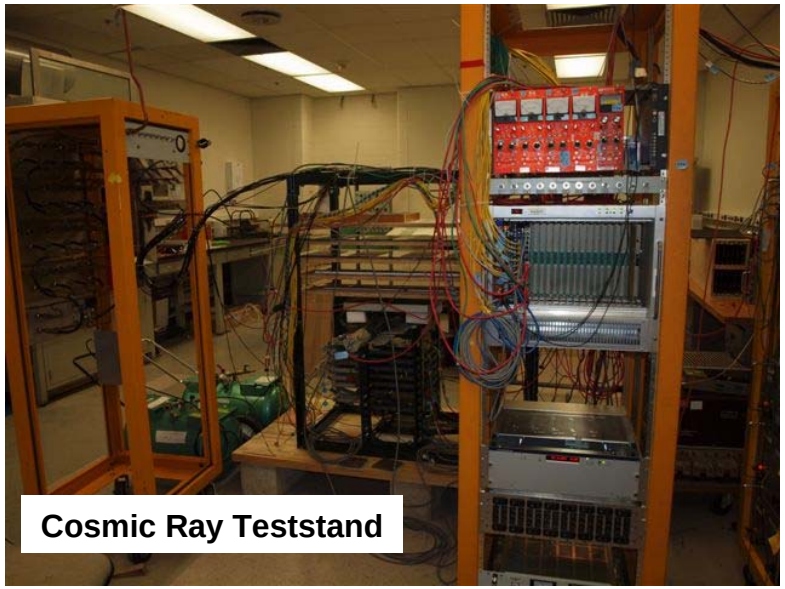


8-layer FE-board (3 layers shown)

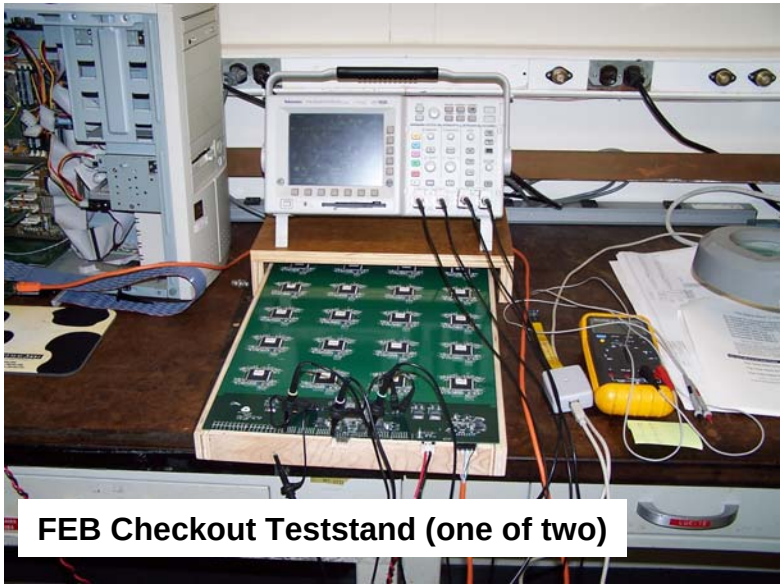


Status of Front End Board Production (Cont.)

- **Status today**
  - All problems in layout fixed
  - All problems in firmware fixed
  - System has been run in Cosmic Ray Teststand for long periods with no errors
  - System has been run in “Torture Mode” (self trigger, low threshold) with no errors
  - System has been operated with a “bad” chamber sparking → *Now Robust!*



Cosmic Ray Teststand

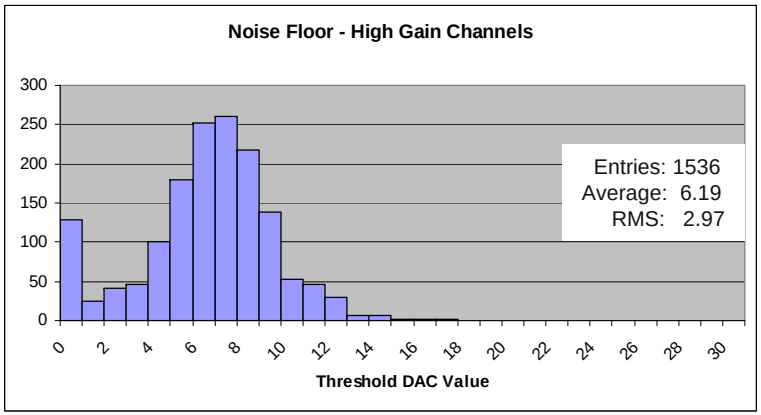


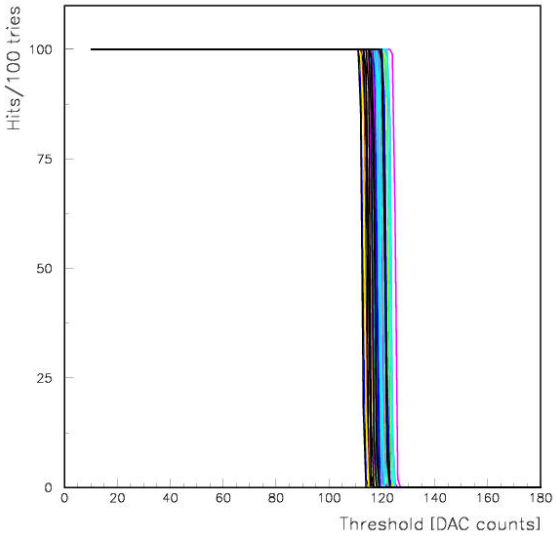
FEB Checkout Teststand (one of two)

⇨ ***Production fabrication of PCBs now in progress***
⇨ ***FEB Checkout Teststands fully operational***

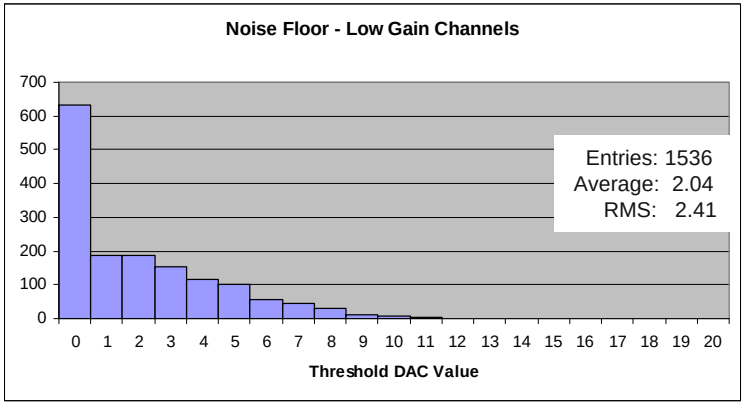
Status of Front End Board Production (Cont.)

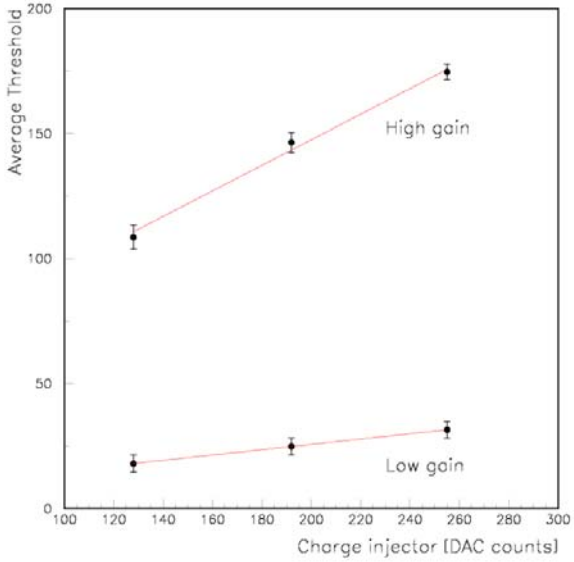
A Few Results





Channel Uniformity for Threshold Scans Using On-board Charge Injection





High Gain:
~0.3 fC / THR_DAC_CNT
→ 75 fC Range

Factor of 6.4

Low Gain:
~1.9 fC / THR_DAC_CNT
→ 480 fC Range
→ Operate ~ 190 fC for RPC

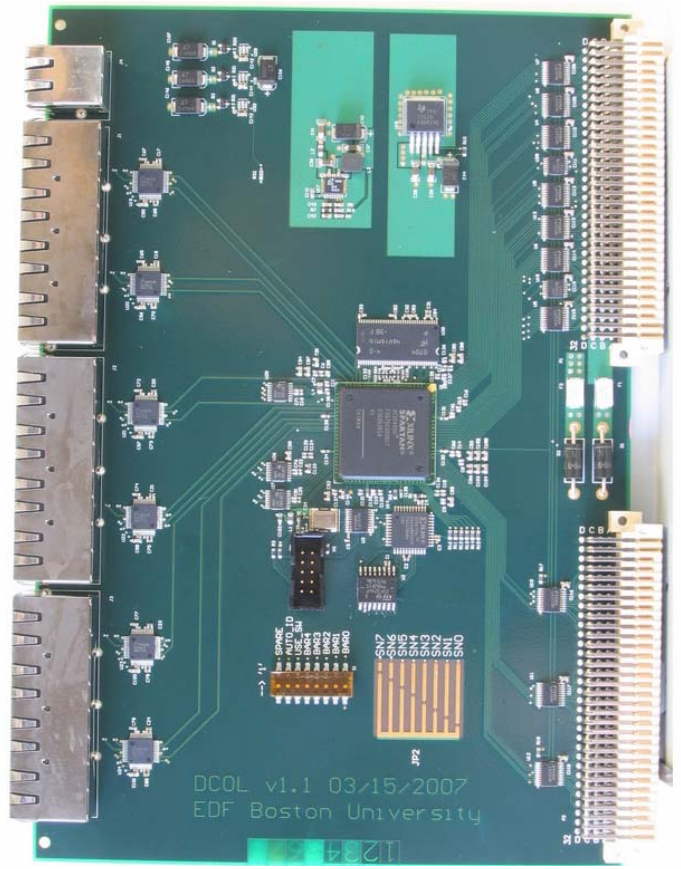
Measurements of Noise Floor

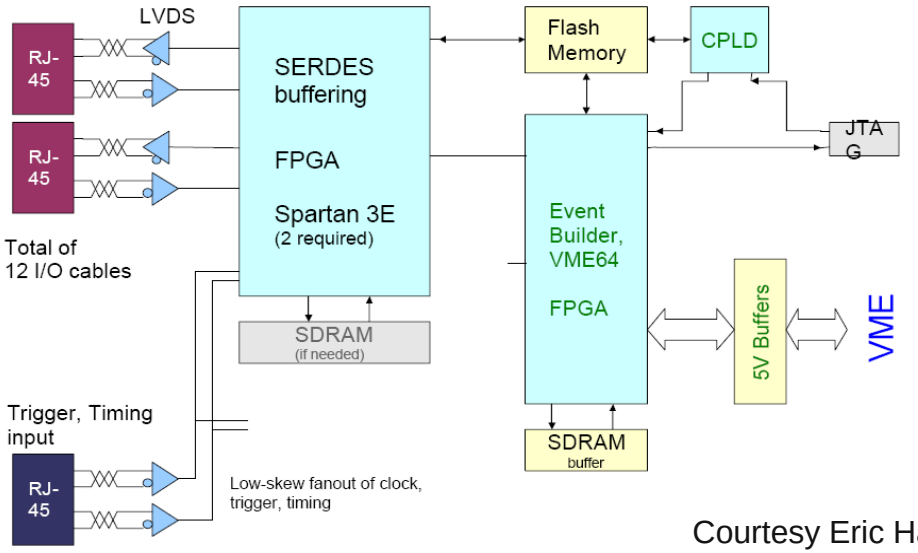
Single channel measurements, 24 Ch FEB
Ext. Trig, No Pad Bd, No Chamber, No HV
Entire Front End Board, 1536 Channels

Status of Data Collector Production

- Production
  - 30 boards fabricated & assembled
  - Testing ~75% complete
  - ~15 delivered to Argonne

⇨ ***Will be ready when needed***



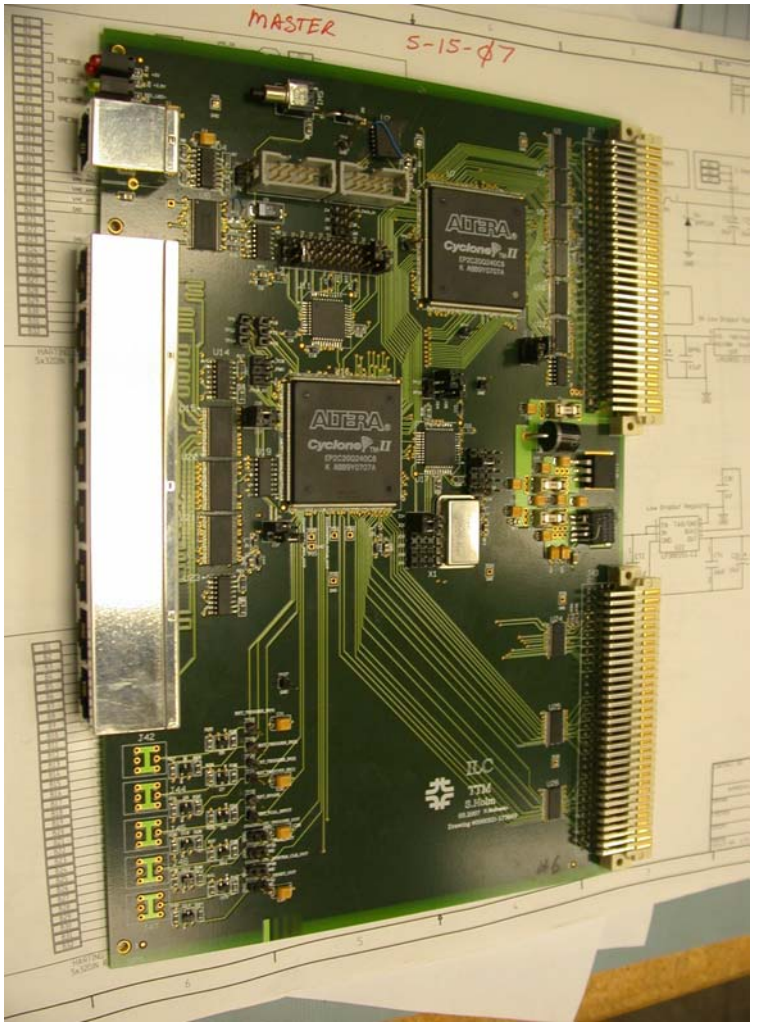


Courtesy Eric Hazen, BU

Status of Timing & Trigger Module (TTM) Production

- Status
  - Redesign completed
    - *Add outputs: 8 → 16*
    - *Makes double-width*
    - *Add capability to use as MASTER or SLAVE*
      - Set a bit to select
  - Production
    - *Need 3 for detector*
    - *Fabrication beginning now*
    - *Assemble ~ April*

⇨ ***Prototypes OK for now***
⇨ ***Will be ready when needed***

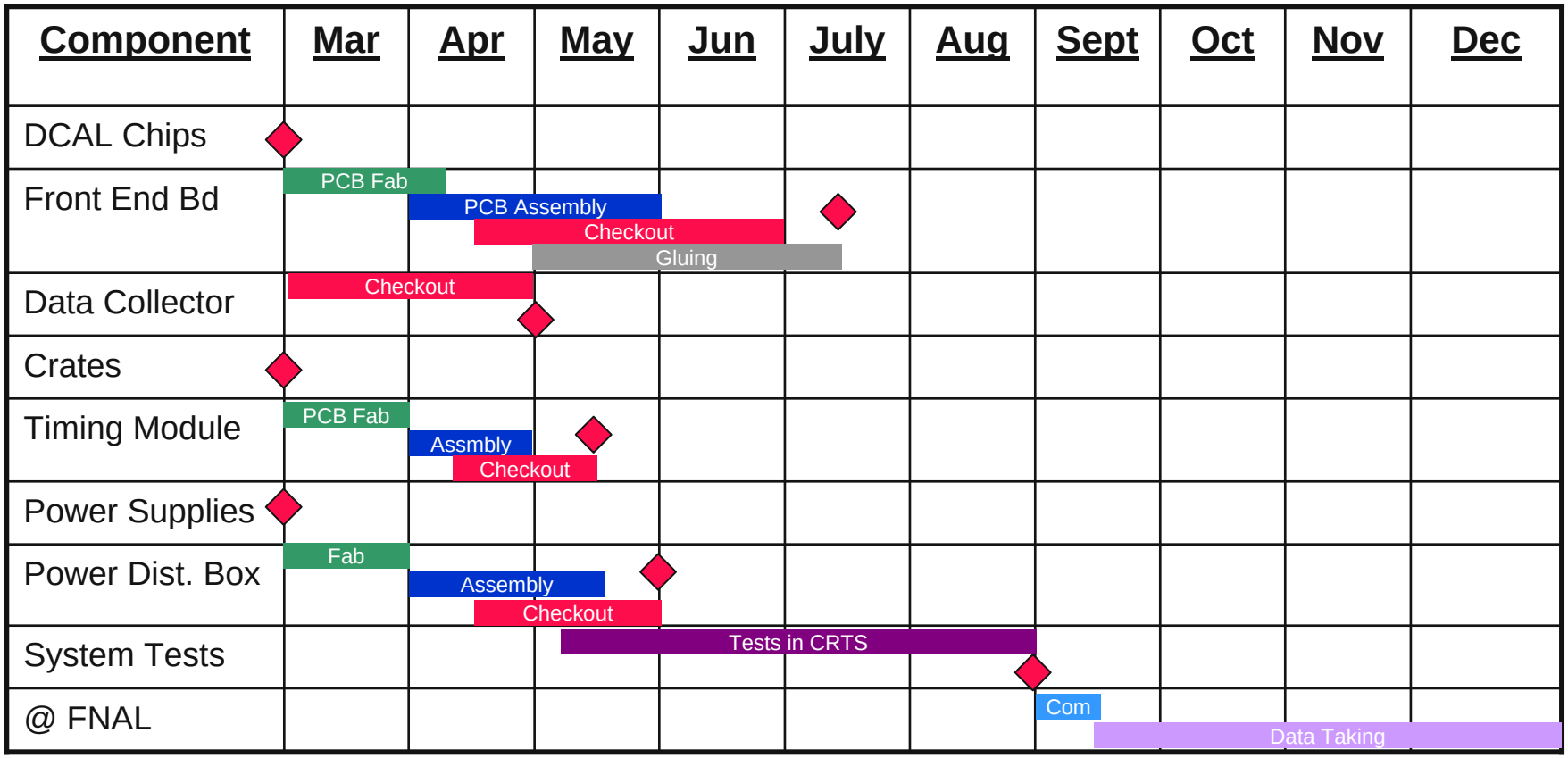


Fermilab

Schedule & Plans

Schedule & Plans

- Projected Production Schedule
  - ~Produce 1 plane per day, all phases of production



Summary

- **We have completed an extensive development program for the electronics of this project**
  - The design of the Front End Board was by far the most difficult aspect of the project
  - The prototype system has been thoroughly tested
    - *Good electronics noise performance → Careful layout & circuit design*
    - *Good measurement of cosmic rays*
    - *Data error rate < 1E-12 → through extensive testing*

- **Production preparations in progress**
  - DCAL ASIC
    - *Checkout complete*
    - *8600 chips in hand → 84% yield*
  - Front-end Board & Pad Board
    - *PCB fabrication in progress*
    - *Plans & preparations for assembly & checkout in place*
    - *Still the critical path in the project*
  - Data Concentrator, Timing Module, Power Dist. Box → Production of all in progress

⇨ ***Begin tests in Cosmic Ray Teststand in May***
⇨ ***Begin installation & commissioning at FNAL in September***