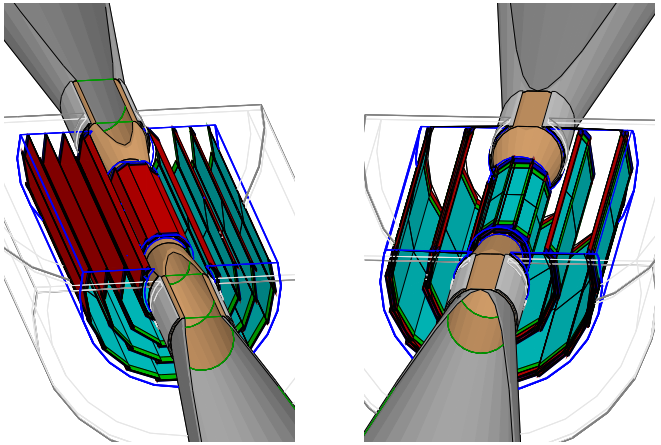
Plans of the VTX Group for the TDR

Yasuhiro Sugimoto & Marc Winter

OUTLINE

- Work plan on performance target values
- Foreseen pixel technology R&D
- Work plan on system integration
- Uncovered tasks
- Summary

Performance Target Values (1/2)



- **Improve justification of $\sigma_{IP} = a \oplus b/p \cdot sin^{3/2}\theta$**
  - $\Rightarrow$ guidance for pixel and ladder R&D

- **Studies based on realistic & detailed phys. simulations**

  (including beam background)

  - ⁂ justify the constraint on a ($\leq$ 5 μm):
    - determine the necessary single point resolution
    - estimate necessary alignment accuracy and monitoring
  - ⁂ justify the constraint on b ($\leq$ 10 $\mu m \cdot GeV/c$):
    - estimate the acceptable (ladder) material budget (b $\propto \sqrt{X/X_0}$)
    - estimate the acceptable inner radius (b $\propto$ R_{in})
    - special concern: low P tracks and vertex charge

- **Quantify necessary performance improvements for running at $\sim$ 1 TeV**

Performance Target Values (2/2)

- **Improve justification of the time resolution**

  ⇛ guidance for pixel and ladder R&D

	radius [mm]		ladder length [mm]		read-out time [μs]	
geometry	VXD-03	VXD-05	VXD-03	VXD-05	VXD-03	VXD-05
layer 1	*15.0*	*16.0/18.0*	*125.*	*125.*	*25–50*	*25–50*
layer 2	*26.0*	*37.0/39.0*	*250.*	*250.*	*50–100*	*100-200*
layer 3	*37.0*	*58.0/60.0*	*250.*	*250.*	*100-200*	*100-200*
layer 4	*48.0*		*250.*		*100-200*	
layer 5	*60.0*		*250.*		*100-200*	

- **Studies based on realistic & detailed phys. simulations**

  (based on critical beam background consideration)

  ※ evaluate degradation of physics performance as a function of increasing occupancy

  ※ compare continuous and delayed read-out

  ※ study impact of track matching with surrounding detectors (bunch tag)

Pixel Technologies (1/2)

- **Pursue pixel technology R&D inside & outside the ILD community**
  - **a)** inside ILD: MIMOSA sensors, FPCCD, 3D (CAIRN)
  - **b)** outside ILD: DEPFET, APSEL, 3D (INFN), others ?
- **Achieve pixel technology specifications at various degrees (a, b, c, d)**
  - **a)** proof of principle
  - **b)** small prototype performance vs specifications:
    σ_{sp}, thinning, read-out speed, radiation tolerance, P_{diss}.
  - **c)** real scale (20-30 % of final sensor area) validation of a) $\oplus$ b)
  - **d)** including system integration aspects: mechanical support, servicing (cooling, power pulsing)
- **Aim at providing a status of each R&D (including its perspectives) at the time of the TDR**

Pixel Technologies (2/2)

- **Make sure that $\geq$ 1 technology (continuous or/and delayed read-out) is qualified at level c) or d)** $\Rightarrow$ nearly all prominent specs satisfied within a factor ≤ 2

- **Identify consequences of technology specific system integration issues:**
  - power pulsing
  - delayed read-out vs continuous read-out
  - etc.

- **Clarify performance perspectives at 1 TeV:**
  - which technologies are best suited for running at 1 TeV ?
  - which specific R&D should be performed ?
  - etc.

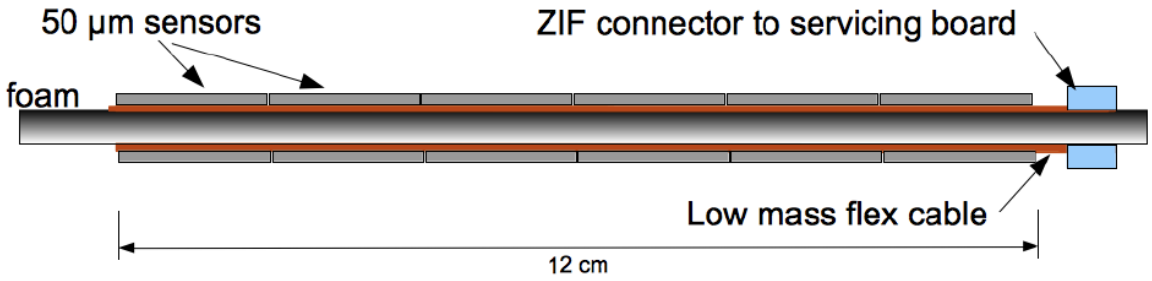
System Integration : General Remarks

- **System Integration is a critical & prominent VTX topic for TDR:**
  - very challenging material budget (may be more critical with power cycling ?)
  - target specifications ($\leq$ 0.16 % X_0 / ladder) well beyond the state of the art
  - substantial amount of work remaining to be done
  - ladder concept is (partly) pixel technology dependent
  - 2 ladder concepts: single-sided vs double-sided

- **4 identified developments under way :**
  - inside ILD: double-sided ladder by the PLUME collaboration
    and unsupported single-sided ladder (SERWIETE project)
  - outside ILD: single-sided ladders for SUPER BELLE by the DEPFET collaboration
    and for STAR at RHIC by the CMOS collaboration

System Integration : PLUME Project

- **PLUME** $\equiv$ **P**ixelated **L**adder using **U**ltra-light **M**aterial **E**mbedding



- **Objectives :**
  - achieve a low material, double-sided, ladder prototype for an ILC vertex detector by 2012
  - use MIMOSA, ISIS (???), other (?) sensors
  - evaluate benefits of 2-sided concept (mini-vectors) :
    σ_{sp}, alignment, shallow angle pointing, elongated ($\equiv$ fast r.o.) vs square ($\equiv$ precise pixels)

- **Collaboration:** Bristol - DESY - Oxford - Strasbourg (synergy with Vertex Detector of CBM/FAIR)

- **Working plan:**
  - 2009: prototype Nr.0 (2 sensor on each side) tested at CERN-SPS
  - 2010: prototype Nr.1 (6 MIMOSA-26 sensors on each side) featuring $\sim$ 0.6 % X_0 tot. mat. budget
  - 2011: prototype Nr.2, like Nr.1 but with 0.4 - 0.5 % X_0 total material budget
  - 2012: prototype Nr.3, like Nr.2 but with 0.3 - 0.4 % X_0 ttotal material budget
    (potentialy one side with $\sim$ 10 μs read-out time)

System Integration : SERWIETE Concept

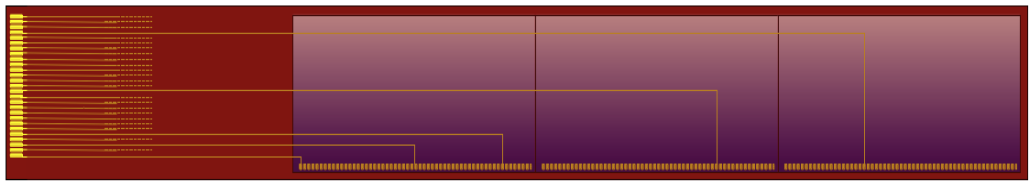
- **Unsupported ladder:** $\equiv$ **SE**nsor **R**ow **W**rapped **I**n an **E**xtra-**T**hin **E**nvelope **(SERWIETE)**

- **Objectives :**
  - achieve a sensor assembly mounted on flex and wrapped in polymerised film with $\lesssim$ 0.15 % X_0 in total
  - evaluate possibility of mounting unsupported ladder on cylindrical surface (serving as mechanical support)
  - proof of principle expected in 2012

Proto 1 ▷ Spring 2010

- **Working programme:**
  - prototype Nr. 1 (2010) made of 1 sensor : MIMOSA-18 (analog output, $\lesssim$ 4 ms)
  - prototype Nr. 2 (2011) made of 3 sensors : MIMOSA-26 (digital output, $\lesssim$ 110 μs)

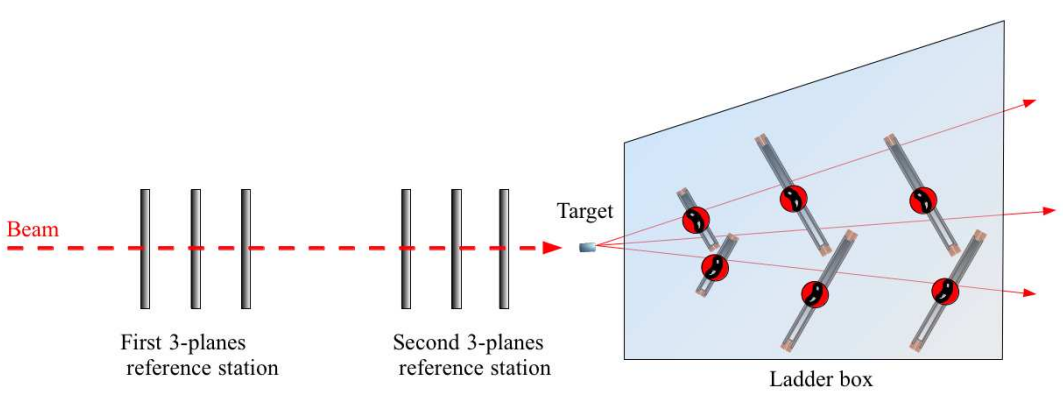
Proto 2 ▷ Summer 2011

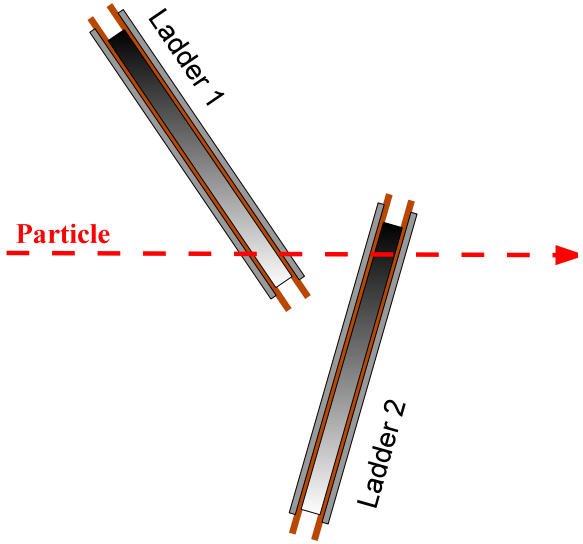


- **Context of development:**
  - E.U. project Hadron Physics 2 (FP-7)
  - collaboration between Frankfurt (CBM/FAIR) and IPHC/Strasbourg

Infrastructure to Study Integration Issues

- **On-beam test infrastructure:**
  - ⁂ Large Area beam Telescope (LAT)
  - ⁂ Alignment Investigation Devices (AID): mini-telescope and/or ladder box
  - ⁂ Very thin removable target





- **Off-beam test infrastructure:**
  - ⁂ thermo-mechanical studies, including effect of air-flow based power extracting system
  - ⁂ power cycling effect in strong magnetic field, e.g. Lorentz forces, on ultra-light ladders
- Project part of AIDA–FP7 proposal (coll. of PLUME membres + Univ. Geneva + Univ. Warsaw) :
  - ⟶ project likely to happen independently of AIDA approval

Uncovered Tasks

- **Development (engineering) of global design concept :**
  - design of cryostat (ladder support, field cage, cabling, etc.)
  - inner layer supports on beam pipe
  - powering and cabling
  - cooling
  - DAQ
- **Global inner tracker concept optimisation :**
  - track link with neighbouring sub-detectors
  - bunch tagging provided by these sub-detectors
  - special concern: shallow angle vertexing

Summary

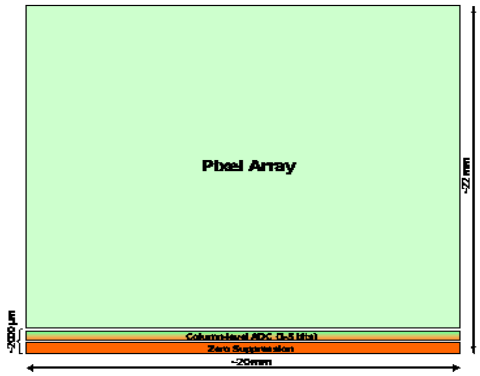
- **Improved target values are requested for more precise guidance to VTX design :**
  - based on complete realistic simulations including beam related backgrounds
  - comparison between double-sided and single-sided ladder design performances
- **Several pixel technologies will continue evolving :**
  - CMOS sensors, FPCCD, DEPFET (for Super Belle), etc.
  - $\geq$ 1 technology expected to be mature enough to give credit to predicted VTX performances
- **Substantial effort on system integration :**
  - full scale double-sided ladder (PLUME coll.) & unsupported ladder (SERWIETE for beam pipe)
  - outside ILD: evolution of DEPFET-ladder for SUPER BELLE & CMOS-ladder for STAR
  - ladder material budget target value ($\lesssim$ 0.16 % X_0) unlikely to be reached by 2012
  - extensive studies on alignment foreseen, as well as on power cycling
- **Several major tasks remain uncovered :**
  - cryostat design, cooling and cable implementation, ...
  - integration in inner tracking system and in IP environment (beam pipe)

BACK UP SLIDES

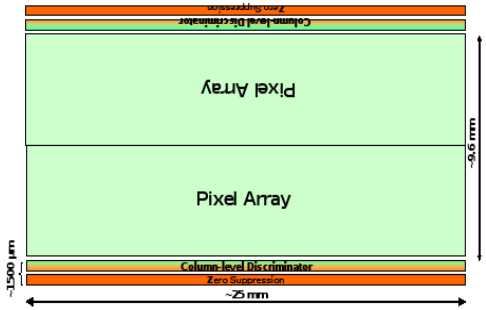
From MIMOSA-26 to the ILC Design

- **Ellaborate on MIMOSA-26 (EUDET BT) full size sensor:**

- **Outer layers ($t_{int} \sim$ 100 μs) :**
  - pitch $\lesssim$ 35 μm (need phys. studies)
  - 4-bit ADC $\Rrightarrow$ $\sigma_{sp} \sim 3\ \mu m$
  - 576 col. of 576 pixels $\Rrightarrow$ 2x2 cm^2



- **Inner layers ($t_{int} \sim$ 25 - 50 μs) :**
  - double-sided r.o. $\Rrightarrow$ twice shorter (= faster) columns
  - pitch $\lesssim$ 15 μm
  - binary r.o. $\Rrightarrow$ $\sigma_{sp} \lesssim 3\ \mu m$
  - 1600 columns of 320 pixels $\Rrightarrow$ $\lesssim$ 24x0.95 mm^2



- **The path to $\lesssim$ 10–20 μs:**
  - exploit double layer concept to implement elongated pixels on one side of inner layer
  - reduced nb of pixels per column $\Rrightarrow$ shorter read-out time $\Rrightarrow$ goal: factor 4–6 w.r.t. square pixel side
  - depleted epitaxial layer $\Rrightarrow$ wider sensing diode spacing $\Rrightarrow$ $\lesssim$ 10 μs may be reachable