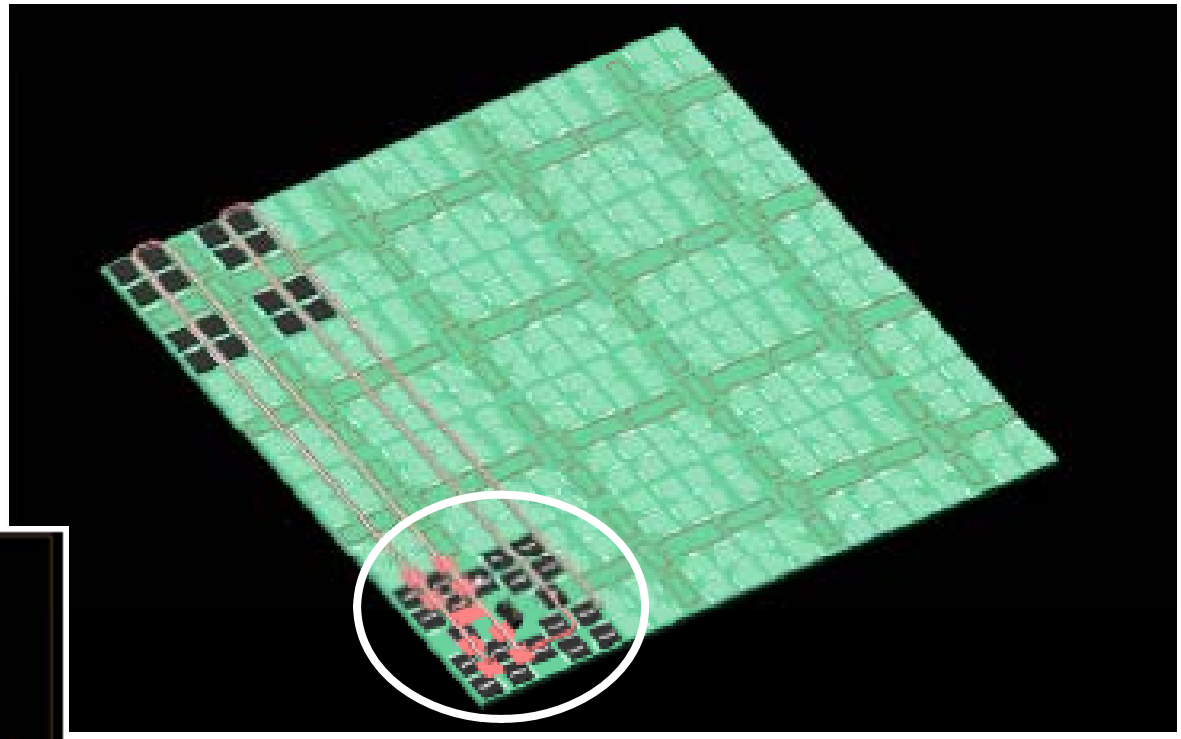
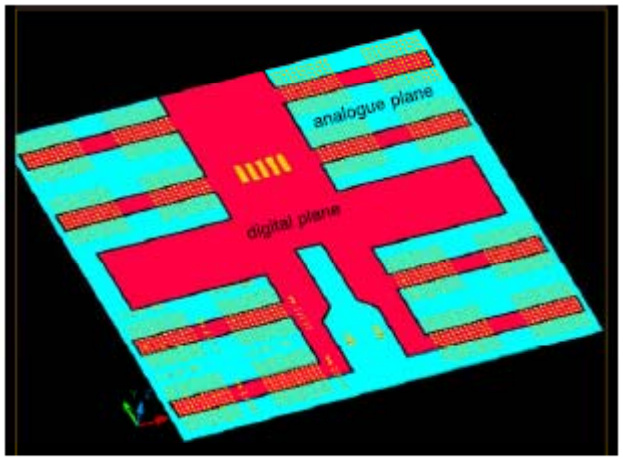
PCB Structure

PCB dummy as similar to real design as possible.

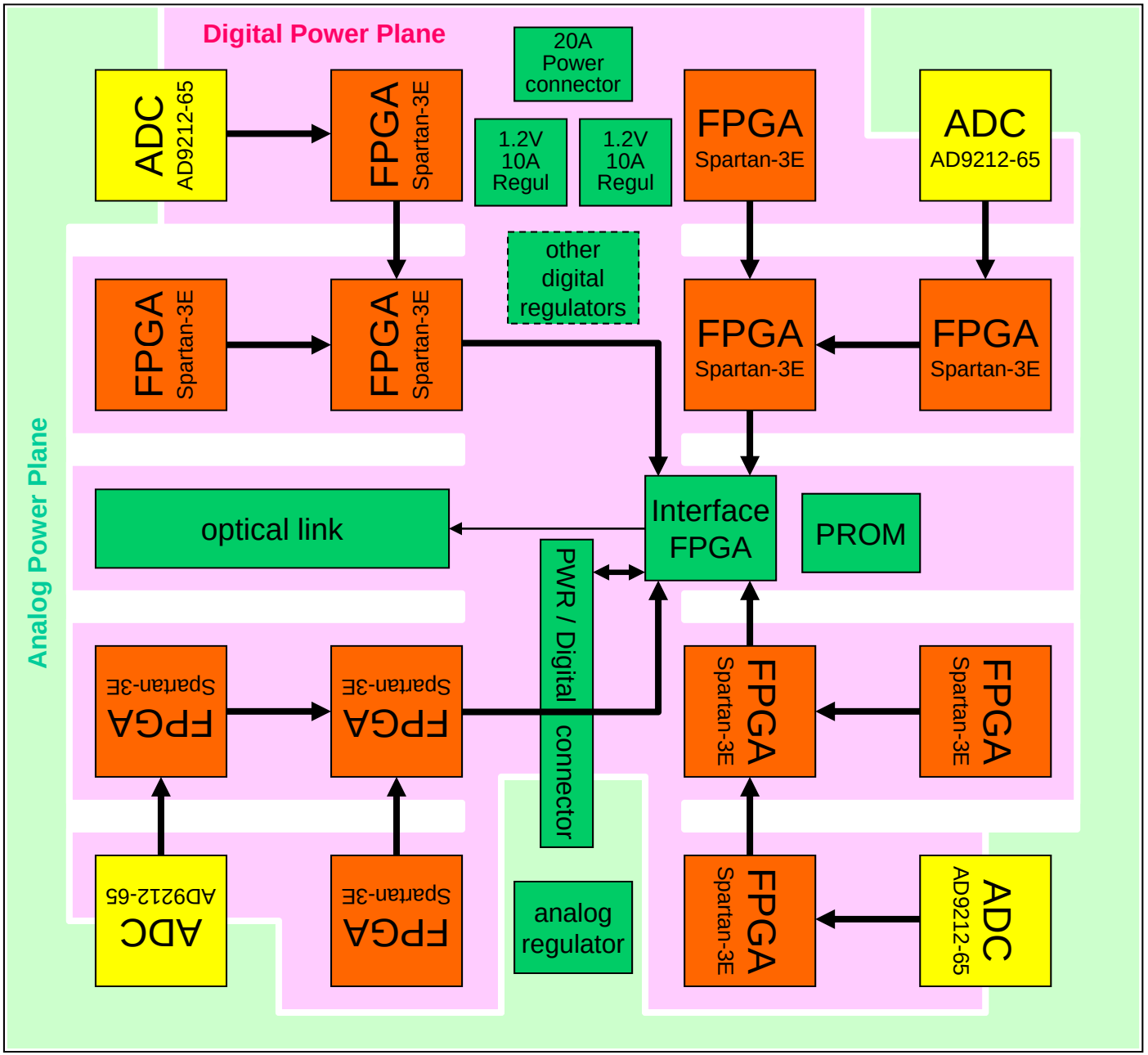




Power plane structure of one module

1 PCB = 16 modules
1 module = 16 S-ALTRO chips

One Module Layout Idea (Original)



Discussions - Regulators

Original Idea:

With SALTRO, peak current per module (16 chips) will be about 50A(25A) at 40Msps (10Msps). Maximum current of obtainable commercial regulator is 10A. The proposed dummy board design has two 10A regulators.

Discussions:

Better to come close to real current.

Conclusion:

Try to mount four 10A regulators (40A in total), i.e., one regulators per three FPGAs, though need to consult layout design company for possibility.

→ Layout designer said it's impossible. Therefore we will put two 10A regulators per module.

Discussions – Power Cycling

Original Idea:
Turn On/Off clock for FPGA because turning off FPGA
clears all of the program in it.

Discussions:
If possible, it's better to power on/off FPGA so that we can emulate precisely
for example charge/discharge of decoupling capacitors on power lines.

Conclusion:
Replace FPGA in current design (Xilinx Spartan 3E) with Actel ProASIC3,
which is called Flash FPGA and re-programming after power on is unnecessary.
It's loss of cost because we have already ordered Spartan 3E.
However, we try to go through the best solution.
As a candidate, AGL250V2QNG132 by Actel is obtainable in two weeks
with similar costs, same package size and same number of pins
as the Xilinx Spartan 3E in the current design.

Discussions – Optical Link

Original Idea:

No idea by me to put one optical link per module.
Looking for very small surface-mount optical link.

Discussions:

There is an all-in-one small optical link, but it's under development and will be obtained next year.

Conclusion:

Use commercial link. Luciano recommends HFBR 5720AL by Agilent Technologies. One link per module is too much. One link on one board will be enough.

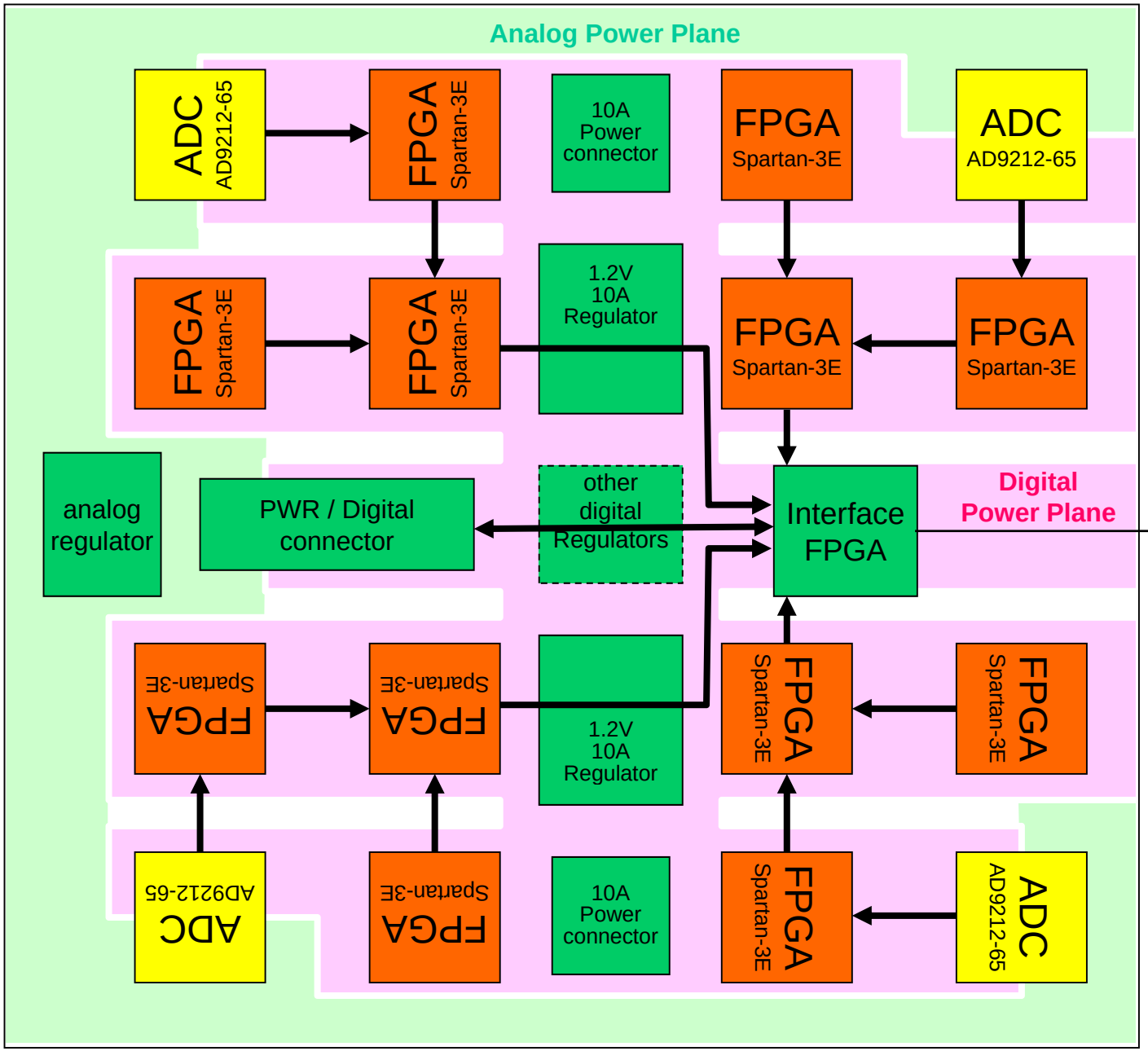
Discussions – ADC

Original Idea:
8 channel high speed ADC (AD9212)

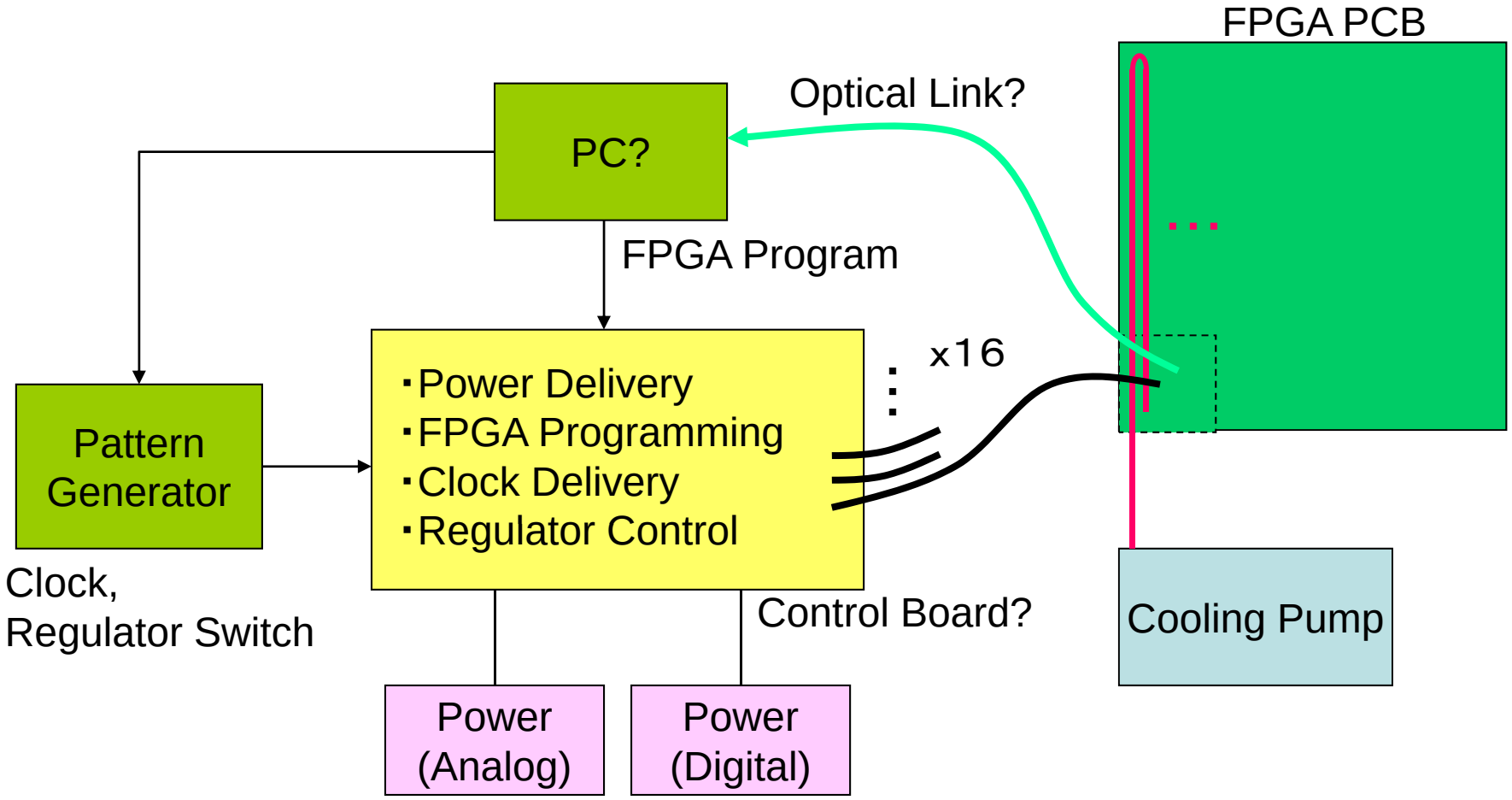
Discussions:
Better to connect Pre-amps (one can measure noise levels with it).

Conclusion:
Put an OPamp (LMP7717) with feedback capacitor and resistor on one channel of the ADC.

One Module Layout Idea (Modified after Discussions)



Test System


FPGA PCB
Optical Link?
PC?
FPGA Program
Pattern Generator
・Power Delivery
・FPGA Programming
・Clock Delivery
・Regulator Control
x16
Clock,
Regulator Switch
Control Board?
Cooling Pump
Power (Analog)
Power (Digital)