Beam Tests in 2010-2011

A realistic approach?

LC TPC WP meeting
mostly dedicated to WP5 discussions

4 March, 2010

Takeshi MATSUDA
DESY / FLC

R&D Phases

1. **Demonstration Phase**: Small prototype tests still going!

   Provide a basic evaluation of the properties of an MPGD TPC and demonstrate that the requirement (1-b,c) can be met using small prototypes.

1. **Consolidation Phase**: LP1: 2007-2010 & LP2 2010 –

   Design, build and operate a "Large Prototype" (of large number of measured points) at the EUDET facility in DESY comparing tecnologies and demonstrating (1-a) in a way.

1. **Design Phase**:

   Start working on an engineering design for aspects of the TPC at ILC.

   (LC TPC collaboration: MOU)

At each phase, we perform beam tests probably with different purposes.

Options of MPGD for ILC TPC

Based on the studies with small MPGD TPC Prototypes

Analog TPC: Immediate options for the current ILC schedule

(1) Multi layer GEM + Narrow (1mm wide) pad readout:

- **Defocusing by multilayer GEM**
- **Narrow (1mm) pads → S-ALTRO meets with 4mm**2 pads.**

(2) MicroMEGAS + Resistive anode pad

- **Widening signal by resistive anode**
- **Size of pads (wider → minimum?)**
- **Adopting S-ALTRO**

(3) Multilayer GEM + Timepix:

- **small pixel → need to improve the efficiency for primary electrons**
- **larger pixel → more like an analog TPC with much smaller pads**

Digital TPC: Still many hardware issues:

(4) Ingrid-MicroMEGAS + Timepix:

- **Digital → Free from the gas gain fluctuation**
  - **More information from primary electrons**
  - **30 % improvement in position resolution (?)**
  - **(to be demonstrated)**

TPC Large Prototype Beam Test (LP1)

LP1 at DESY T24-1 beam area

TPC Large Prototype Tests: LP1

Klaus Dehmelt

2008:	
Nov-Dec	MicroMEGAS modles w/ resistive anode (T2K electronics)
2009:	
Feb-Apr	3 Asian GEM Modules w/o Gating GEM (3,000ch ALTRO electronics)
Apr	TDC electronics with an Asian GEM Module
Apr-May	Maintenance of PCMAG
May-Jun	Micromegas w/ two different resistive anodes (New T2K electronics)
	Setup and test of laser–cathode calibration
Jun	GEM+Timepix (Bonn)
Jun	Installation of PCMAG lifting stage and Si support structure
July	TDC electronics with an Asian GEM module
	ALTRO electronics study w/ an Asian GEM module
July-Aug	Installation of PCMAG lifting stage
Aug	MicroMegas w/o resistive anode with laser-cathode calibration
Sept	A Bonn GEM module (A small aria GEM with ALTRO electronics)
Nov.	A preliminary test of the silicon emvelope with a MicroMegas module.
Dec.	Test of new MicroMEGAS modules with new reistive anode.

2010: (see next page)

TPC Large Prototype Beam Test: LP1 in 2010

"Demonstrate full-volume trucking in non-uniform magnetic field, trying to provide a proof for the momentum resolution at LC TPC"

2010:

spring/summer

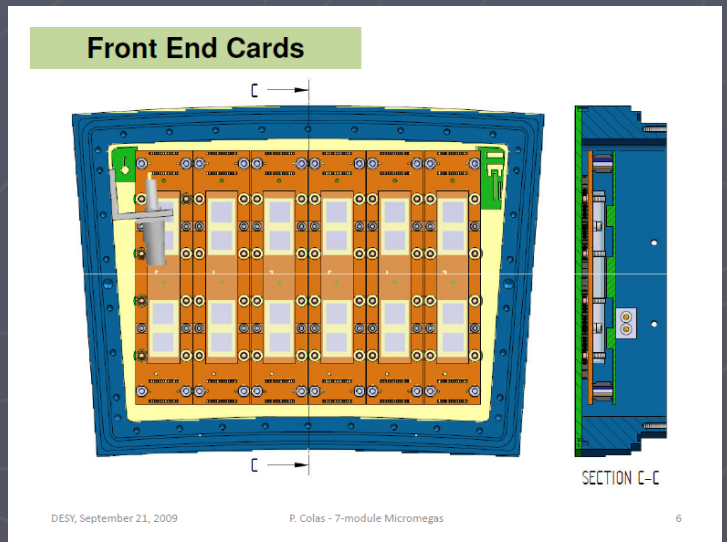
4 Asian GEM Modules w/ gating GEM (10,000ch ALTRO electronics)

DESY GEM modules (w/ gating devices?) (ALTRO electronics)

fall /winter 7 MicroMEGAS modules w/ resistive anode

(12,000ch T2K electronics)

New MicroMEGAS modules in 2010



Two Other Important R&D Issues in 2010-2012

Advanced endplate:

Requirement: thickness 15% Xo

Thin endplate
High density, low power electronics S-ALTRO
to match with the small pad size (4mm**2) surface-mounted directly on the back of pad plane of MPGD detector module
Power delivery, power pulsing and cooling

Ion Feed back and Ion disks: Gating Device

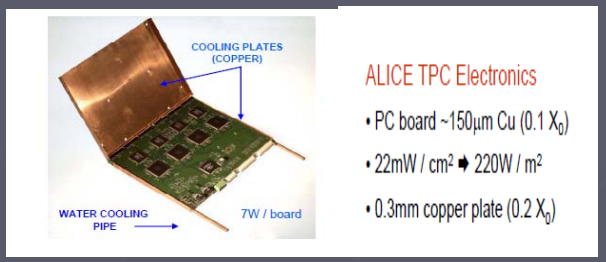
Ion feed back ration and beam backgrounds

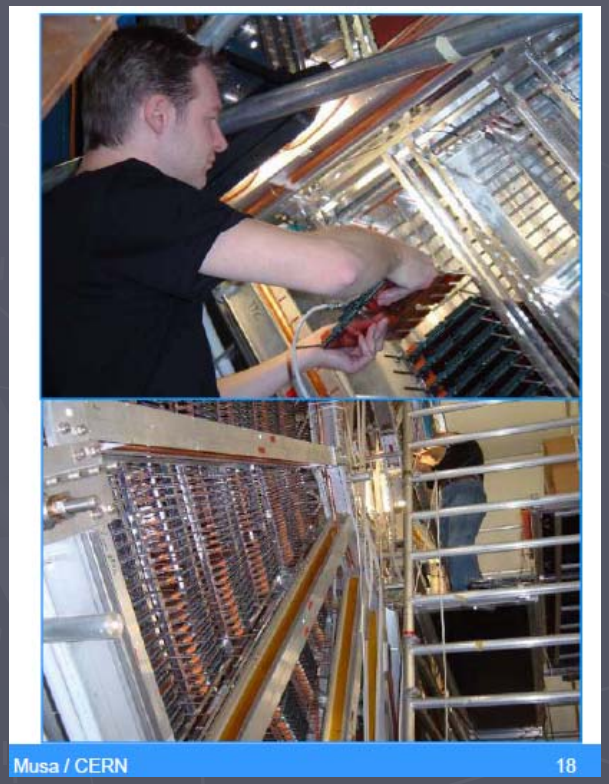
Estimate distortion due to the ion disks (simulation)
Options of gating device: Wire gating, GEM gating
Methods of calibration

S-ALTRO Team
LC TPC collbaoration

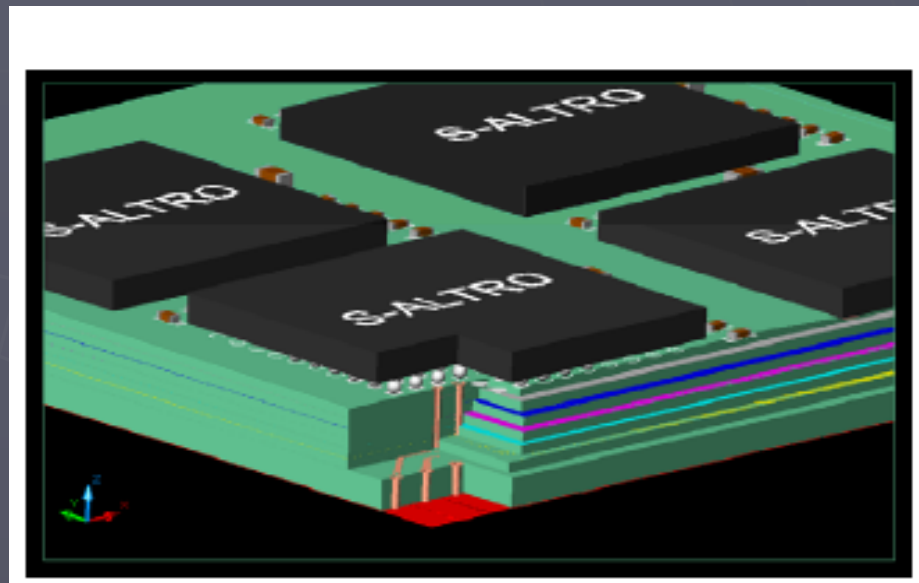
Advanced Endplate: S-ALTRO

High density, low power , low material electronics for TPC





ALICE TPC



The S-ALTRO team at CERN

P. Aspell, H. Franca Santos, E. Garcia,
A. Junique, M. Mager, C. Patauner,
A. Ur Rehman, L. Musa

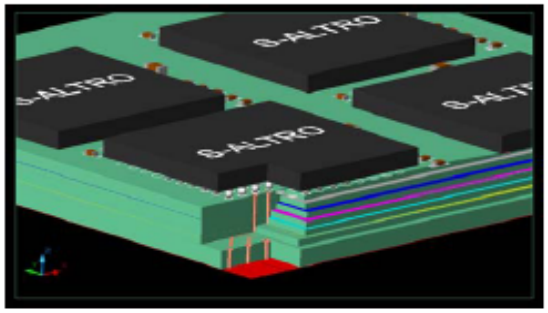
ILC (ILD) TPC

Advanced Endplate: S-ALTRO

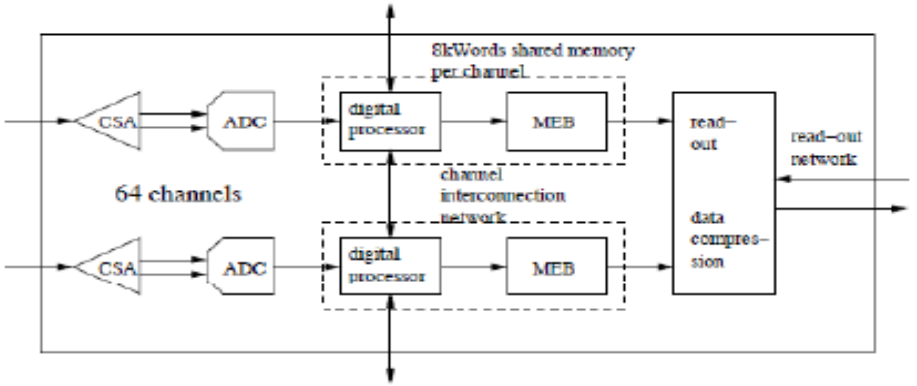
High density, low power electronics for TPC

A multi purpose readout chip for TPC detectors

A multi-purpose readout chip for TPC detectors



- 64 complete readout channels (from detector pad to data link)
- programmable charge sensitive amplifier
  - sensitivity to a charge in the range ~10^2 - ~10^6
  - programmable shaping time in the range 30 to 300ns
- 10-bit 40 MSPS ADCs
- 8k multi acquisition memory per channel (dynamically allocated)
- digital signal conditioning (4th order IIR filter and FIR filter) for baseline correction
- 3-D zero suppression
- lossless data compression
- readout net work controller
- output bandwidth 160 Mbyte/sec



Advanced Endplate: S-ALTRO

L. Musa

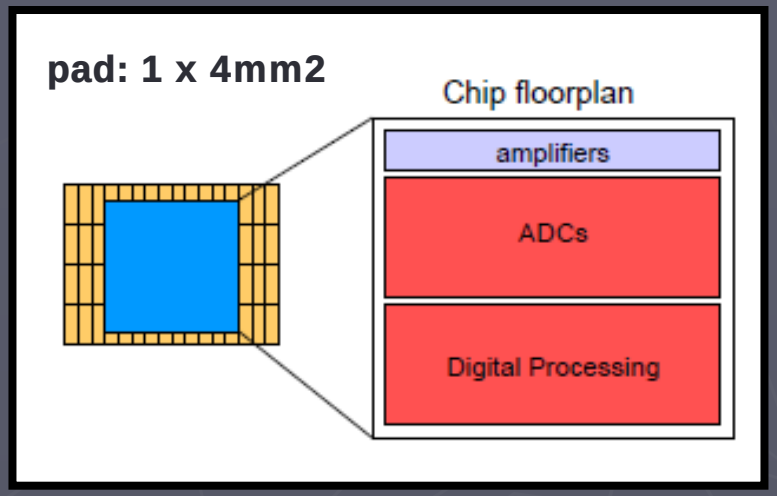
Chip size and Power consumption

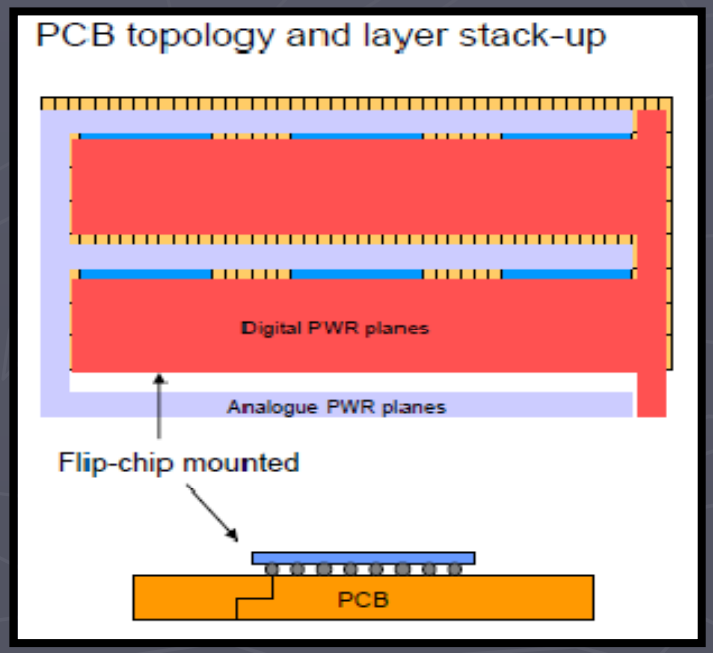
Chip size: (*estimate)

- Shaping amplifier 0.2 mm²
- ADC 0.7 mm² (*)
- Digital processor 0.6 mm² (*)
- When 1.5mm²/channel
  - 64 ch/chip ➡ ~ 100 mm²
- PCB board ~ 27 x 27 cm²
  - ⇨ ~16400 pads or 256 chips/board
- Bare die flip-chip mounted or chip scale package
- Minimum-size capacitors (0.6x0.3x0.3mm3)
- Standard linear voltage regulators
- Data link based on ALICE SPD GOL MCM

Power consumption: (*) 10 -40MHz

Amplifier	8 mW/channel
ADC	12-34 mW/channel (*)
Digital Proc	4 mW/channel
Power reg.	2 mW/channel
Data links	2 mW/channel
Power reg. eff.	75%
Total	32-60mW/channel (*)
Duty cycle:	1.5% (Electrical duty)
Average power	0.5 mW / channel
	100 -200W/m2 (*)





Advanced Endplate: S-ALTRO

Status and Schedule

Status & Plans

Status

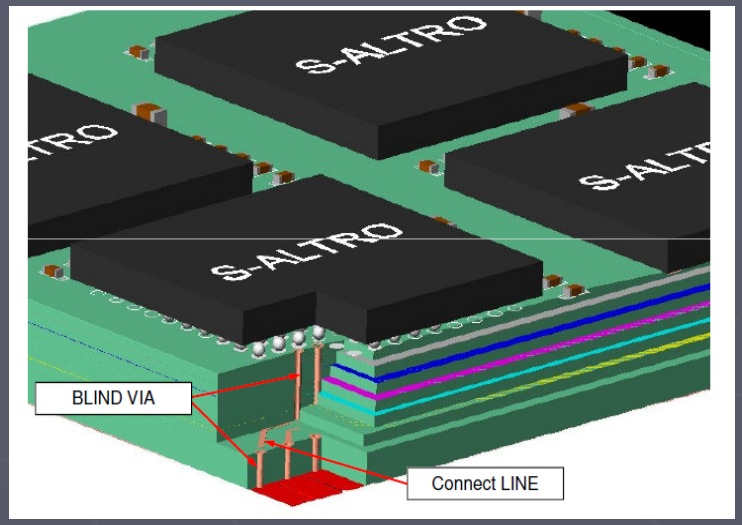
- 2006 12-channel prototype of CSA (no programmability)
- 2007 16-channel prototype programmable (1000 chips for LPTPC @ Desy)
- 2009 2-channel ADC prototype (samples expected in June)
- 08/09 specifications digital blocks and design entry (Verilog) of data processor
- 2009 first design of readout board

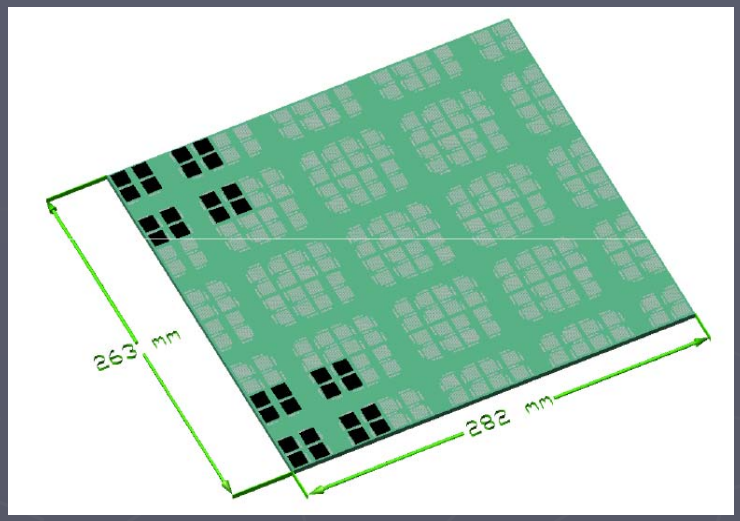
Plans

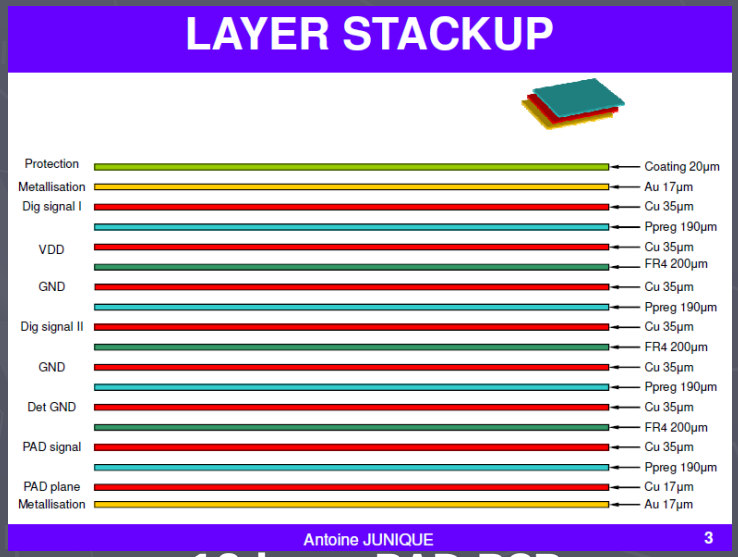
- 2009
  - characterization of ADC samples (Jul – Aug)
  - optimization of ADC design or ADC IP (S3) and migration to IBM 130nm
  - design of 16-channel of complete readout chain (with simplified digital processor)
- 2010
  - characterization of 16-channel prototype
  - decide how to continue the project according to the results achieved

Advanced Endplate: S-ALTRO

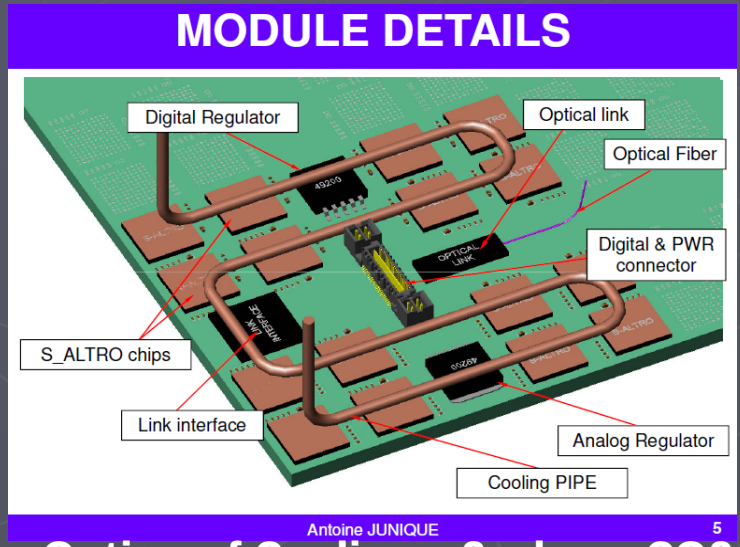
Design of Pad Board







18 layer PAD PCB

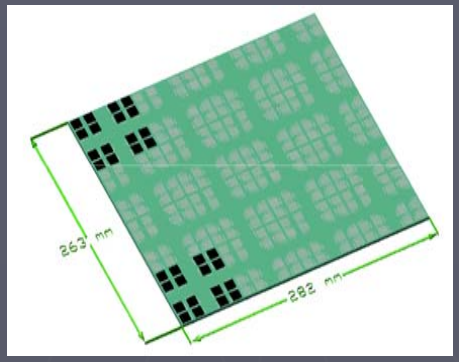


Option of Cooling: 2-phase CO_2 cooling / traditional H_2O cooling

Advanced Endplate: PCB Test

Test with a Pad PCB model

S-ALTRO Team
LC TPC groups



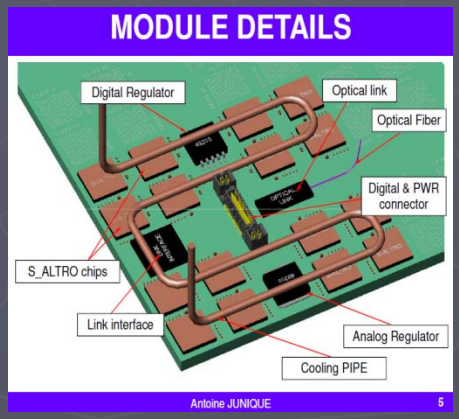
Test:

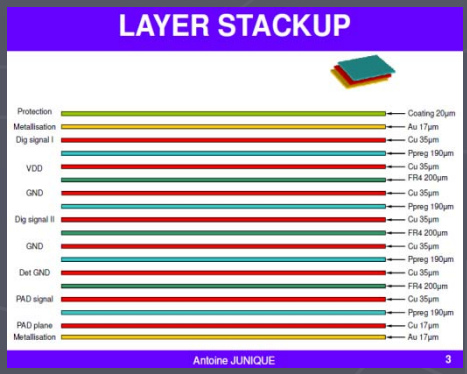
Power switching
Power delivery
Cooling:
Thermo-mechanical feature
In a high field (DESY 5T magnet, PCMAG, etc.)

Pad PCB model:

Realistic design of pad PCB with all components
64ch S-ALTROs replaced by proper FPGAs and
OP amp/ADC as current load and heat source.
Connect pads to the FPGA analog outputs
Try cooling by the 2-phase CO2 cooling
(AMS and LHCB: Bart Verlaat/Nikhef)
Test also digital software model/communication in FPGA
Test in high magnetic field

Schedule: 2010





Advanced Endplate: Cooling

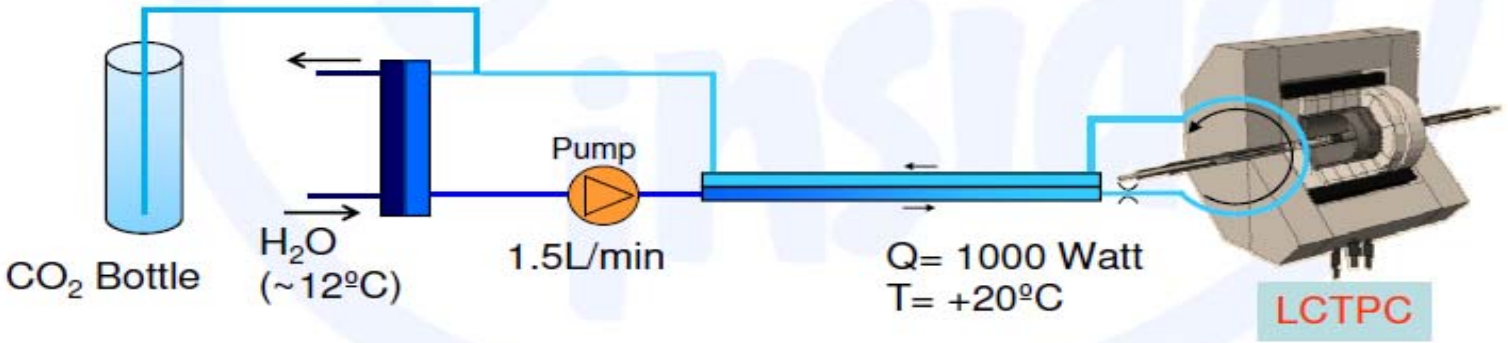
Option of the 2-phase CO2 cooling

2PACL for LCTPC

Warm 2PACL very simple

- Accumulator is CO_2 bottle @ room temperature
- Cold source is cold water

Bottle temperature = Detector temperature



AMS-TTCS was tested in the same way

(Cold test done with bottle outside in winter)

18

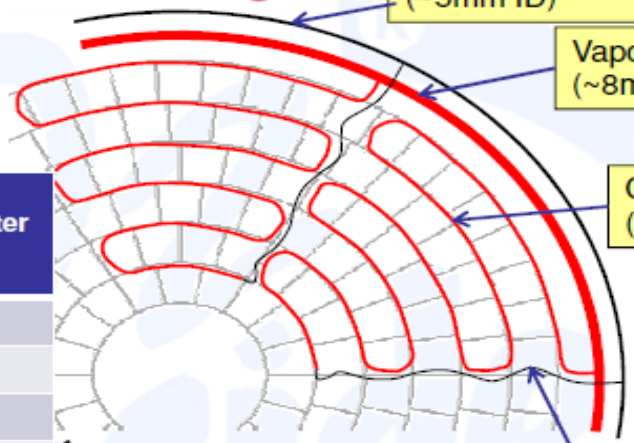
Applied to AMS and LHCb

Advanced Endplate: Cooling

Preliminary Design Consideration for ILC TPC
Advantage of thin piping (high pressure)

TPC end plate cooling tube routing

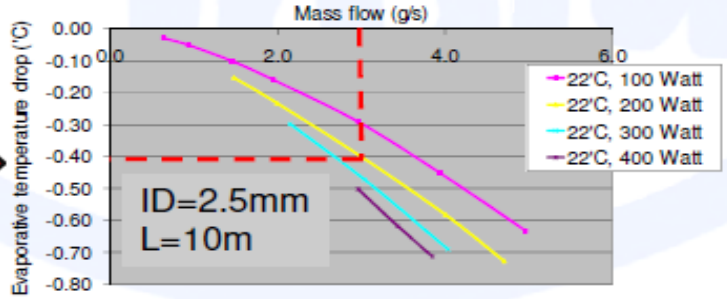
Possible layout of the 6 loops option



	Qty Frames / loop	Heat load per loop (W)	Tube length (m)	Inner diameter (mm)
1 loop	200	1000	48m	6.2
2 loops	100	500	24m	4.3
4 loops	50	250	12m	3
6 loops	34	171	8m	2.2

Similar to AMS-TTCS

AMS test data (2001)
0.4ºC temperature gradient



16

TPC Large Prototype Beam Test (LP2) in 2011-2012

Most realistic to stay at DESY

2011 Some remaining tests from 2010?

Modification of PCMAG (6months) for “Liq. He less” operation (funded by AIDA and else)

2012- Tests of “Advanced Endplate (at least modules)”

Continue testing modules with Time pix

with the current LP TPC with PCMAG at DESY

With options of:

Some dedicated tests in a higher magnetic field

Some dedicated tests with a hadron beam

Because of:

Time/limited

Availability of hadron test beam/unclear (in 2011)

Funding for moving LP TPC/not foreseen

Still possible to measure momentum precisely

We do not need the (I)LC time structure of beam for test(?)