CHERWELL: *TOWARDS INTELLIGENT TRACKERS*

Joel Goldstein
The University of Bristol
For the SPiDeR Collaboration
LC 2010

Ideal Trackers

Ideal Trackers

* Fast

Ideal Trackers

SPiDeR

* Fast
* High precision

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Silicon

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* High granularity

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* High signal-to-noise

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→ Silicon

→ Pixels

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SPiDeR

* Fast
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* High signal-to-noise
* Low cost

Silicon

Pixels

Ideal Trackers

SPiDeR

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* High precision
* High granularity
* High signal-to-noise
* Low cost
* Low mass

Silicon

Pixels

Ideal Trackers

SPiDeR

- Fast
- High precision

→ Silicon

- High granularity
- High signal-to-noise

→ Pixels

- Low cost
- Low mass

→ Monolithic CMOS

Ideal Trackers

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- High granularity
- High signal-to-noise
- Low cost
- Low mass
  - *(Minimal dead area)*

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→ Pixels

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→ 100% fill factor

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→ Intelligent

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→ Pulsed power/rolling shutter

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- Radiation hard

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→ Silicon

→ Pixels

→ Monolithic CMOS

→ 100% fill factor

→ Intelligent

→ Pulsed power/rolling shutter

→ Fast charge collection

Intelligent CMOS

SPiDeR

- Similar requirements for vertexing and calorimetry
- Family of monolithic CMOS pixel sensors
  - In-pixel intelligence
  - Distributed processing
    - Minimal dead space
    - Flexibility for different applications
- Other features:
  - Full depletion
  - Pulsed power
  - Large area

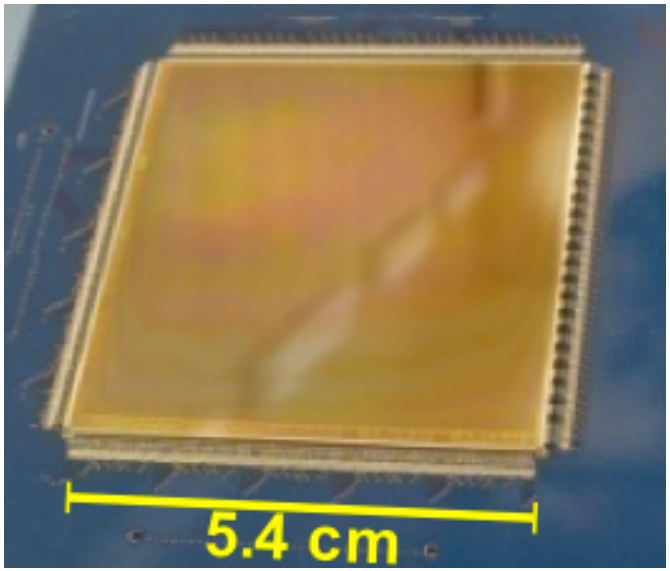
SPiDeR

SPiDeR

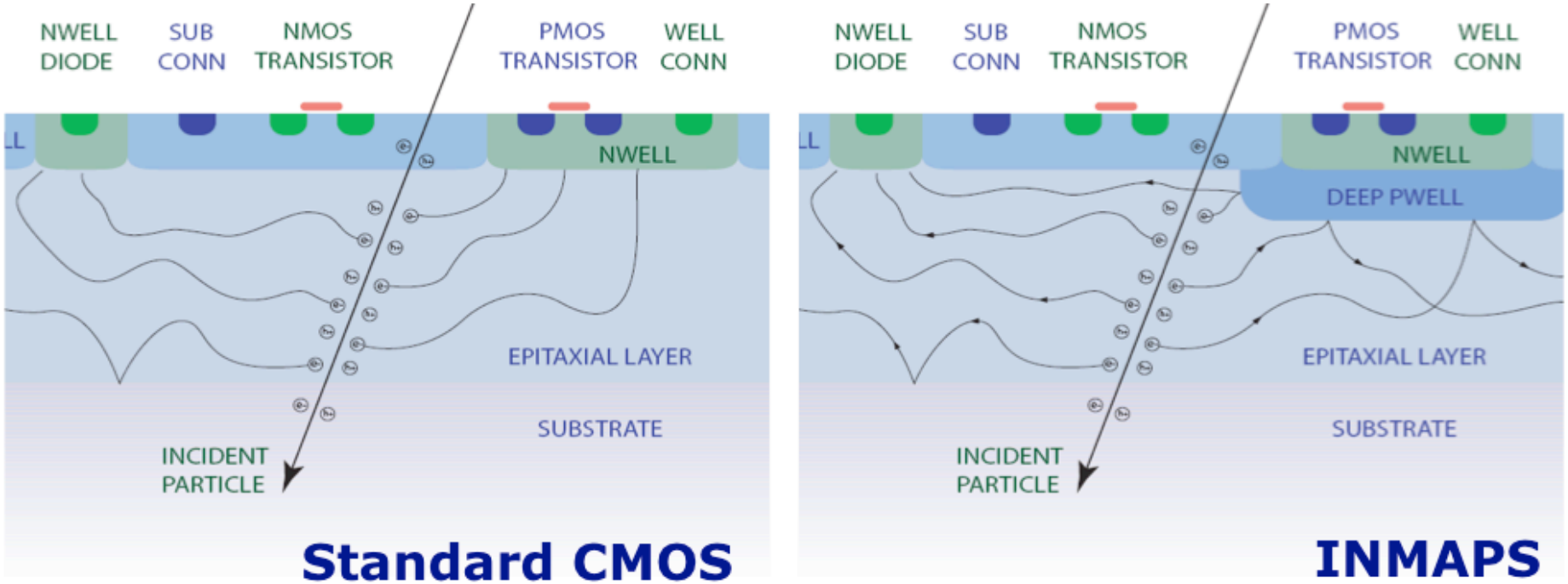
- **Develop CMOS imaging technology for particle physics**
- UK-based collaboration
- Birmingham, Bristol, Imperial, QMUL, Oxford
- STFC-RAL Particle Physics and Engineering
  - CALICE and LCFI experience
  - RAL Microelectronics group

Technology

- RAL have "INMAPS" process available
- Standard CMOS with added....
  - Deep p-well
  - 4T pixels
  - High resistivity epitaxial layer
    - Up to ~10 kΩ cm
  - Stitching
    - e.g. RAL-designed LAS

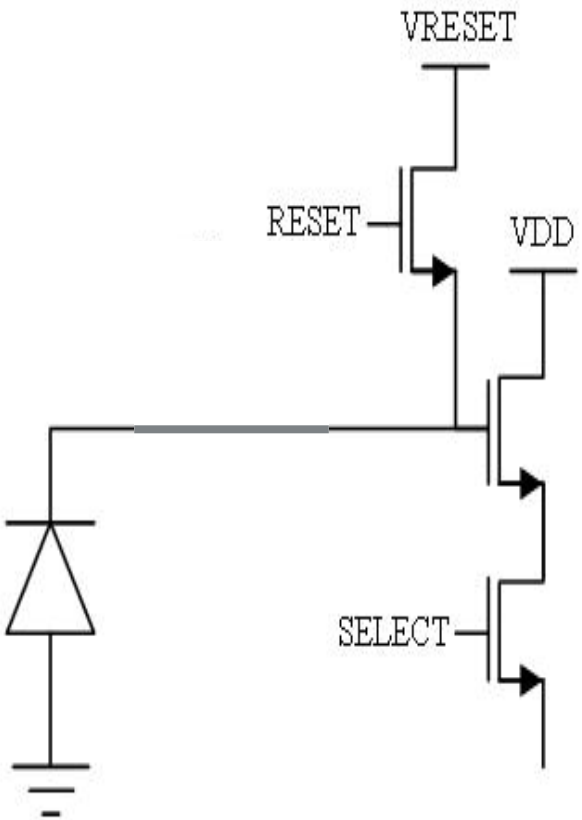


Deep p-well



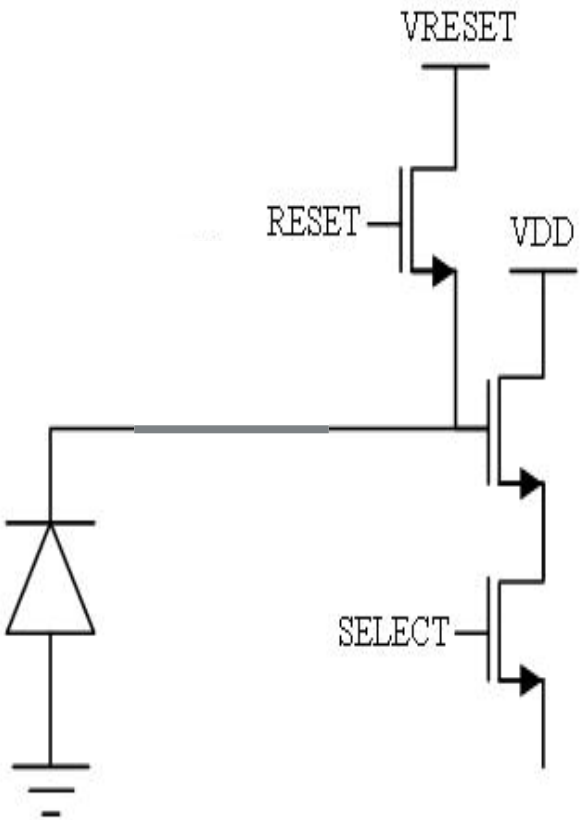
- Eliminates charge collection by n-well
- Enables full CMOS capability

4T Pixel



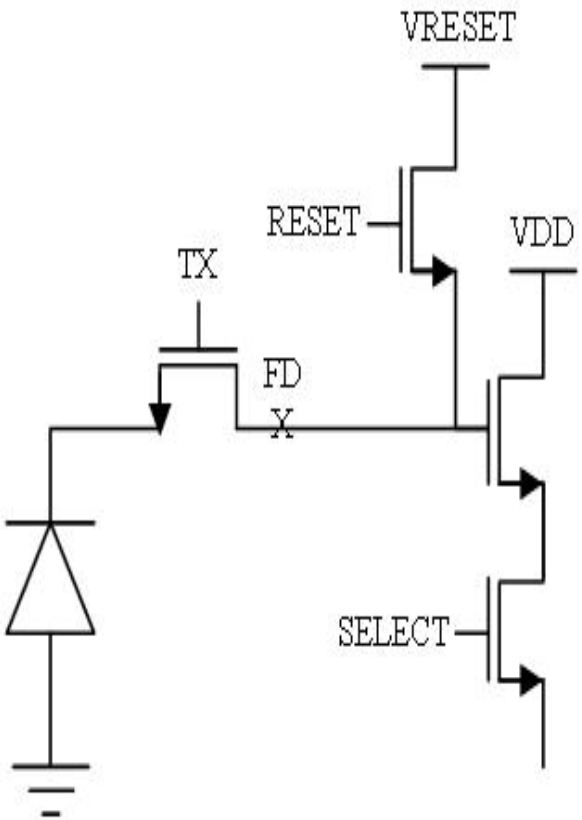
* Traditional "3T" circuit

4T Pixel



- Traditional "3T" circuit
- Additional "transfer" gate

4T Pixel



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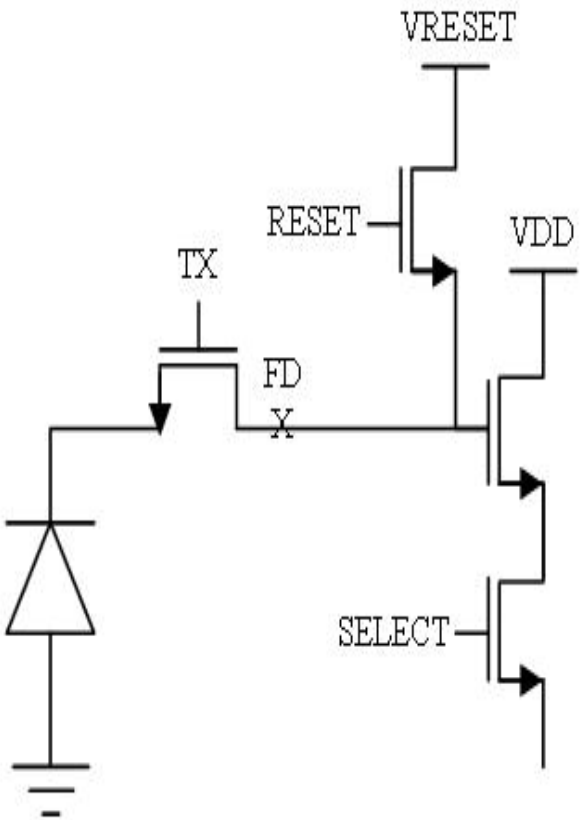
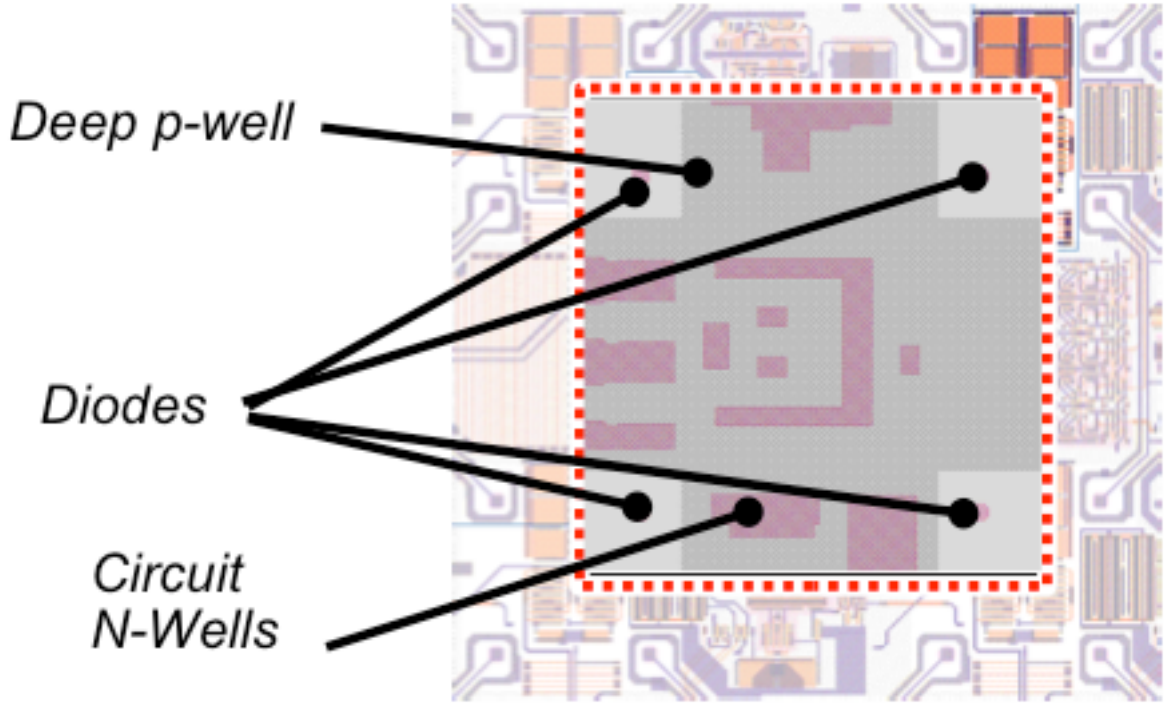


- Traditional "3T" circuit
- Additional "transfer" gate
- Separate amplifier from detector
- Allows CDS
- Gate much smaller than diode:
  - Increase gain
  - Decrease noise

TPAC

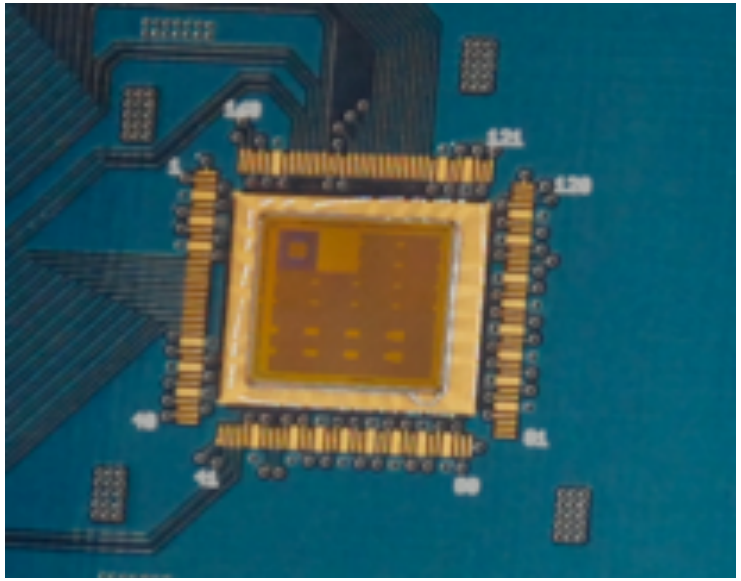
SPiDeR

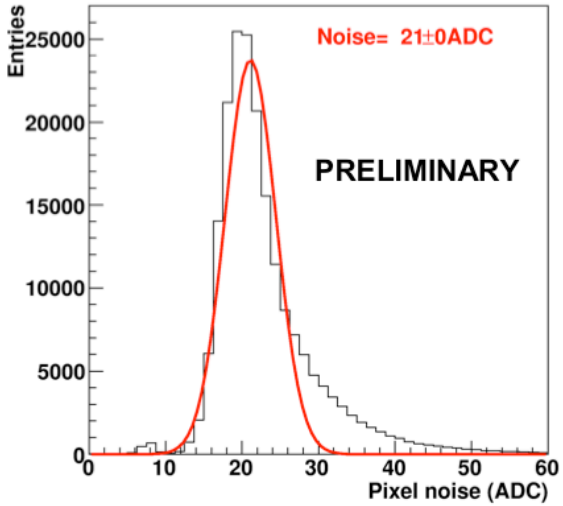
- Inherited from CALICE
- Digital calorimetry
- 50μm×50μm
- Pixel contains
  - 4 diodes
  - Discriminator
- Proof of deep p-well

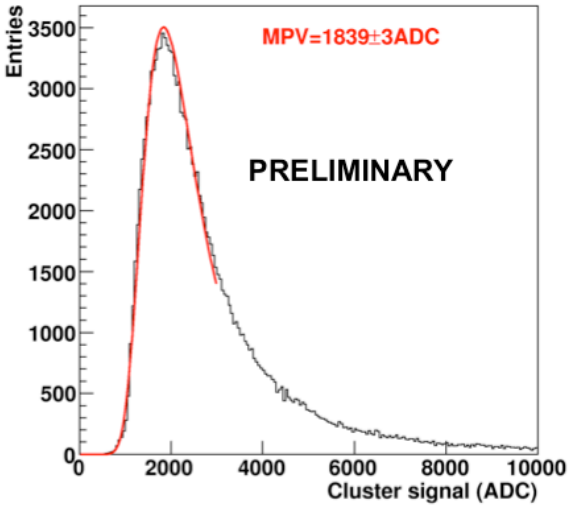


FORTIS

- Inherited from RAL CfI
- 4T demonstrator
- Rolling shutter
- Many variants (high-res)
- Signal-to-noise ~ 100:1

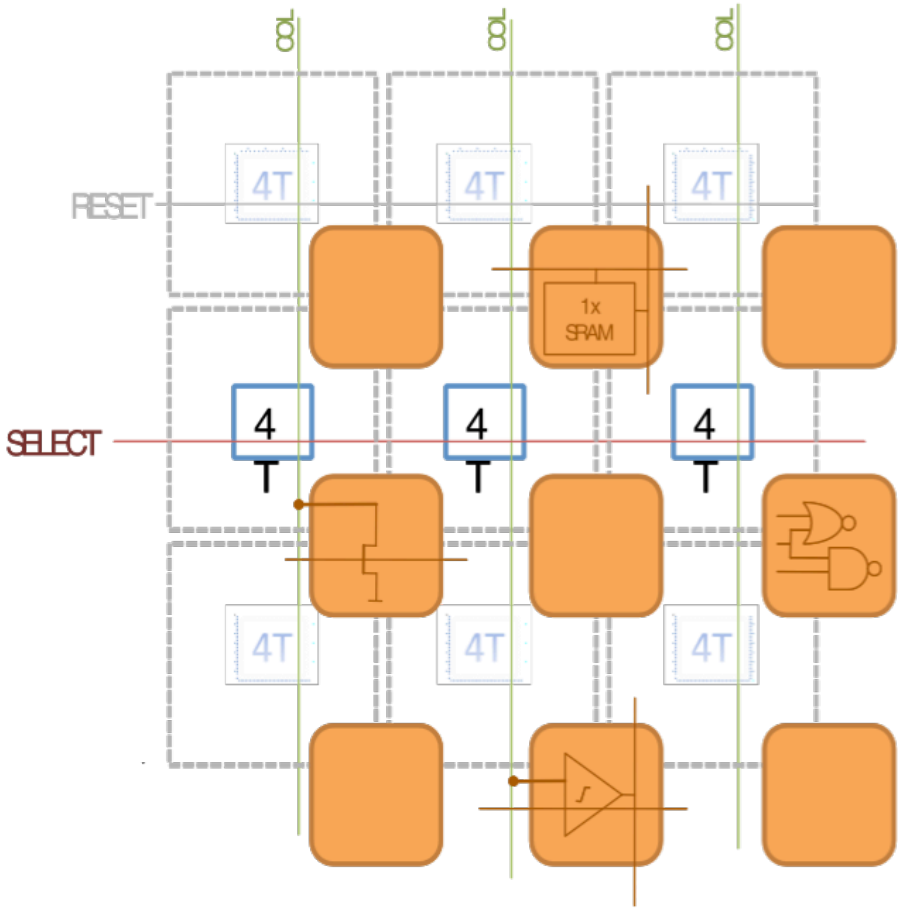




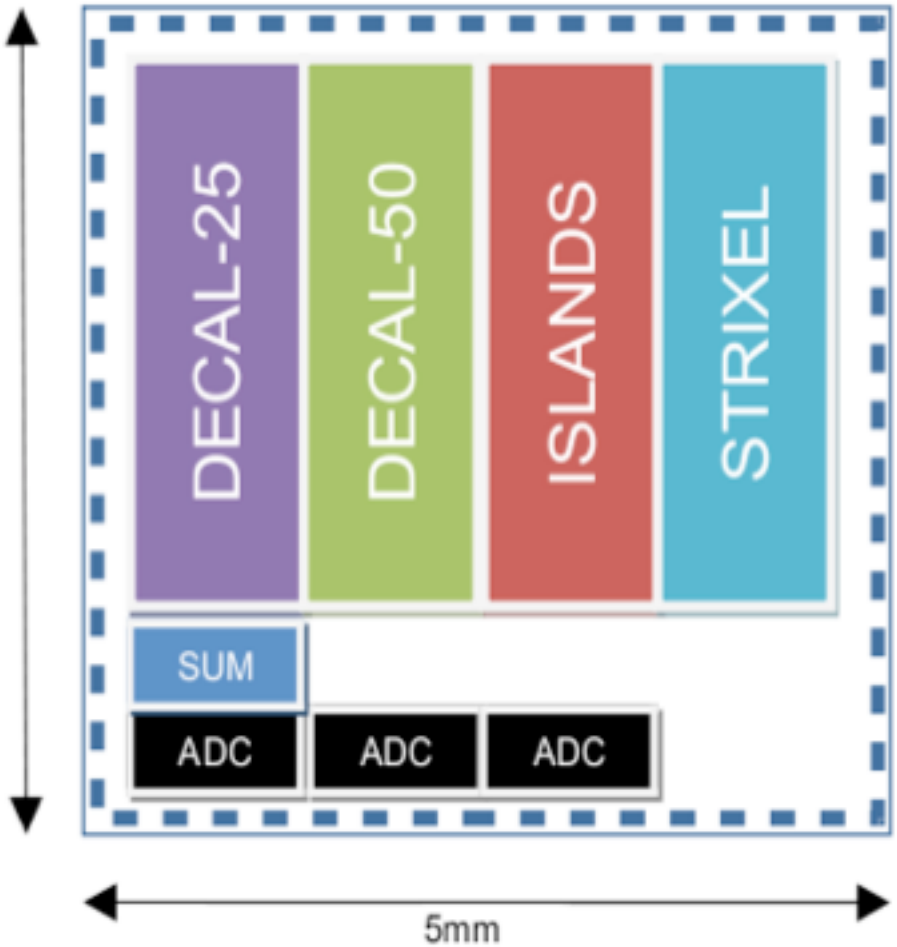


Cherwell

- Combine TPAC + FORTIS
  - Deep p-well
  - 4T pixels
  - High-res epi
- "Islands" hold CMOS
- Can distribute/share
  - Memory
  - Logic
  - ADC
  - ....



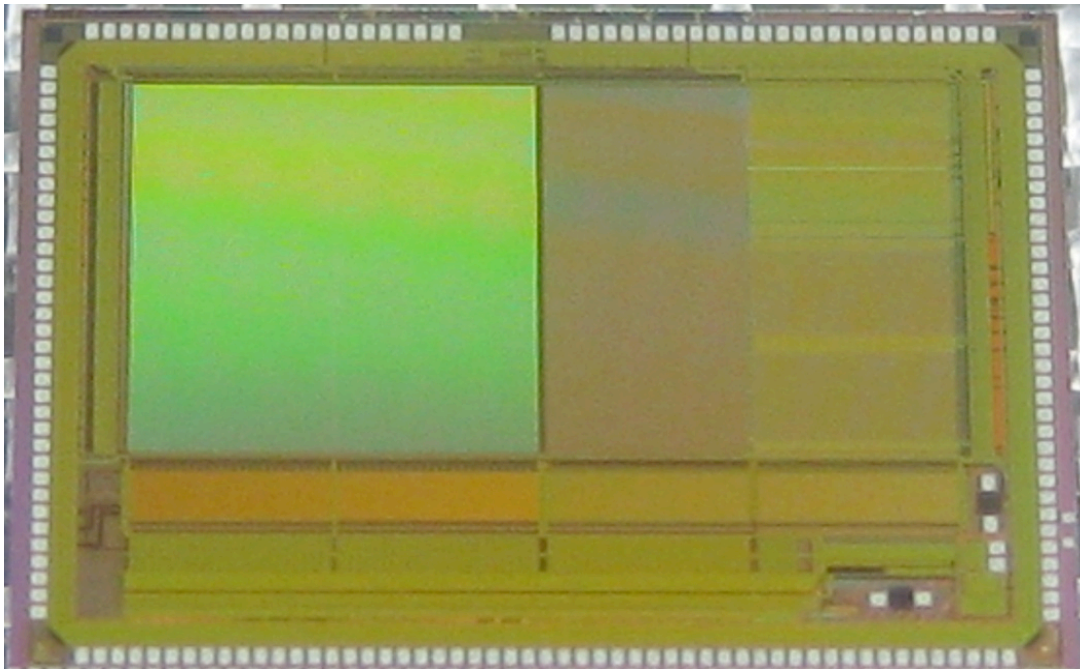
Cherwell-1

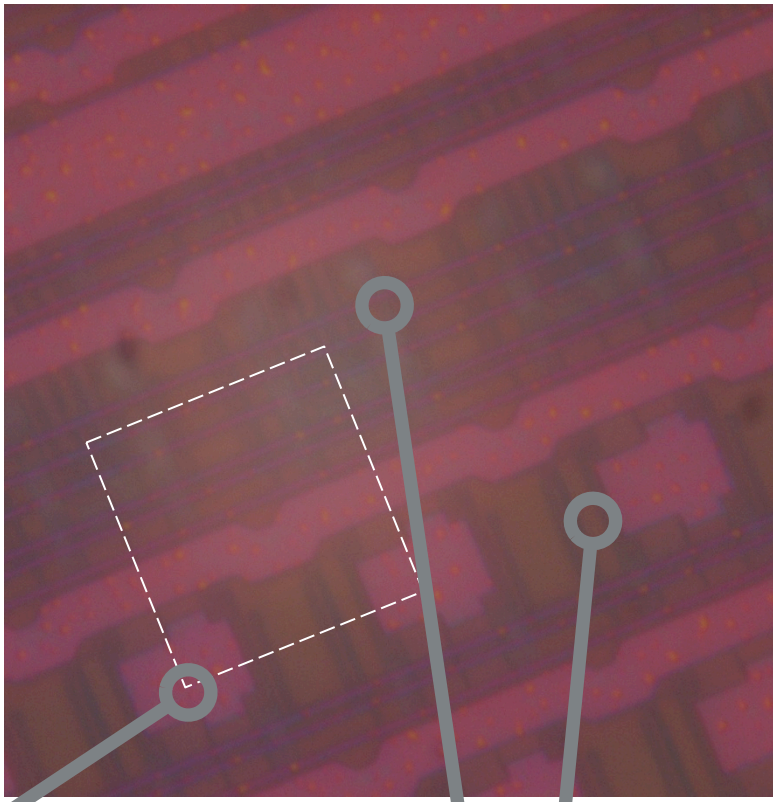


- Proof of concept
- 5mm×5mm total area
- 2 types of calorimetry pixels
- Deep p-well islands
- ADC distributed among pixels

Chips

Cherwell-1 currently awaiting testing





Pixel Boundary

ADC Structures

Status

- SPiDeR approved in December 2008
  - Funding withheld pending UK programmatic review
  - Cut in Spring 2010
- CHERWELL-1 fabricated, awaiting testing
  - Test board design by V. Rajovic, *Belgrade*
- Two SPiDeR CERN test beams in 2010 (*thanks EUDET*)
- Some testing effort available for CHERWELL-1
- CHERWELL-2 large area prototype strixel chip planned
  - Timescale uncertain

Summary

- CMOS pixel sensors have great HEP potential
  - Low mass, high performance trackers
  - Vertexing, calorimetry
- CHERWELL concept
  - Deep p-well, 4T, high-res, stitching....
  - Distributed intelligence in active pixels
  - CHERWELL-2 prototype tracker sensor

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- **Full speed when funding returns...**