A Silicon Pixel Tracker (SPT) for ILC/CLIC

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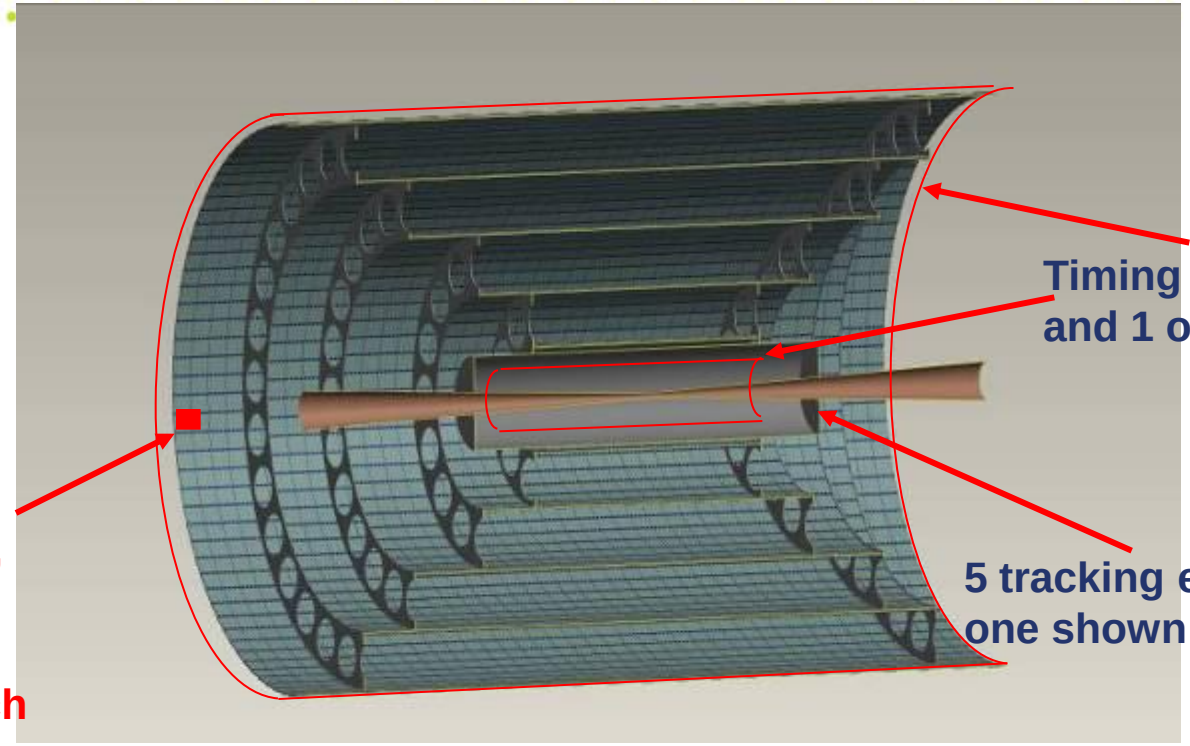
CONTENTS

- **SPT was first presented by Konstantin Stefanov at Sendai LC workshop in March 2008. KS was made redundant by STFC shortly afterwards, but internationally, interest in the SPT has grown steadily**
- **Brief reminder of design concept**
- **Mechanical simulations by Steve Watson at RAL establish the robustness of the very simple non-demountable design concept**
- **Feasibility – new results with charge-coupled CMOS pixels from Jim Janesick (California) and Dave Burt (e2V, Chelmsford) working with Jazz/Tower Semiconductors**
- **First overall performance simulations coming soon – Norm Graf at SLAC**
- **This work has found an intellectually stimulating home within the SiLC collaboration – participation of Aurore Savoy-Navarro and colleagues is much appreciated. They are doing a great job of keeping alive 'alternatives' in the field of LC tracking detectors**

Overview of Design Concept

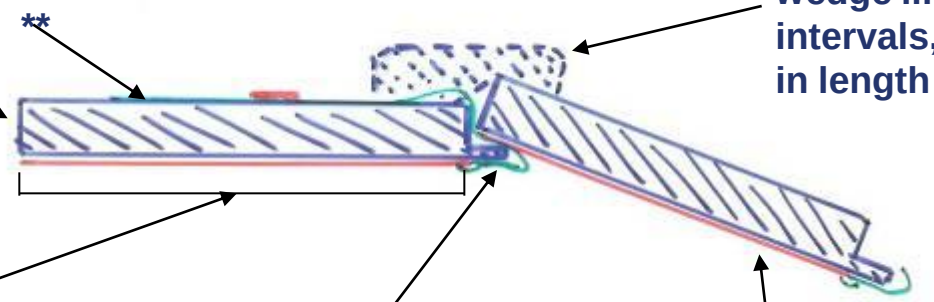
- **Basic goal is to devise a tracker design which significantly reduces the material budget**
- **Thin monolithic *charge-coupled CMOS pixel* devices look promising**
- **The largest pixel tracking system in HEP (the SLD vertex detector with 307 Mpixels) used CCDs. Charge-coupled CMOS pixels have evolved from this technology, achieving much higher functionality by in-pixel and chip-edge signal processing**
- **Basic concept is a 'separated function' design – precision timing on every track *but not on every point on the track.* So we suggest an optimised mix of tracking layers and timing layers. Optimisation to follow from detailed simulations, not yet done.**
- **Key requirements are timing at the 10 ns level (for CLIC timing layers, we need only 300 ns for ILC) and on-sensor data sparsification (for both timing and tracking layers)**
- **By keeping to the *monolithic planar architecture* (CMOS technology) the systems will be scalable circa 2020 to the level of ~40 Gpixels**
- **Such system size may by then be achieved for more advanced architectures (eg vertical integration). However, on grounds of simplicity and minimal cost, we believe we have an attractive solution …**
- **Regarding the design concept, many thanks to ILC and CLIC colleagues for helpful suggestions**

Possible layout (October 2010)



- **Barrels:** SiC foam ladders, linked mechanically to one another along their length
- **Tracking layers:** 5 closed cylinders (incl endcaps) **~50 μm square pixels**
- ~0.6% X_0 per layer, 3.0% X_0 total, over full polar angle range, plus <1% X_0 from VXD
- **Timing layers:** 3 as an **envelope** for general track finding, and one or two between VXD and tracker, ~1.5% X_0 per layer, evaporative CO_2 cooling **~150 μm square pixels**
- **Matching endcap layers:** 5 tracking and 3 timing (envelope)

End view of two barrel ladders ('spiral' geometry)



** Single layer Cu/kapton stripline with one mesh groundplane runs length of ladder, double layer in region of tabs (~5 mm wide) which contact each sensor.

Single Cu/kapton stripline with one mesh groundplane runs round the end of each barrel, servicing all ladders of that barrel.

Sparsified data transmitted out of detector on optical fibres (1 or 2 fibres per end), continuously between bunch trains

Continuous (not pulsed) power for tracking layers, so minimal cross-section of power lines

Tracking layers cooled by a gentle flow of nitrogen gas, hence no cooling pipes within tracking volume.

Timing layers need pulsed power, evaporative CO_2 cooling, hence thicker

Track reconstruction

- Start with mini-vectors from on-time tracks seen in the outer triplet of timing layers, together with an approximate IP constraint
- Work inwards through each successive tracking layer, refining the track parameters as points are added
- For curlers at polar angles near 90 degrees, timing information from the endcap layers will be less useful; recover by using the relatively short inner timing barrel
- K-shorts, lambdas and photon conversions will be findable, starting from the mini-vectors in the timing layers, omitting the IP constraint and substituting a V^0 constraint.
- Background level (~7000 out-of-time tracks at CLIC at 3 TeV) appears daunting at first sight, but pixel systems can absorb a very high density of background without loss of performance
- General principle, established in vertex detectors in ACCMOR (1980s) and SLD (1990s): fine granularity can to a great extent compensate for coarse timing. Precision time stamping costs power, hence layer thickness, fine granularity need not
- Back-of-envelope calculations look promising (LCWS Warsaw 2008); looking forward to a real simulation from Norm Graf in near future
- If required by simulations, could make system more robust, for example by switching some of the endcap tracking layers to timing, at cost of ~0.9% X_0 per layer.

Main technical challenges

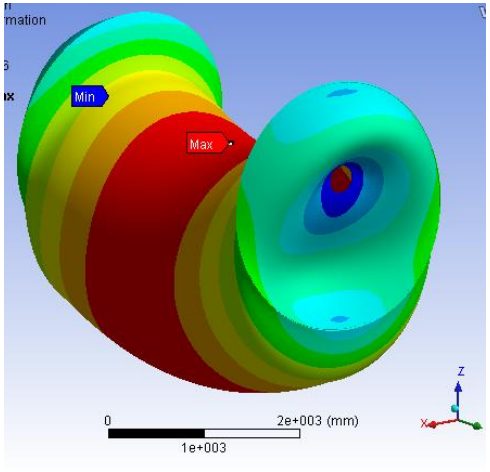
- **Mechanical design – can such large structures be made sufficiently stable?**
- **Overall scale - 33 Gpixels for tracking layers, 5 Gpixels for timing layers. Reasonable, given progress in astronomy etc**
- **Need excellent charge collection efficiency, non-trivial for these relatively large pixels. Can be slow for tracking layers but needs to be fast (<10 ns for CLIC, ~100 ns for ILC) for timing layers**
- **Need few-e^- noise performance, due to small signals from thin layers. Achievable, due to recent advances in charge-coupled CMOS pixel technology – a fast moving area of device physics**

- **Let's consider these issues in turn …**

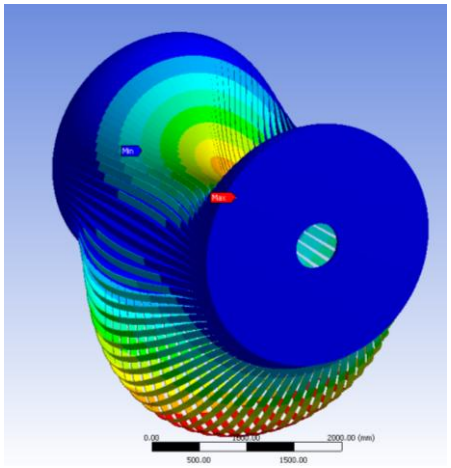
Mechanical structure

- SiC foam favoured wrt ‘conventional’ CFC sandwich, due to:
  - Homogeneous material, ultra-stable wrt temp fluctuations
  - Accurate match of expansions coefficient wrt Si, so bonding of large flexible thinned devices to substrate works well
- But what about the lower elastic modulus of SiC? A structure made of discrete ladders supported at ends would sag unacceptably under gravity
- Idea of non-demountable adhesive-bonded closed half-barrels was devised to minimise material budget (and is justified by long-term reliability of large pixel systems in space and other applications)
- This suggests small foam links between ladders, both in the endcaps and in the barrels.
- Now established with ANSYS that this spectacularly improves the shape stability, almost to the level of a continuous cylindrical structure

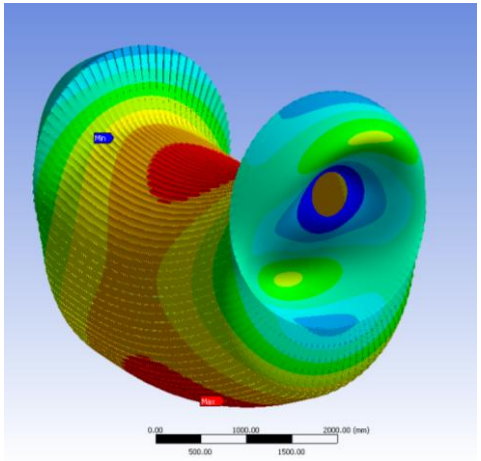
ANSYS simulation of Layer 5



- Continuous foam cylinder
- Max deflection 10 μm



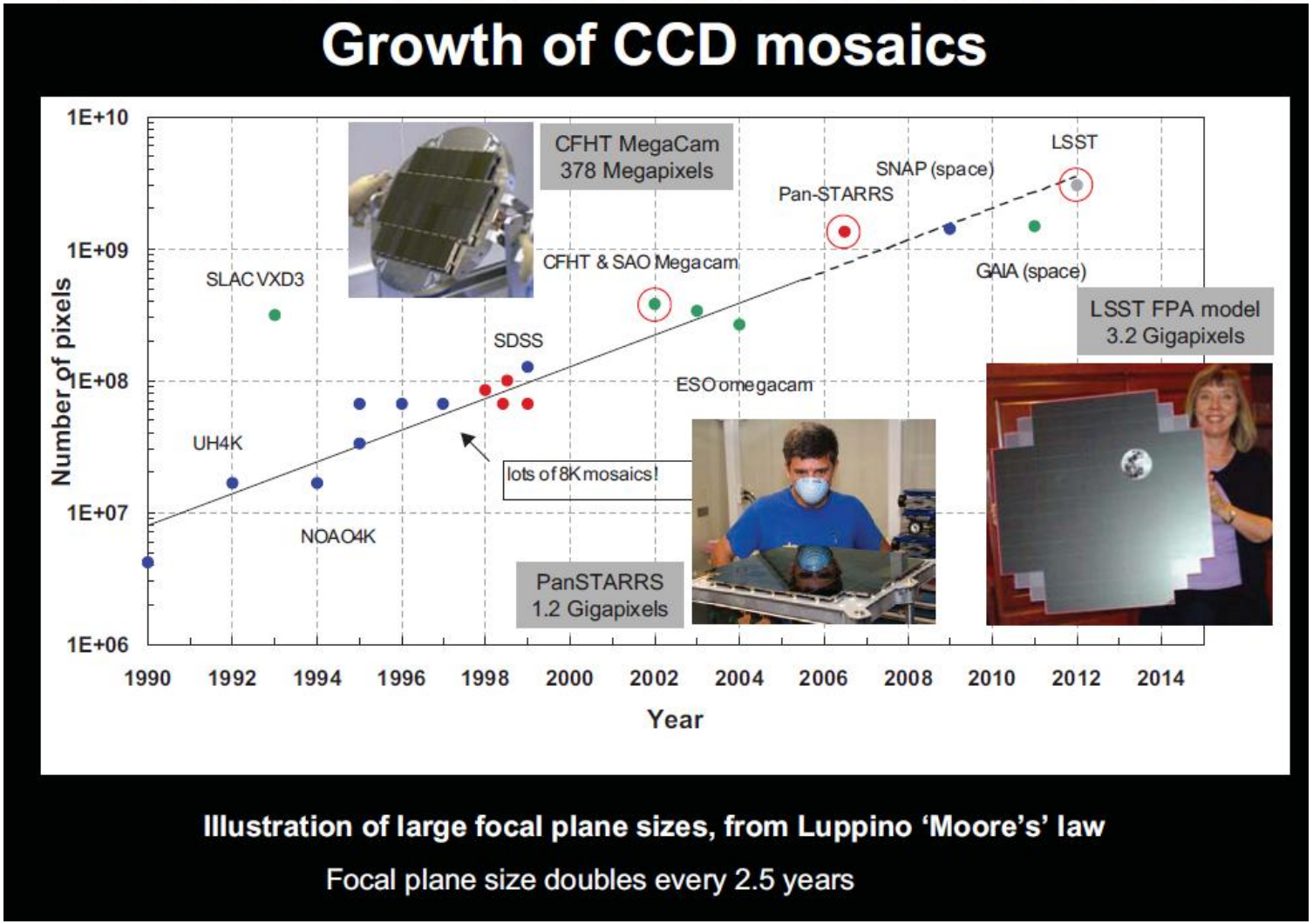
- Separate foam ladders
- Max deflection 20.5 mm



- Ladders joined by small foam piece every 40 cm
- Max deflection 20 μm

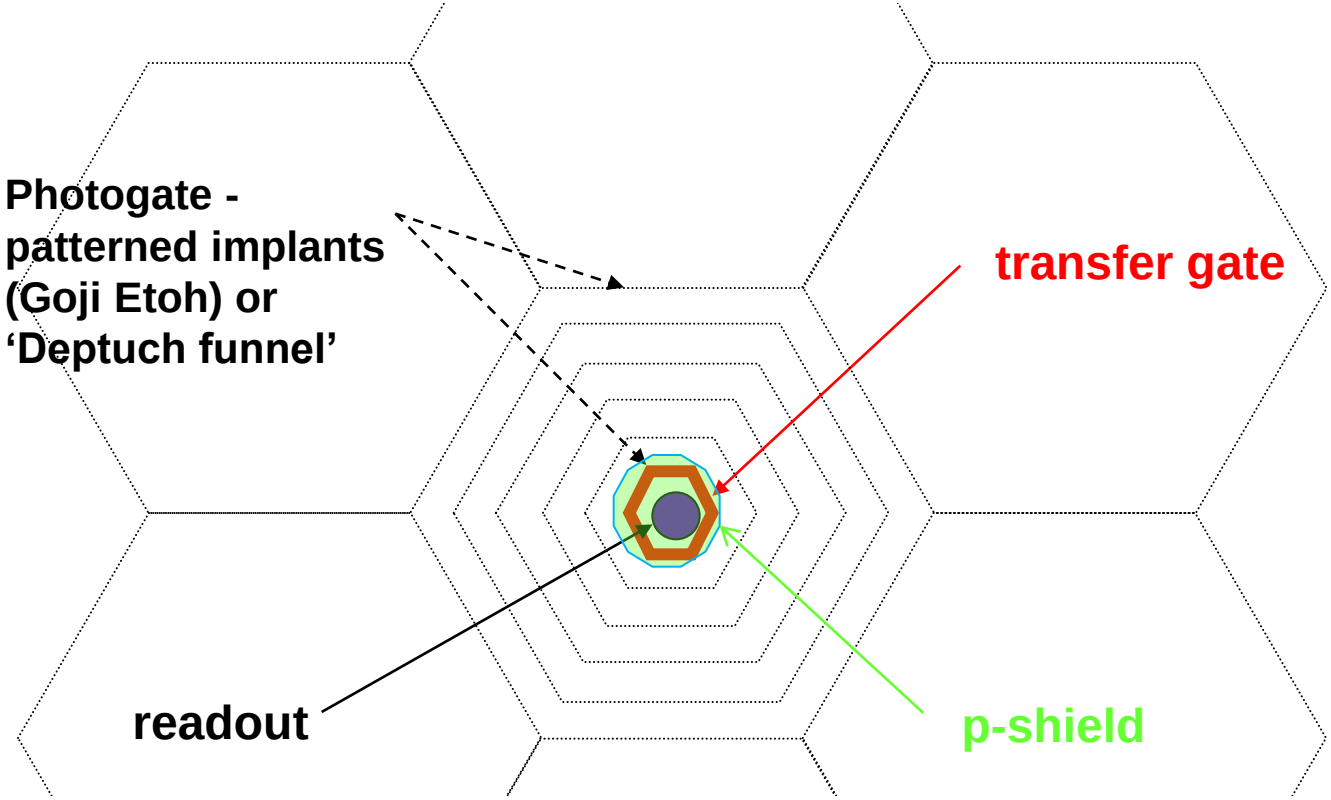
Steve Watson - *RAL*

System scale



LSST R&D going well – final stages of prototyping

SPT tracking layers for ILC or CLIC



SPT tracking pixels (~50 μm diameter):

- **PG preferred over PPD for such large pixels, charge collected under the ring-shaped transfer gate and then to the gate of the tiny sense transistor, below the p-shield**
- **Very promising also for timing layers (with additional in-pixel logic): patterned implants – all signal charge can be collected with time spread of ~10 ns**

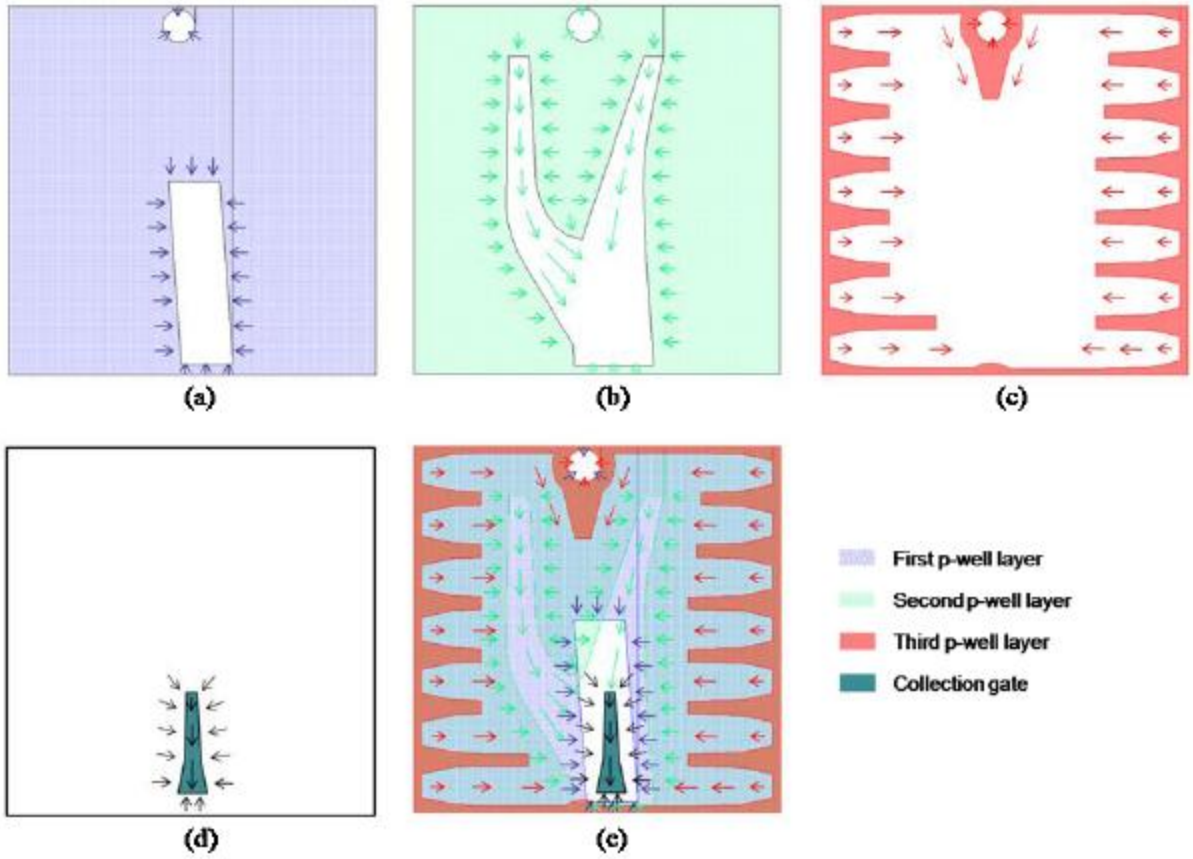
SPT timing layers for ILC or CLIC

Regions where 'full' time stamping is needed – 300ns or 10 ns

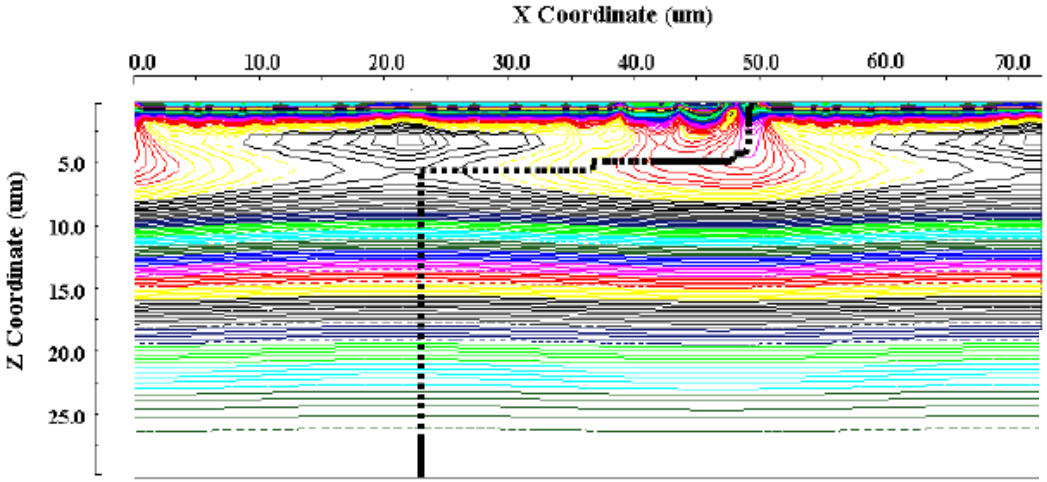
Timing pixels (~150 μm diameter):

- **in-pixel CDS, sense transistor and discriminator, with time stamp. Possibly with multi-hit register**
- **Between bunch trains, apply data-driven readout of hit patterns for all bunches separately**
- **p-shield ensures full min-I efficiency, as with the tracking pixels**
- **Higher power dissipation of continuously active front-end implies active cooling, with an impact on layer thickness**

Patterned implants for fast charge collection

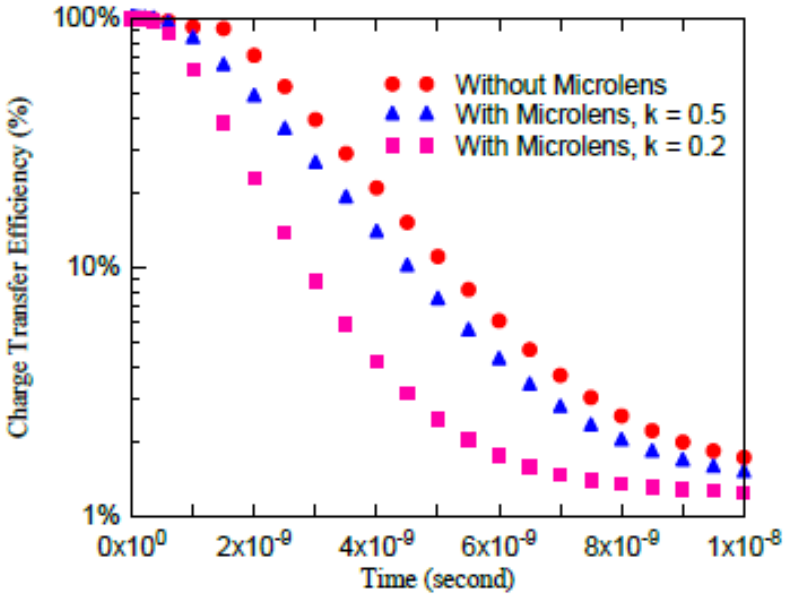


Goji Etoh, 2009



90% charge collection from uniform illumination of back surface within ~5 ns (simulation)

Goji Etoh, 2009



Recent work by e2V on CMOS pixel waveform sensors for huge multi-mirror telescopes covers many of the requirements for ILC timing layers. Growing interest in fast CMOS pixel sensors

DSM transistors – noise performance

New results from Jim Janesick, reported at workshop on imaging systems for astronomy, San Diego, June 2010. Figures from Janesick SPIE 7742-11 (to be published)

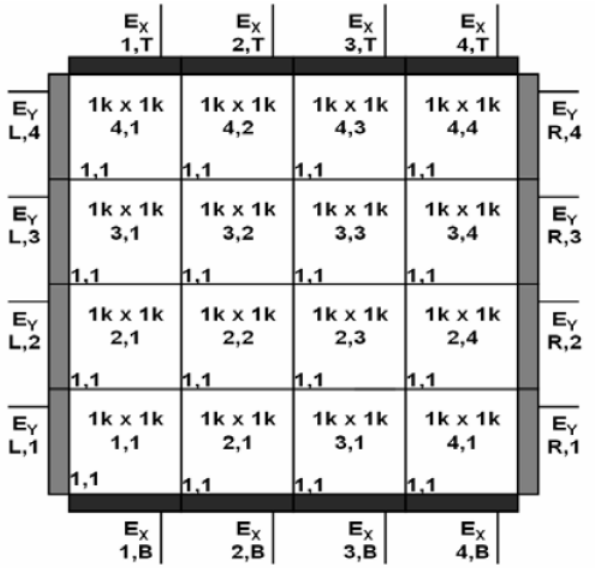
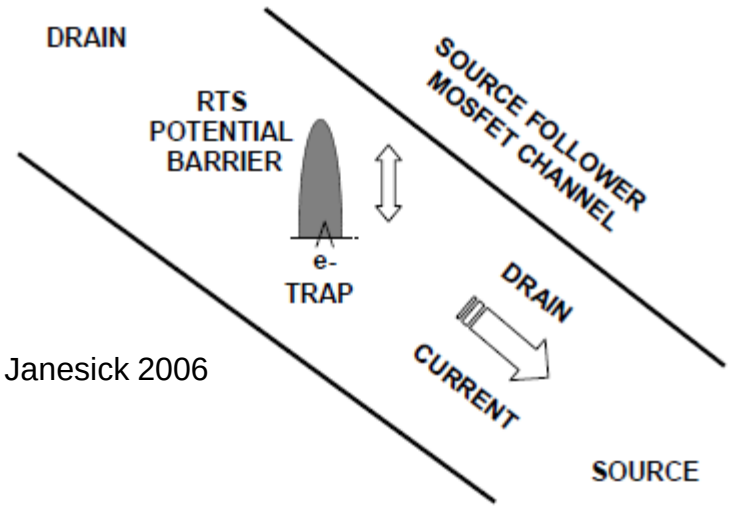


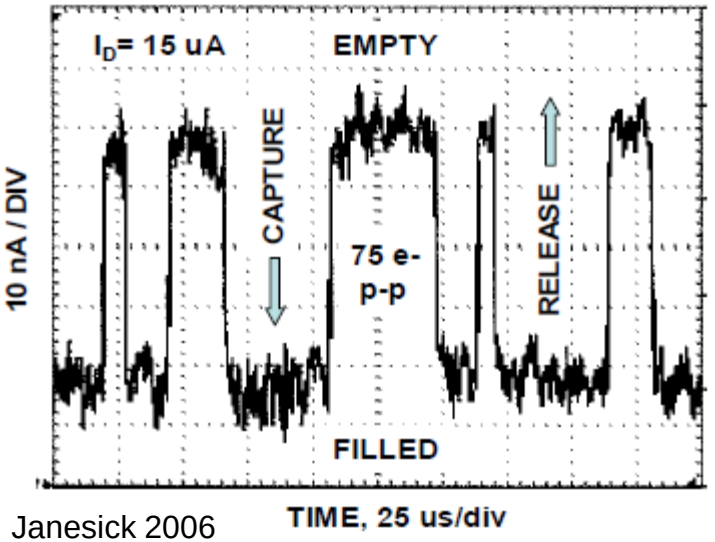
Figure 15. Block diagram of a stitched 4k x 4k imager.

4 x 4 cm^2 devices in Sandbox 6 (SB 6), 10 x 10 cm^2 to be processed next year, in SB 7. SB 6 yields are 'high'

RTS noise



Janesick 2006



Janesick 2006

Note: These fluctuations amount to only 0.3% of the drain current

- **RTS is the dominant residual noise source in charge-coupled CMOS pixels**
- **As with CCDs, transistor noise can be much reduced by using a buried-channel MOSFET for the source follower (but not completely eliminated, due to the presence of bulk traps). Now established for CMOS pixels by recent work from Janesick …**

Device architecture and noise performance – observations from e2V

- Studies by Dave Burt, building on noise optimisation in CCD structure over many years, now working with CMOS pixel devices from Tower
- Main source of 1/f noise is **not** interfaces states, which are *filled* during transistor operation
- Evidence for this includes: ionising radiation increases the interface state density (and hence the in-pixel dark current) but does not degrade the 1/f noise
- Main source is believed to be tunneling to bulk trapping states in the dielectric
- RTS noise is probably due to individual traps of this type, which trigger current injection from edge effects, or other 2-step phenomena (K Kandiah was a great pioneer in this)
- **RTS noise can be effectively suppressed by correlated double sampling (CDS), which is included in our design concept, both for tracking and timing devices**
- From their CCD experience, patterned implants (Goji Etoh) or the 'Deptuch funnel' can achieve nanosecond-level charge-collection, but not necessarily satisfying the typical **voltage restrictions** of deep-submicron CMOS
- The 5 V/1.8 V dual gate process at Jazz may suffice, but higher voltage can be explored (with significant NRE costs). Not many DSM foundries offer such flexibility, but the need for advanced imaging devices for science is increasing

Cost estimate

- **For construction starting ~2020, estimates are pretty speculative**
- **Assume 'SLD Vertex' approach, not typical astronomy approach of fully tested Grade A devices**
- **This means a simple DC-pass acceptance test by vendor, with full testing by customer (yield was >95% for 8.0x1.6 cm^2 SLD devices)**
- **Under these conditions, e2V estimate current costs of ~$1k per 8x8 cm^2 thinned device**
- **12,700 devices (tracking) plus 17,900 devices (timing) → $40M total**
- **Add ~10% for mechanics and off-device electronics, but device costs will fall with expanding markets**
- **More expensive than SiD tracker, but enhanced performance may make it interesting. In any circumstances, it is a modest fraction of the overall detector cost**

Conclusions

- The SPT offers the possibility of high performance tracking over the full polar angle range, with minimal material in all directions
- For multi-jet physics (where there's always something in the forward region) this looks particularly appealing
- In general, having nearly all the photons convert in the ECAL (or just before it, in timing layers) is desirable
- These advantages need to be established and quantified by simulations, which are now beginning
- The needed pixel technology is currently available, though some development may be needed to make timing layer devices that satisfy the CLIC requirements
- The LC detector community may not have enough resources to sustain all the R&D needed for this, but much is being done for astronomy and SR applications. Goji Etoh, Jim Janesick and others are very willing to collaborate. Inter-disciplinary R&D in this area looks quite promising
- By 2020, 40 Gpixel systems for science will be quite common. We are not alone …

World's largest CMOS imaging sensor, by Canon Inc, 20.2x20.5 cm^2 (thanks to Norm Graf for the link)