

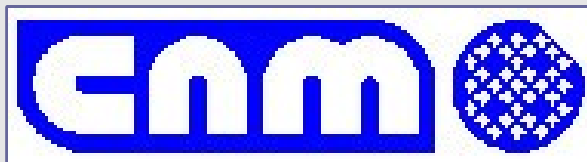
# IR Transparent Si microstrips

## (alignment optimized Si sensors)



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This year, the International Workshop on Linear Colliders organized by the European Committee for Future Accelerators (ECFA) will study the physics, detectors and accelerator complex of a linear collider covering both CLIC and ILC options.

**Monday 18 - Friday 22 October 2010**  
**CERN & CICG** (International Conference Centre Geneva, Switzerland)  
<http://cern.ch/WLC2010>

### International Workshop on Linear Colliders 2010

## IWLC2010

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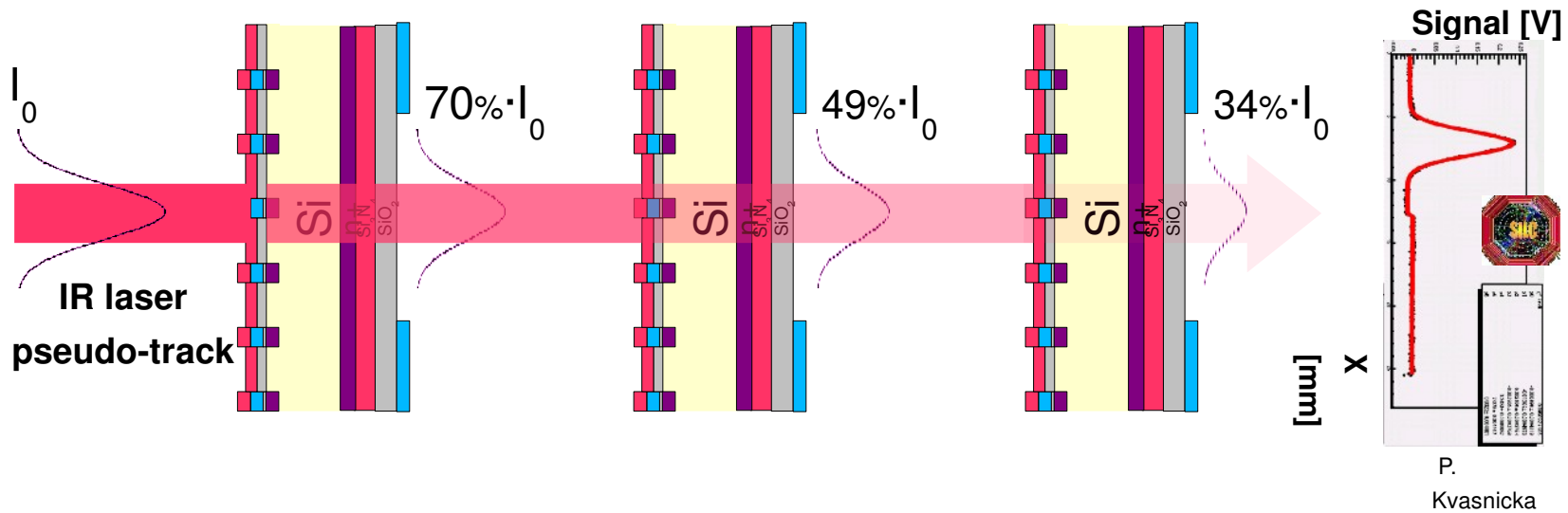


# Outline

- What is an infrared hardware alignment system
- How to increase transmittance of a microstrip detector
- Simulation of prototype transparent microstrips
- Measurements of prototypes
- Conclusions and outlook

# Microstrips as semitransparent light detectors

- Laser tracks can be used by a hardware system to align the tracker



- First implemented by AMS I, then AMS II and CMS
- Goal of this project is to improve transmittance to infrared light of microstrip detectors.

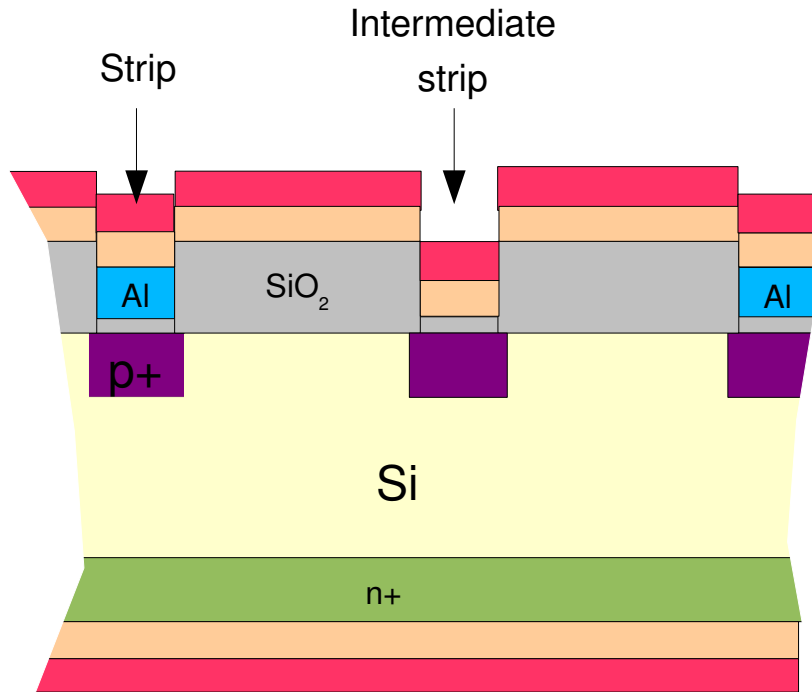
Main constraint are:

- Do not alter the standard production process
- Do not include alien materials

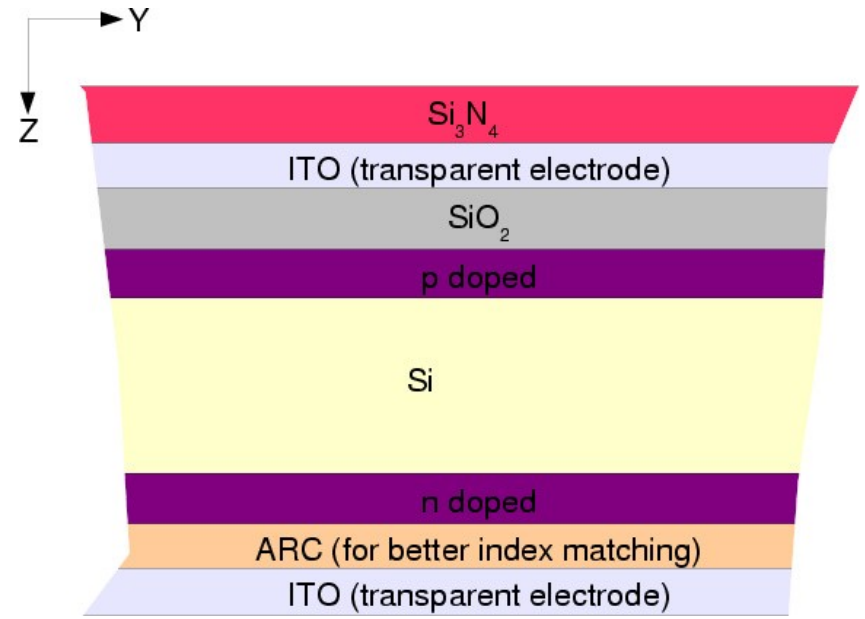
## How to increase %T of a strip detector

- **Aluminum** strips act like **mirrors**. If strips are too wide, reflectance will increase too much
  - Optimize pitch to strip width ratio
  - Use transparent electrodes?
  
- IR light penetrates 300  $\mu\text{m}$  Si. Multiple reflections at the interfaces  $\Rightarrow$  **Interferences**
  - Choose thickness of the materials such that **light interferes constructively**
  - Complications come from strips  $\Leftrightarrow$  **diffraction** grating (pitch $\sim$ 50  $\mu\text{m}$ ,  $\lambda\sim$ 1  $\mu\text{m}$ )
  
- We need to develop a **simulation** to calculate:
  - Transmittance (%T), Reflectance (%R) and Absorptance (%A) for a  $\mu$ strip detector
  - Optimize the design (pitch, strip width, thickness of layers)
  - Define prototypes

# Simplified simulation of $\mu$ strips as plane-parallel layers



$\approx$



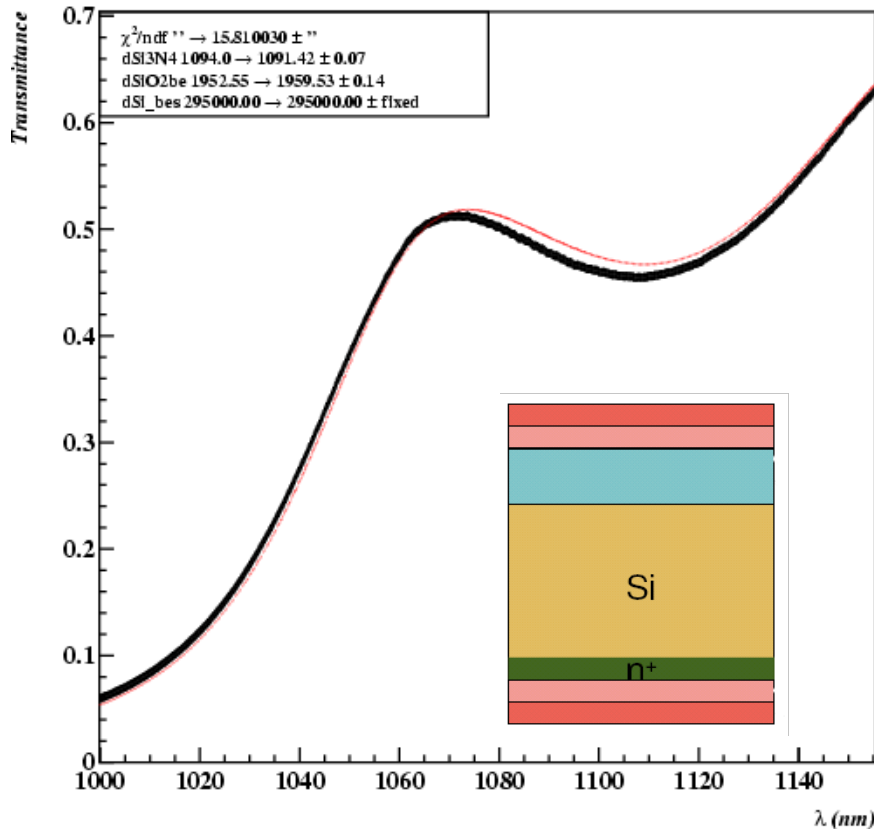
- ✓ Interference
- ✓ Diffraction

- ✓ Interference
- ✗ Diffraction

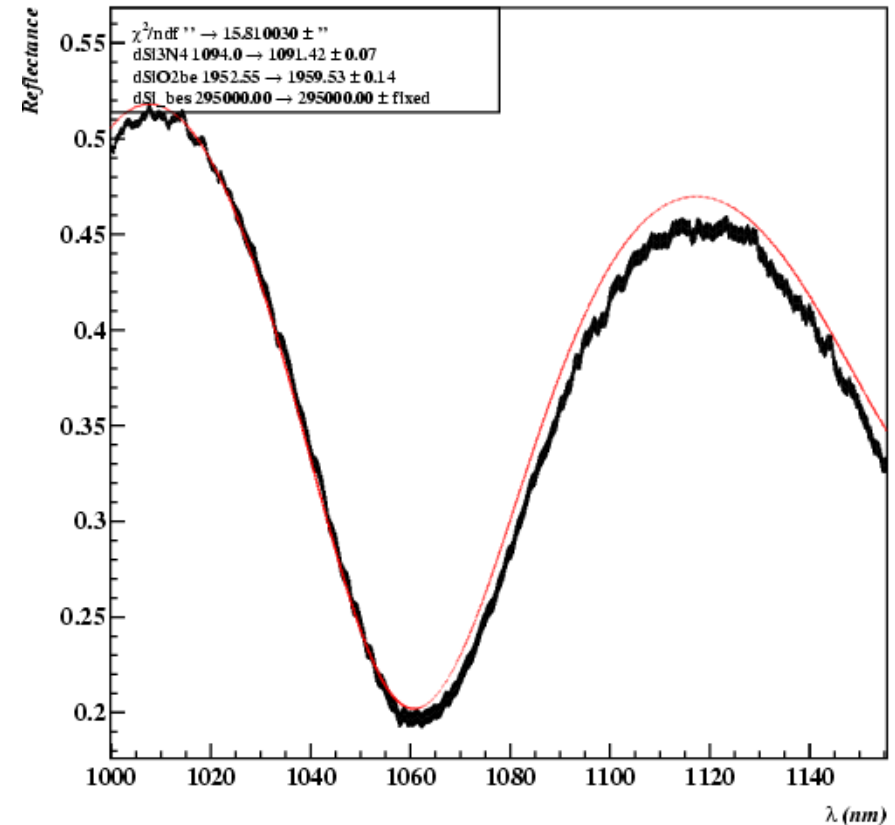
# Planeparallel layers simulation

- Ideal layout: no strips  $\Rightarrow$  no diffraction  $\Rightarrow$  all energy goes forward
  - Useful to estimate maximum performance ( $T_{\max} \sim 75\text{-}80\%$ )
- Useful to characterize refractive index of materials and deposition tolerance (backengineering)

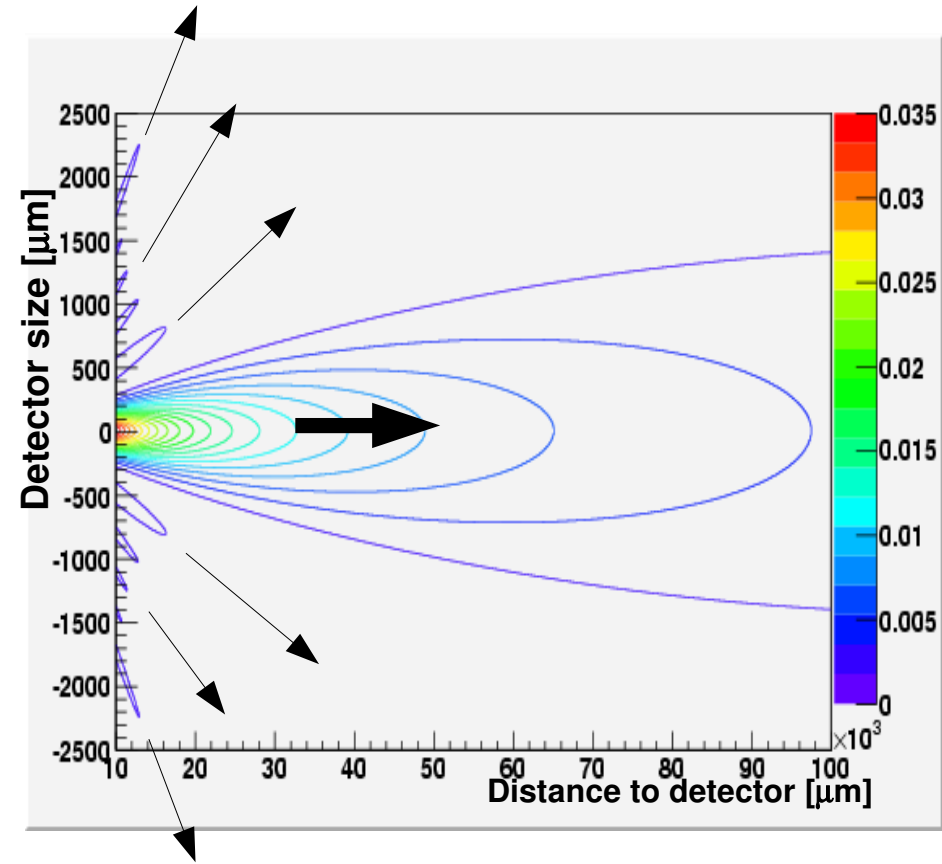
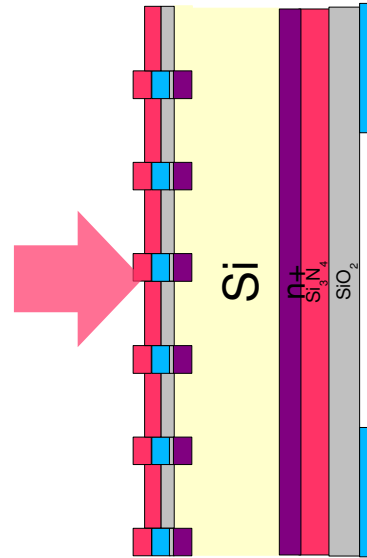
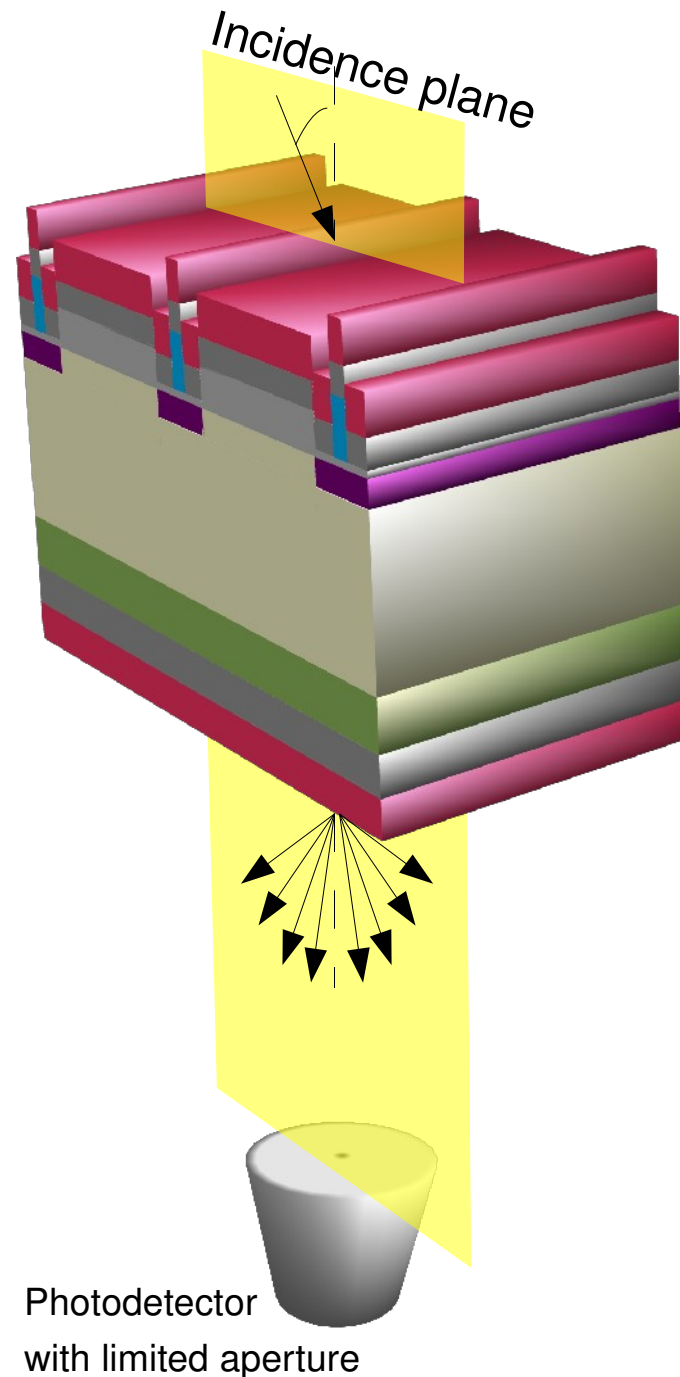
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## Including diffractive effects



- Diffraction here means that:
  - Energy spreads in secondary maxima
  - Light spreads off the central beam
  - Experimentally  $T = T(\text{distance to detector})$

## Main conclusions from full simulation

See for instance: [Eudet-Memo-2009-23](#)

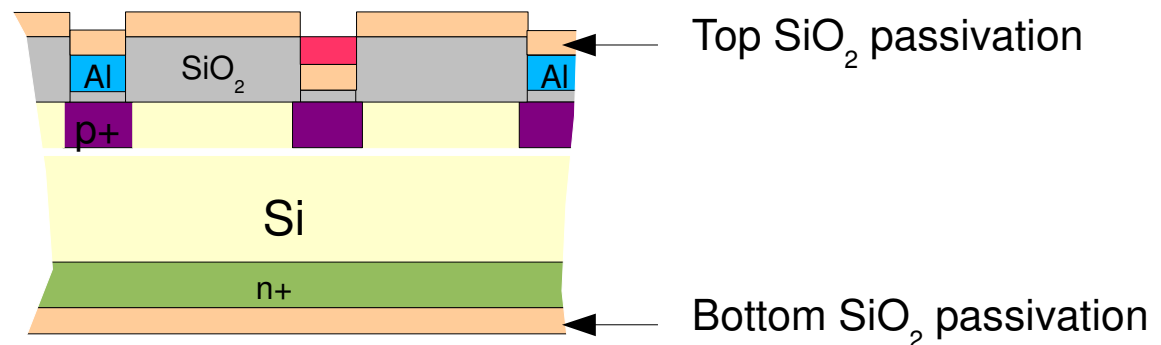
- Strips (having metal or not) behave as a diffraction grating.  
Sensors with intermediate strips are more “efficient” gratings  $\Rightarrow$  worse as %T devices
- Pitch reduction (=closer strips):
  - decreases transmittance (1<sup>st</sup> order effect)
  - increases reflectance (2<sup>nd</sup> order).
- Strip width increase:
  - increases reflectance (1<sup>st</sup> order)
  - reduces transmittance (2<sup>nd</sup> order).
- Top and bottom passivation layers<sup>(\*)</sup> behave as an **AntiReflection Coating (ARC)**  
Top passivation thickness more critical than bottom.

(\*) Passivation= $\text{Si}_3\text{N}_4$  on  $\text{SiO}_2$

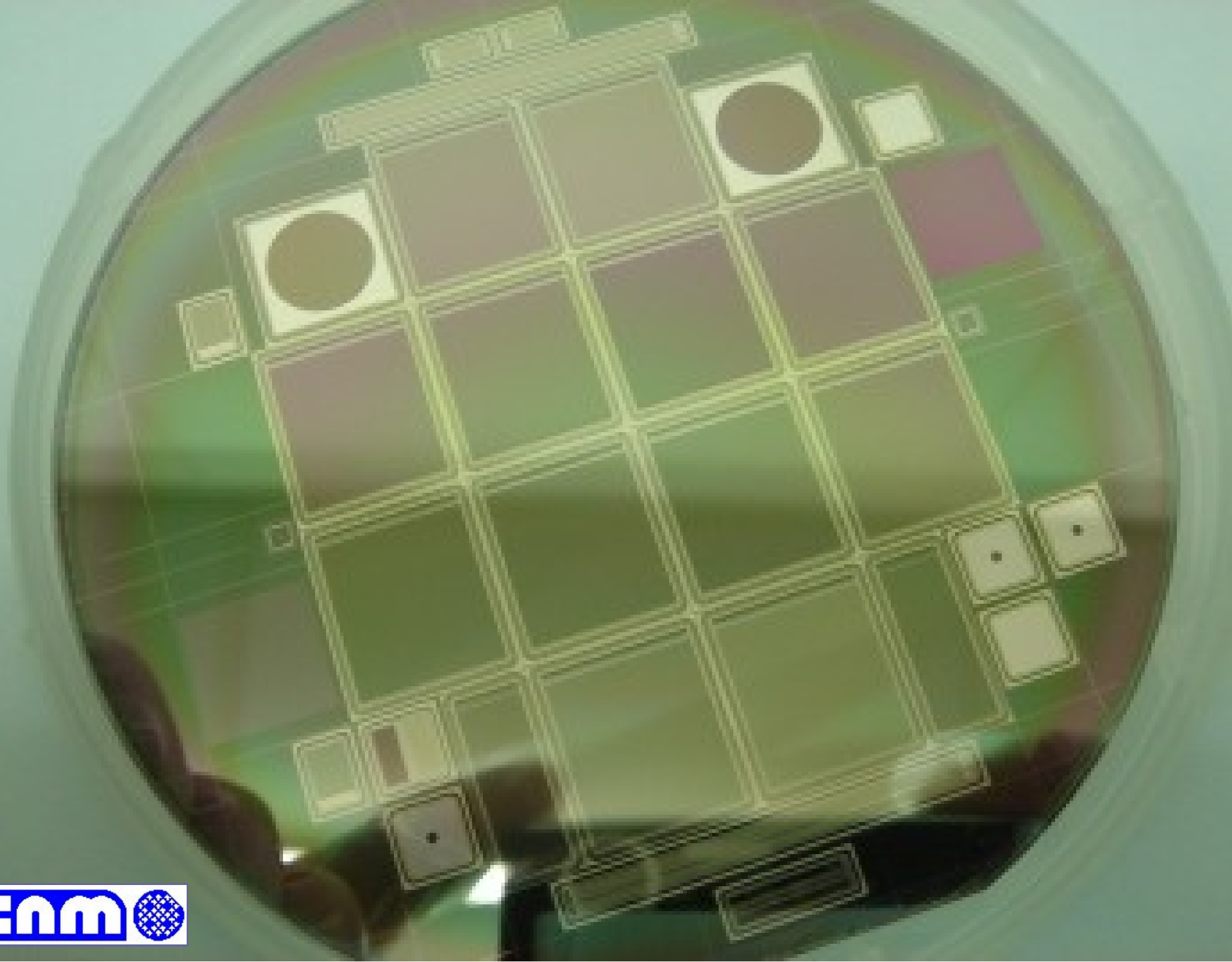


## Validation of full simulation (interference + diffraction)

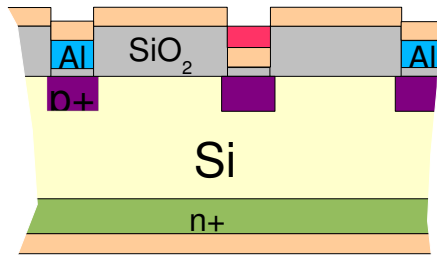
- Validation of simulation not possible with already existing sensors from Hamamatsu
  - No information available on layers and thicknesses
- Therefore we need to validate the simulation with the same sensors we want to optimize
  - Flexibility of CNM allows to hold processing after first layer of passivation



- Observed simulation  $\neq$  measurement  $\Rightarrow$  Tune simulation

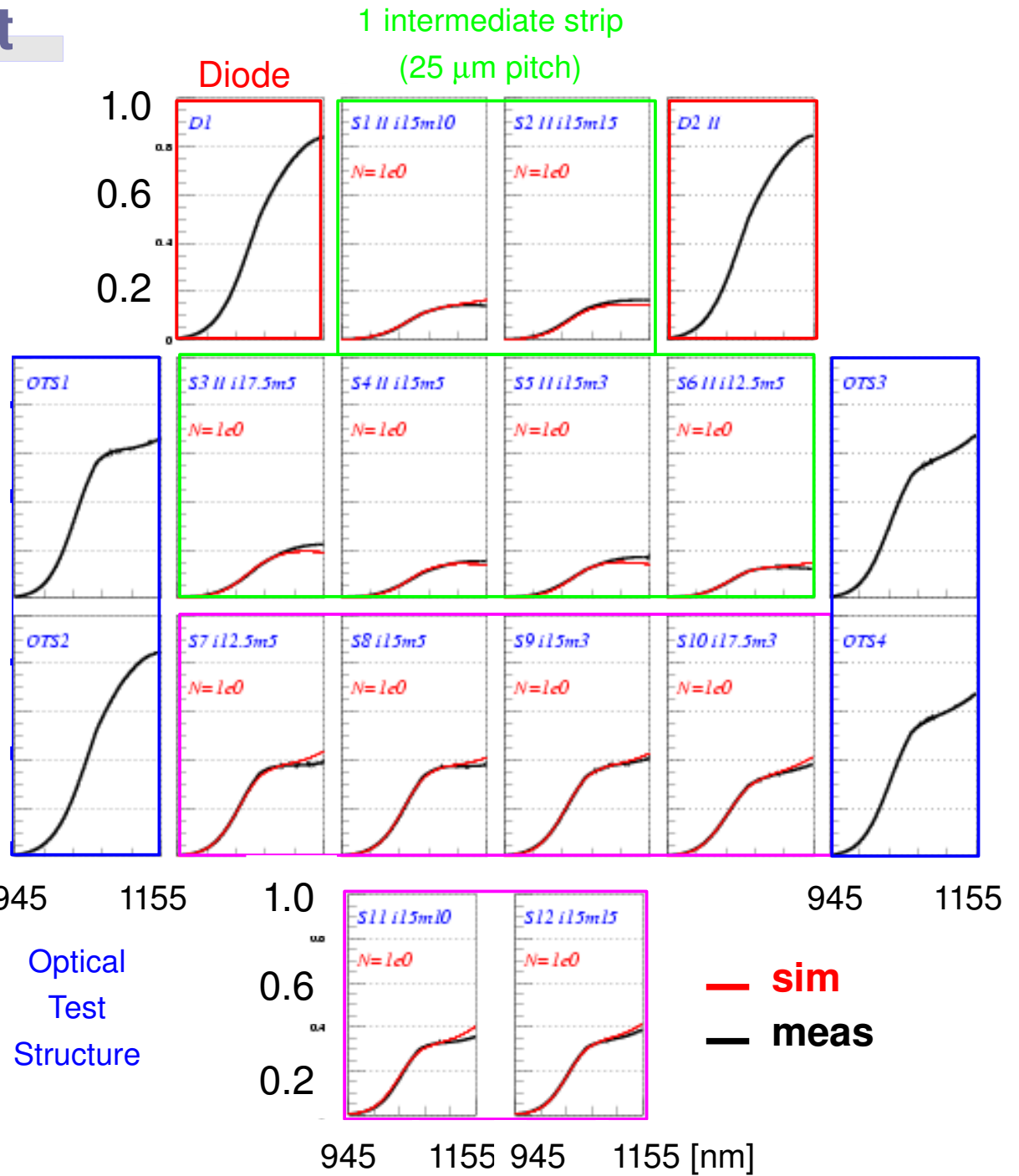


# Wafer 1, measured & fit



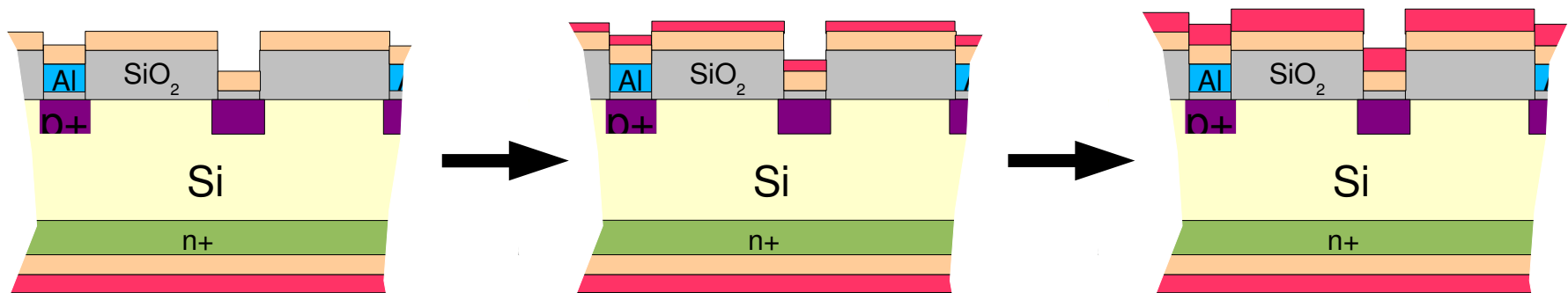
Uncomplete top&bottom passivation

Transmittance ~40%



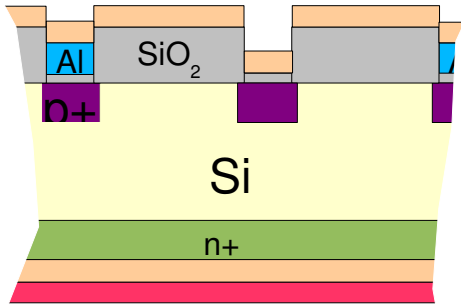
## Last steps before the end of the run

- Now, for the last 3 wafers:
  - Iterative process: deposit  $\text{Si}_3\text{N}_4$  → measure %T → fit → correct if needed



Current situation  
(18<sup>th</sup> October 2010)

# Wafer 3, measured



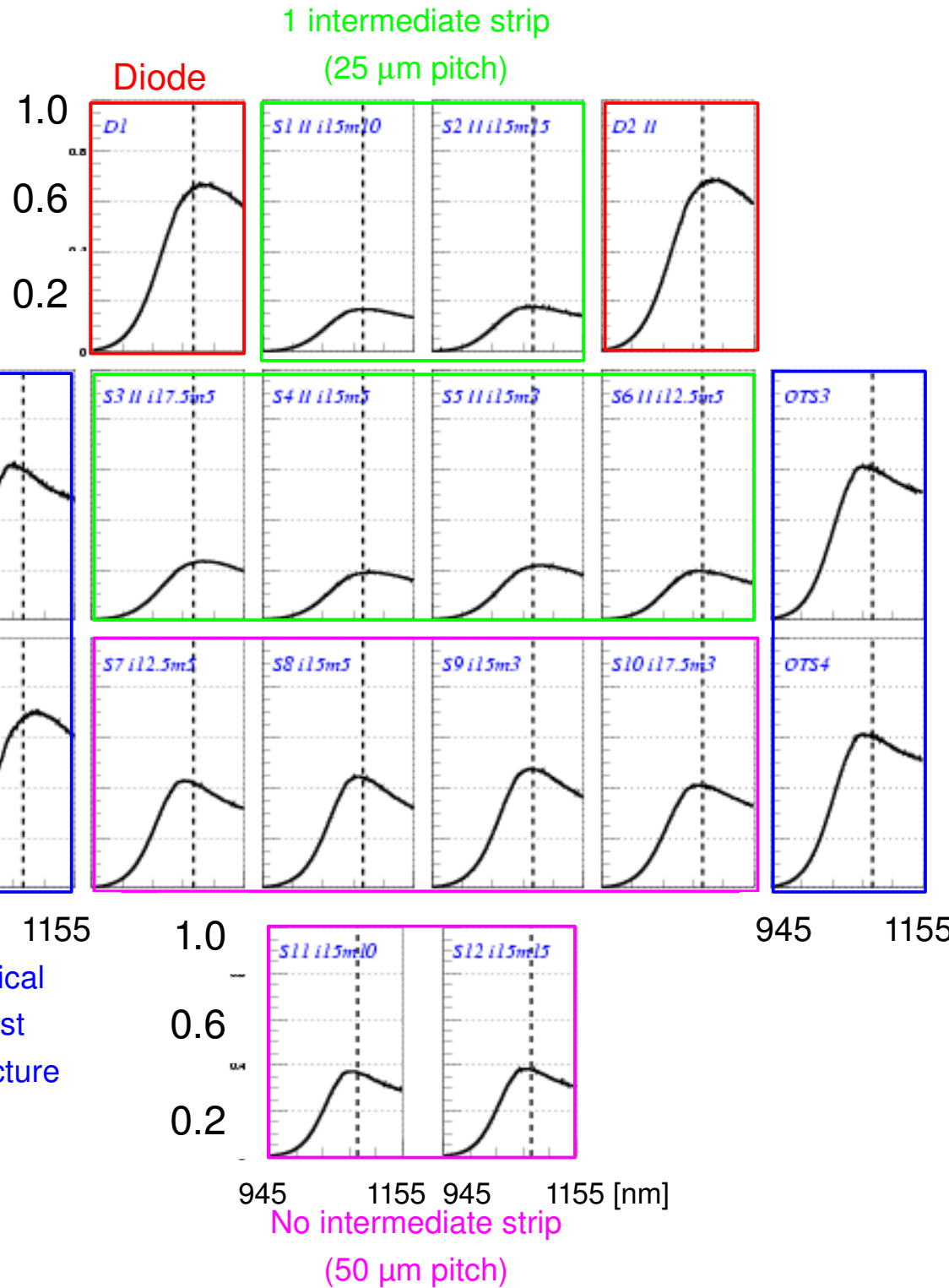
Current situation  
(measured yesterday at CNM)

Complete bottom passivation  
Transmittance~45%

For comparison:

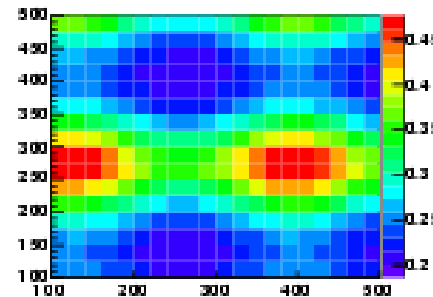
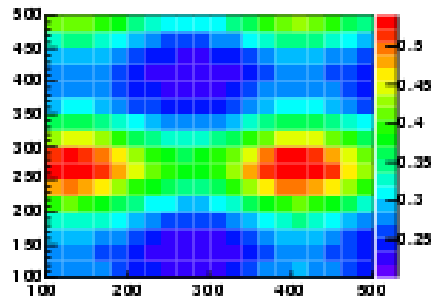
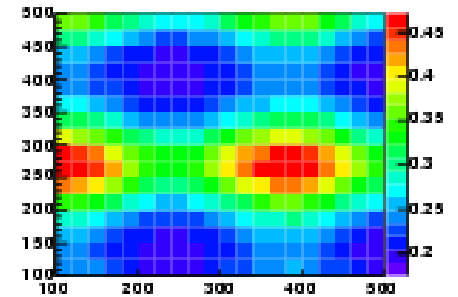
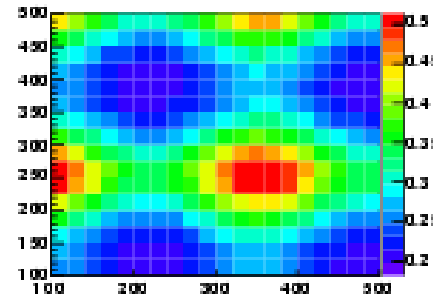
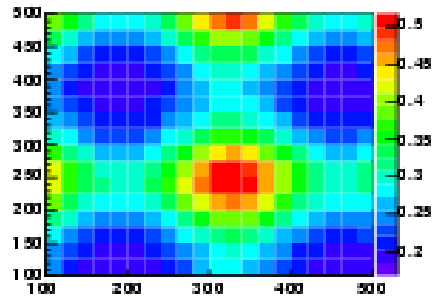
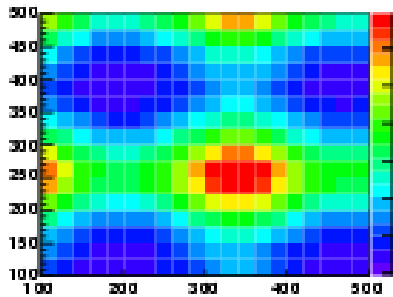
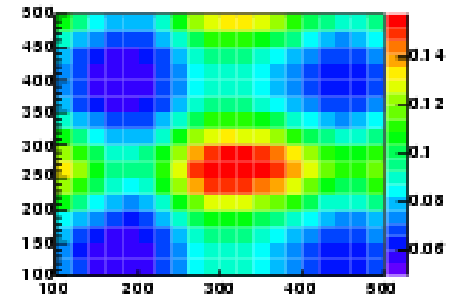
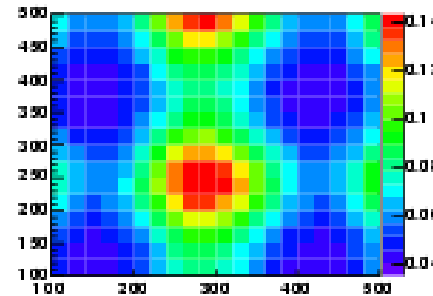
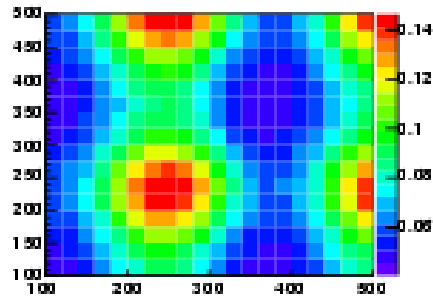
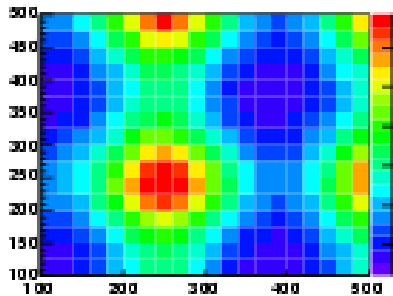
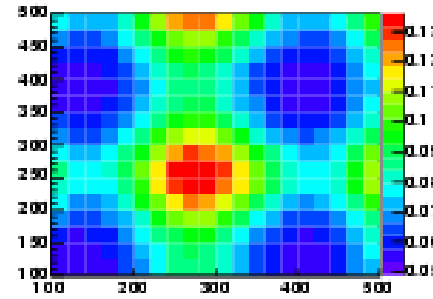
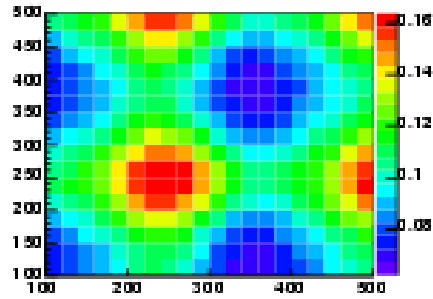
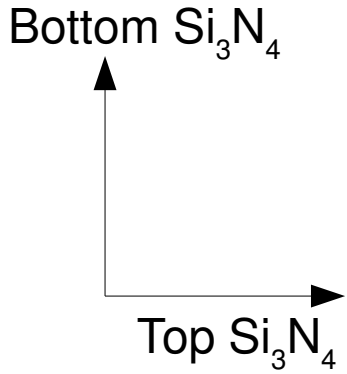
CMS=20% with pitch > 80 μm

AMS=50% with pitch 110 μm

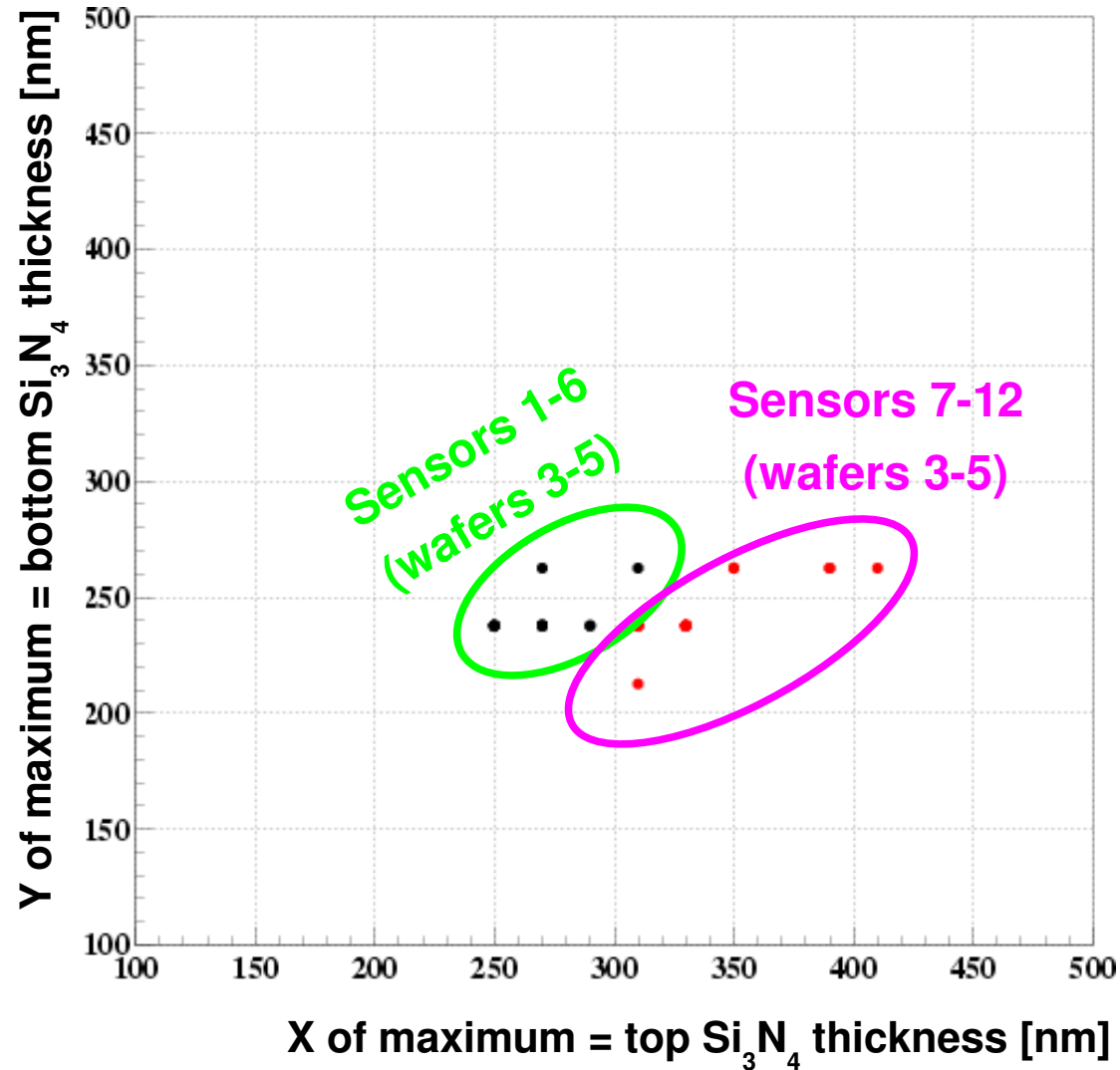


# Wafer 3: Sequential deposition of Si<sub>3</sub>N<sub>4</sub> (using measured thickness)

$T = T(\text{top Si}_3\text{N}_4 \text{ thickness, bottom Si}_3\text{N}_4 \text{ thickness})$  for the 12 sensors



## Best top and bottom thickness (wafers 3-5)



- Thickness of bottom Si<sub>3</sub>N<sub>4</sub> passivation layer does not depend on intermediate strip
- Upper Si<sub>3</sub>N<sub>4</sub> layer is thicker for sensors without intermediate strip

# Conclusions

- Densely populated microstrip silicon sensors can be made >50% transparent
- Transmittance depends more on pitch and less on strip width
  - Sensors with intermediate microstrips have lower %T
- Reflectance depends more on strip width
- Overall transmittance defined by the thickness of upper passivation  $\text{Si}_3\text{N}_4$  layer
  - Aiming for 55%
- We have very good transmittance for a very busy structure
- Upper  $\text{Si}_3\text{N}_4$  layer is thicker for sensors without intermediate strip
- Run will be finalized in October.

# Outlook

- Apply lessons learnt in a new run of highly transparent sensors
  - Aiming for >60%

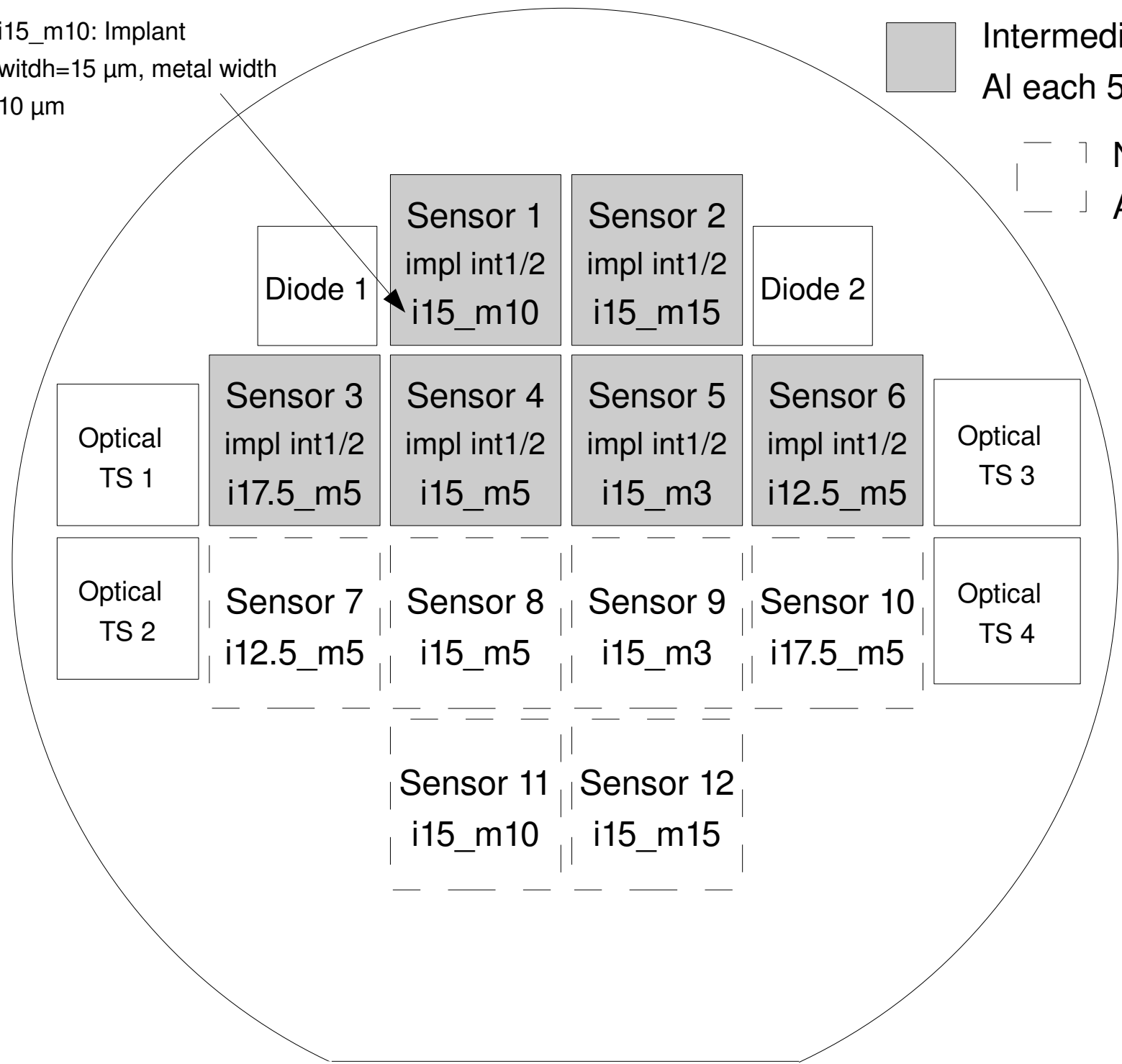


**BACKUPS**

i15\_m10: Implant  
width=15 μm, metal width  
10 μm

Intermediate implant each 25 μm  
Al each 50 μm

No Intermediate implant  
Al each 50 μm



# (x,y) of first maximum vs sensor id in wafers 3, 4, 5

X= top  $\text{Si}_3\text{N}_4$  thickness

Y= bottom  $\text{Si}_3\text{N}_4$  thickness

Sensors with intermediate strips=25  $\mu\text{m}$  pitch

Sensors without intermediate strips=50  $\mu\text{m}$  pitch

