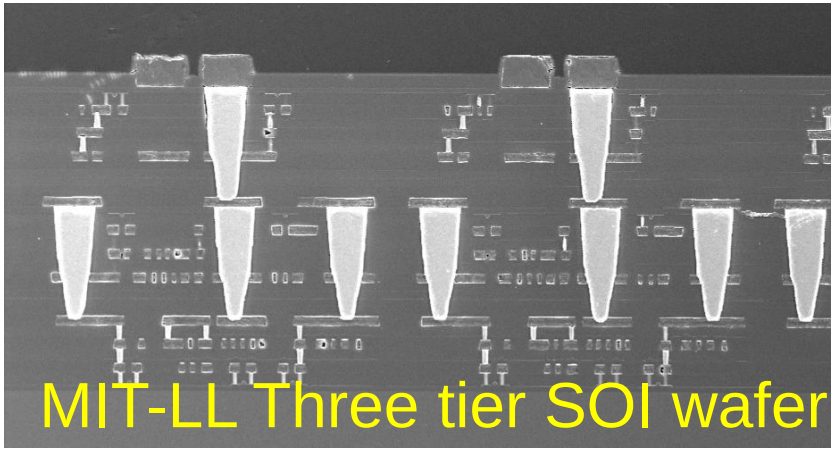
3D Vertex Detector Status

The requirement for complex functionality in a small pixel led us to investigate vertically integrated (3D) processes. Developed to enable stacking of multiple layers of chips, the suite of technologies includes many techniques of interest for vertex detector development. These processes include techniques developed for:

- Wafer Bonding
- Wafer thinning
- Alignment
- Fabrication of vias



I will discuss the status of 2 initiatives, the VIP (Vertically Integrated Pixel) chip in the MIT-LL SOI 3D process and the VIP2b, being fabricated in the Chartered/Tezzaron process.

VIP Chip Concept

The VIP chip was designed to demonstrate the ability to implement a complex pixel design with all required ILC properties in a 20 micron square pixel

Previous technologies limited to very simple circuitry or large pixels

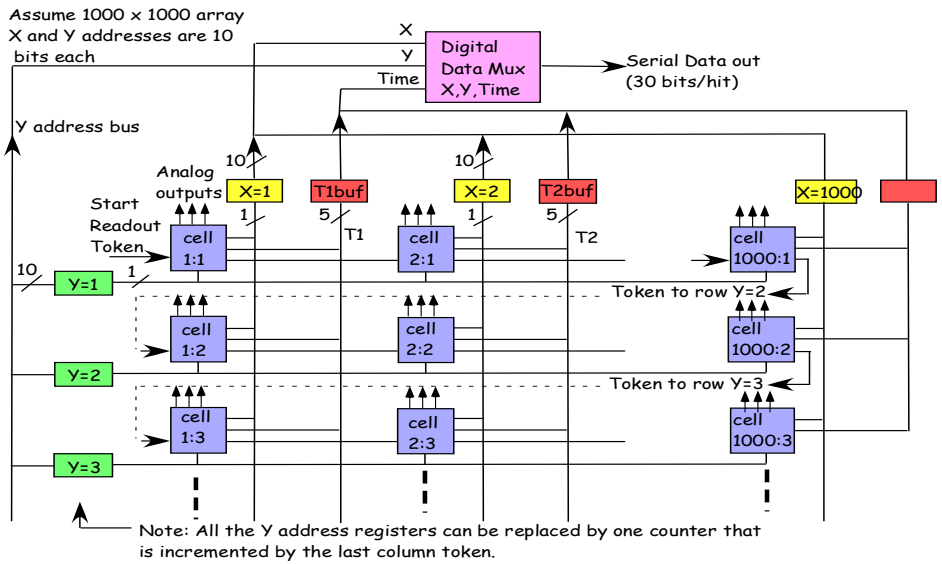
- 3D density allows analog pulse height, sparse readout, high resolution time stamp in a 20 micron pitch pixel.
- Time stamping and sparse readout occur in the pixel, Hit address found on array perimeter.
- VIP-1 64 x 64 pixel demonstrator version of 1k x 1k array.
- VIP2a 48x48 pixels with 30 micron pitch
- Submitted to 3 tier DARPA-sponsored multi project runs.

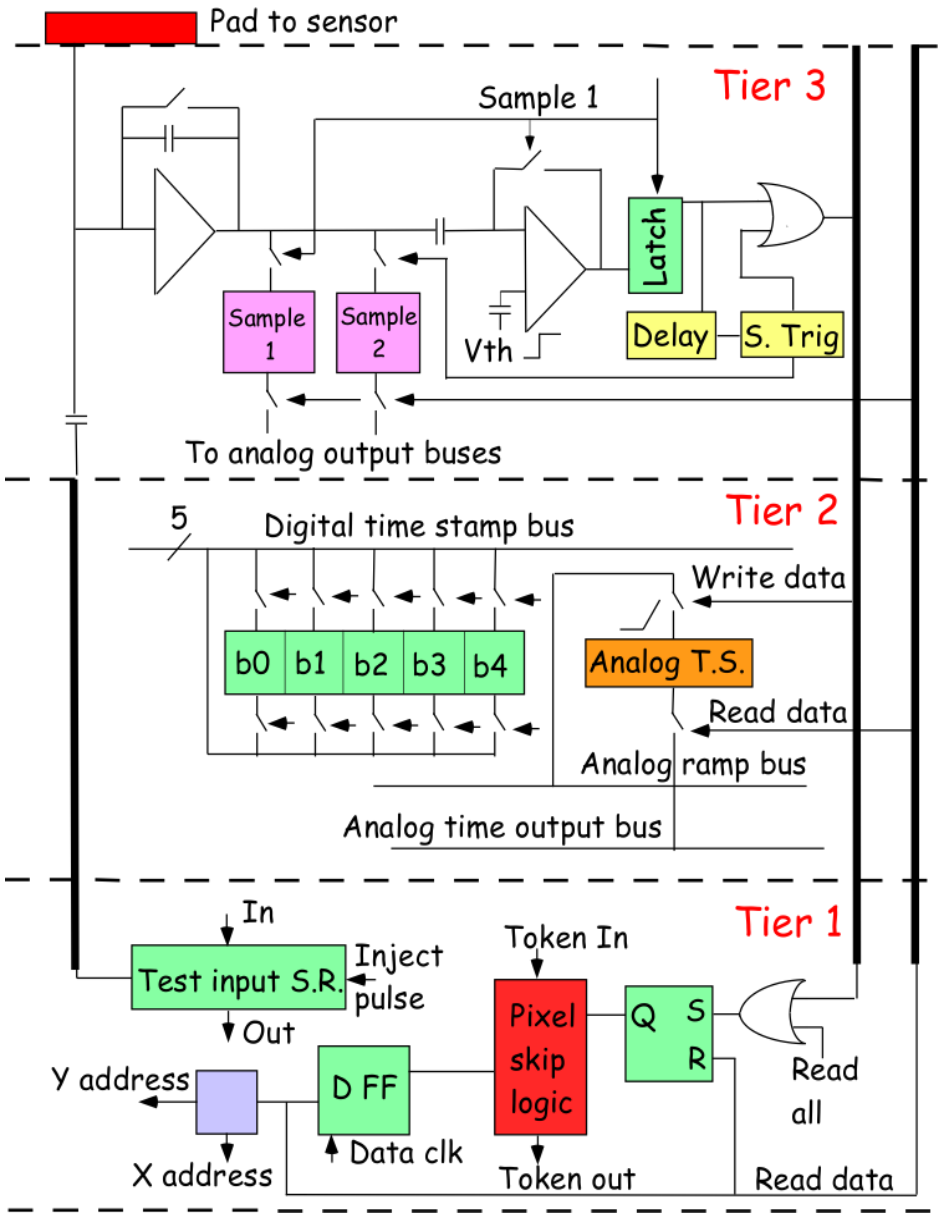
Low power front end 1875 $\mu W/mm^2$ x Duty Factor

VIP Chip Concept

Two (VIP2b) or three (VIP1,2a) tiers

- Double correlated sampling
- Analog and digital time stamp
  - Can use analog as a vernier to provide single bunch resolution
- Minimal area lost to peripheral circuits





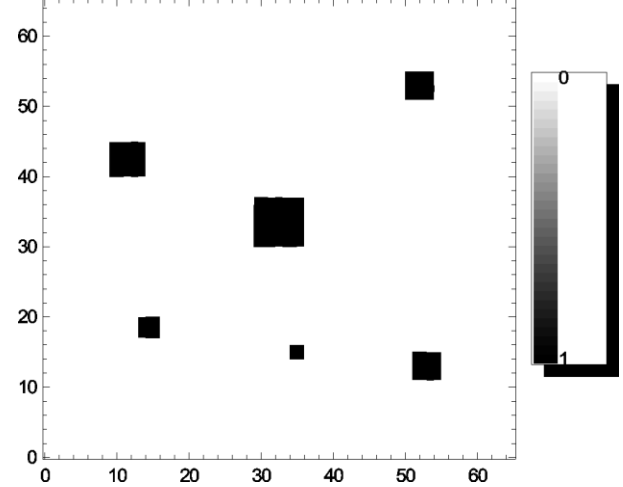
VIP1 Results

Basic functionality of the chip was demonstrated

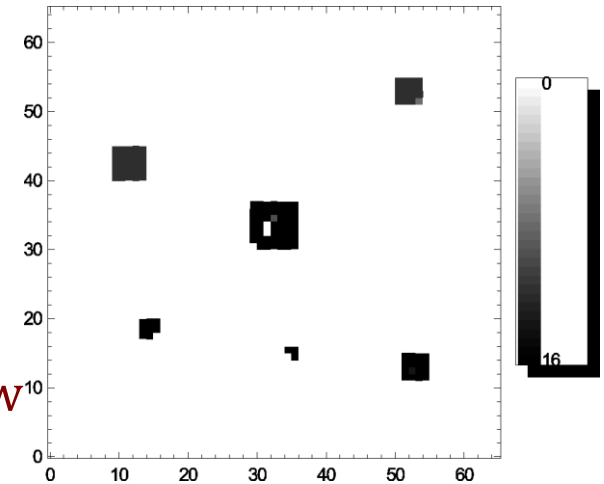
- Propagation of readout token
- Threshold scan
- Input test charge scan
- Digital and analog time stamping
- Fully sparsified data readout

No problems could be found associated with the 3D vias between tiers. However:

- Chip performance compromised by SOI issues:
- Large leakage currents in transistors and diodes
- Poor current mirror matching, Vdd sensitivity, low yield
- Soft shorts between nodes

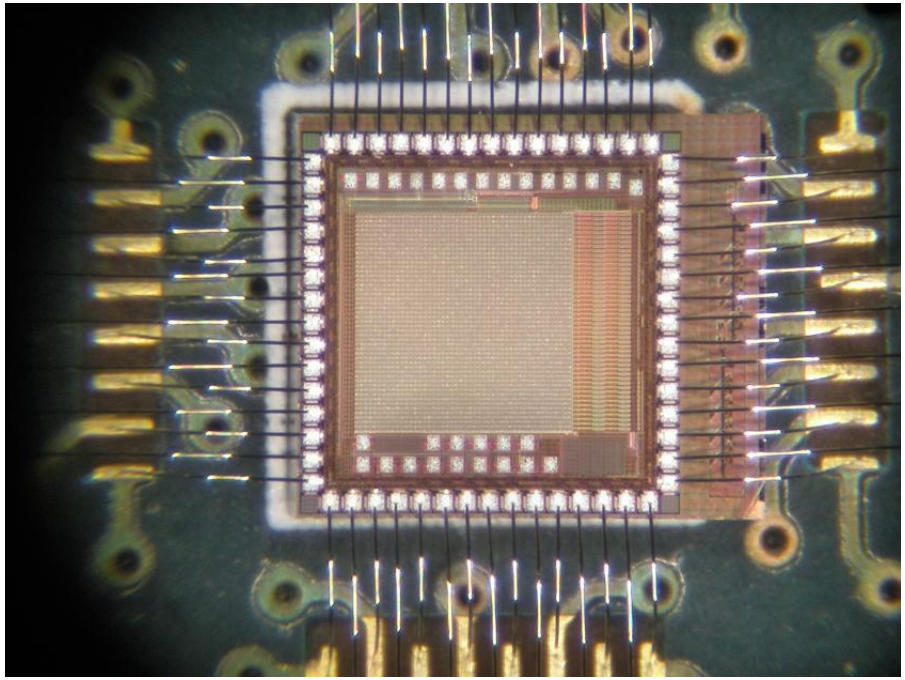


Preselected pattern of pixels for the injection of signal to the front-end amplifiers; pattern shifted into the matrix, than positive voltage step applied accross the injection capacitance; threshold levels for the discriminator adjusted according to the amplitude of the injected signal



Pattern of pixels from the preselected injection pattern that after injection of tests charge reported as hit (grey level represents number of repetition – 8 times injection)

VIP2a design



Conservative design to avoid SOI issues:

- Replace dynamic by static flip flops
- Scale trace routing rules by 1.2
- Increase transistor sizes (0.15μm -> 0.35μm)
- Replace source followers by Op amps
- Extensive power/ground mesh
- >2x larger sample/hold capacitors
- Redesigned current mirrors (use all separate devices instead of inter-digitated devices)

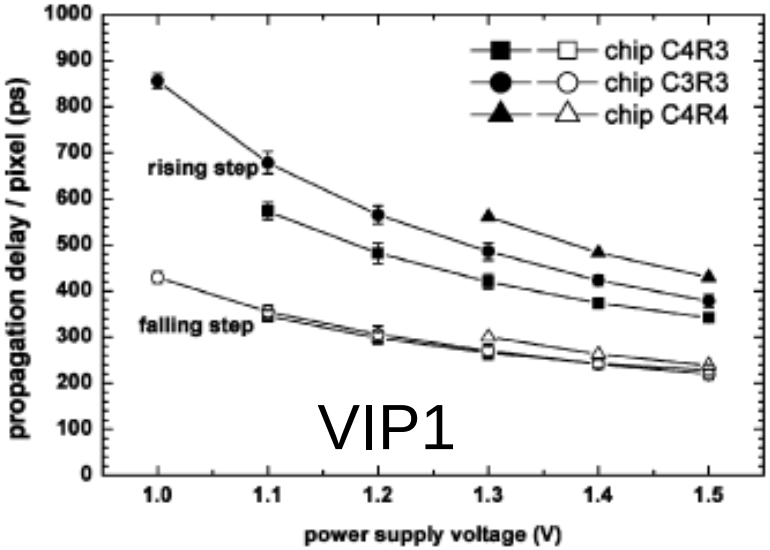
Increased functionality and testability

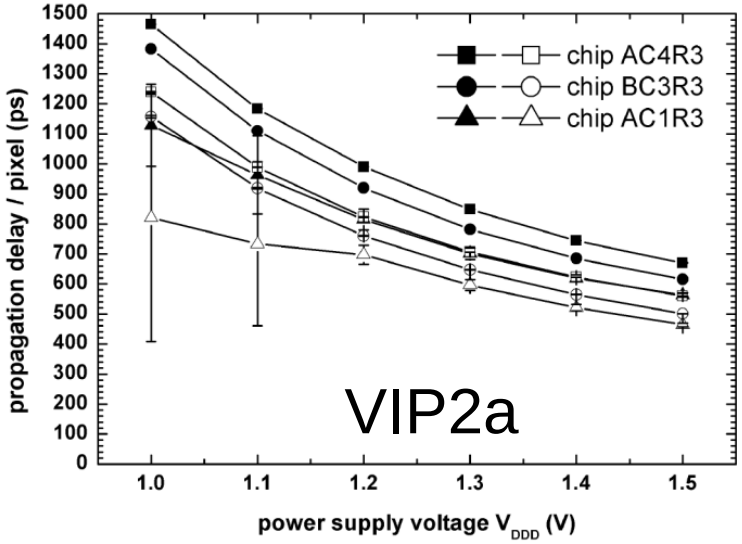
- 5->7 bit digital time stamp
- Discriminator arming on digital tier (reduce coupling)
- Switchable 20 fF load capacitor
- 48 x 48 array of 28 x 28 um pixels

VIP2a Test Results

The yield and performance are significantly improved in VIP2a.

- In VIP1 the analog time stamp did not work due to high leakage currents
- The analog time stamp, based on a voltage ramp and S&H, works well in VIP2a
  - Excellent linearity (no droop) from 10 us to 1 ms
  - Can be used in conjunction with digital time stamp to achieve equivalent 12 bit time resolution (less than 1 usec in 1 msec)
- Sparsification token propagation works over wider voltage range and on many more chips than on VIP1
- Token propagation time is higher in VIP2a due to larger transistor sizes
- Sparsification test mode works
- Protection diodes no longer leak

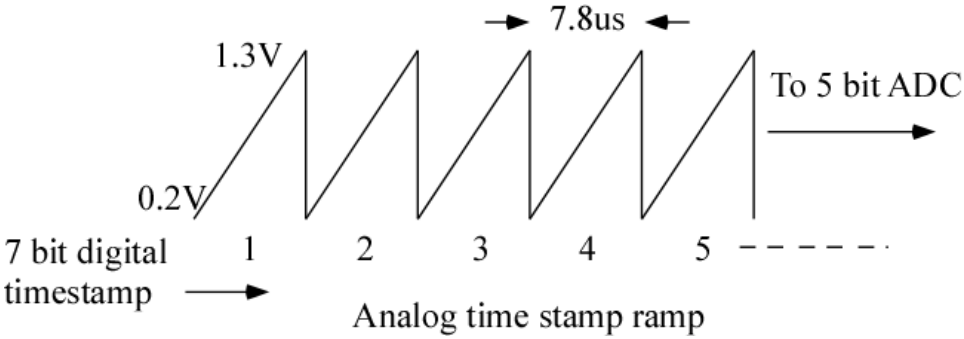


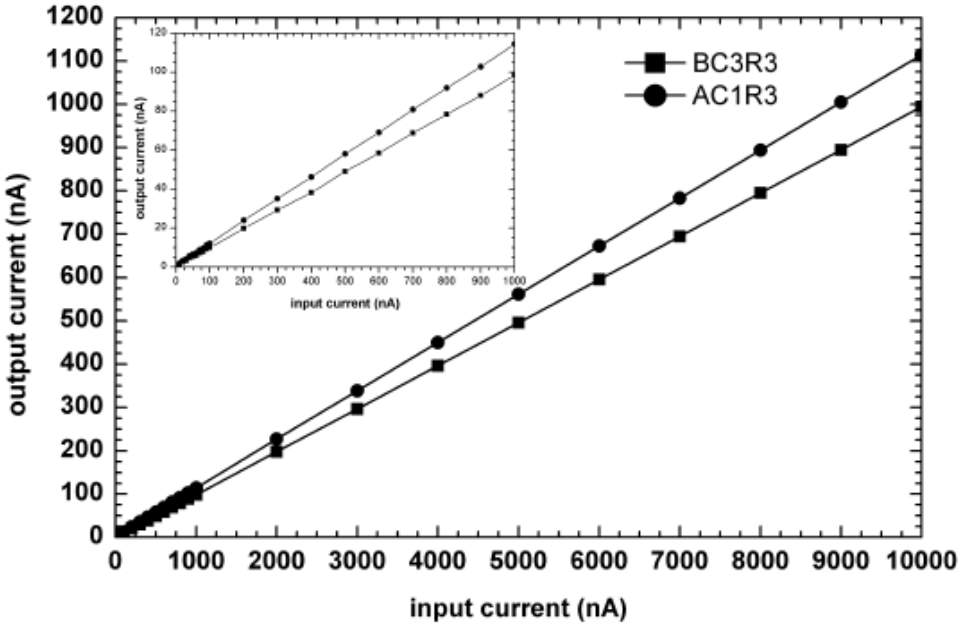


VIP2a Time Stamping

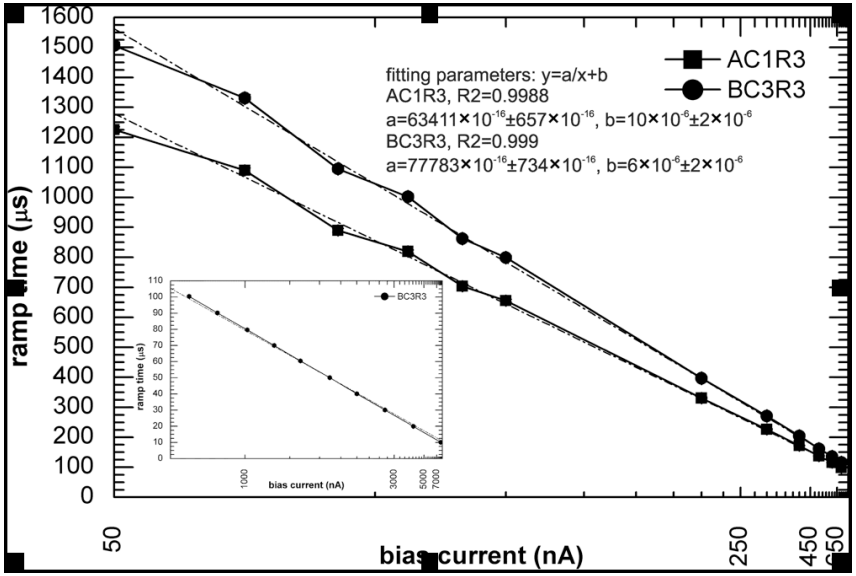
The current mirrors and time stamp ramp now function well

- Time jitter and linearity better than 1%
- Control over the full range to 1 ms





Current mirror linearity

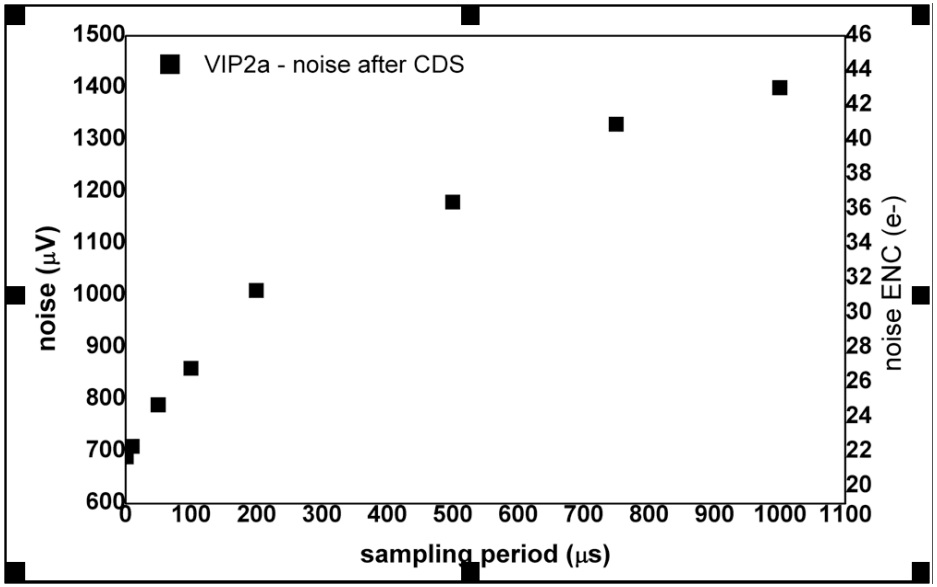


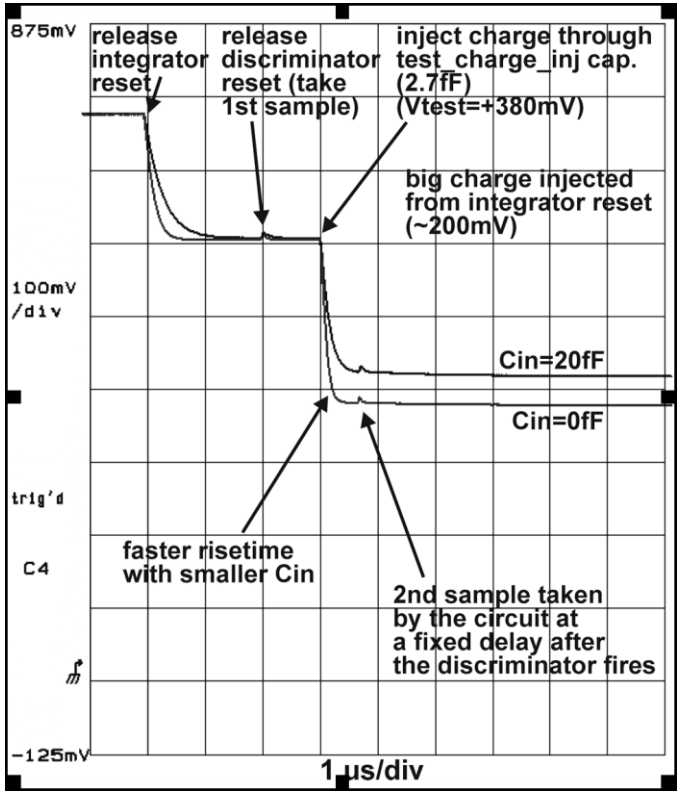
Analog Time Stamp ramp

VIP2a Front End

Double correlated sampling (fist sample at beginning of train)

- Good noise performance (20 fF simulated load, DCS with differential analog output, 1 us sample time, T_r=120 ns, I_b=0.5uA, Cs=100fF)
- Gain ~ 200 mV/fc at C_L = 20 fF





Full matrix tests underway

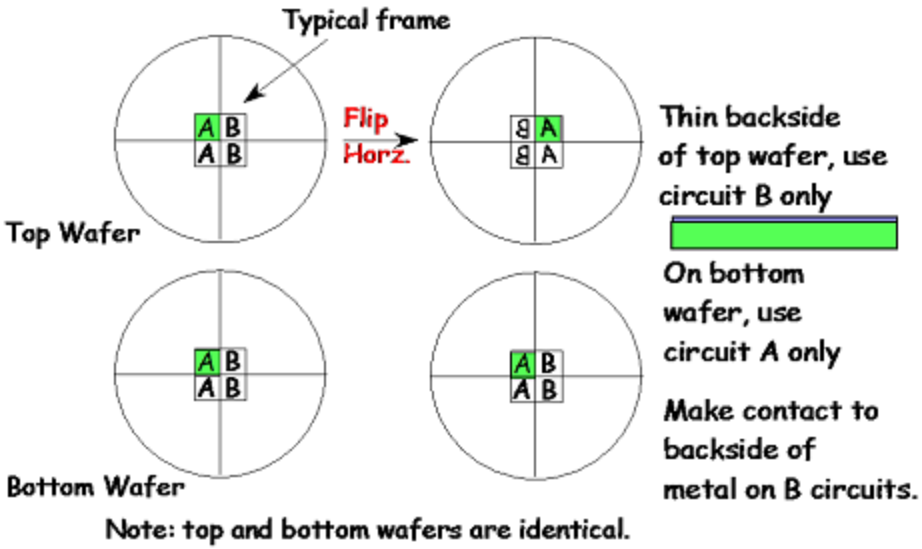
VIP2b

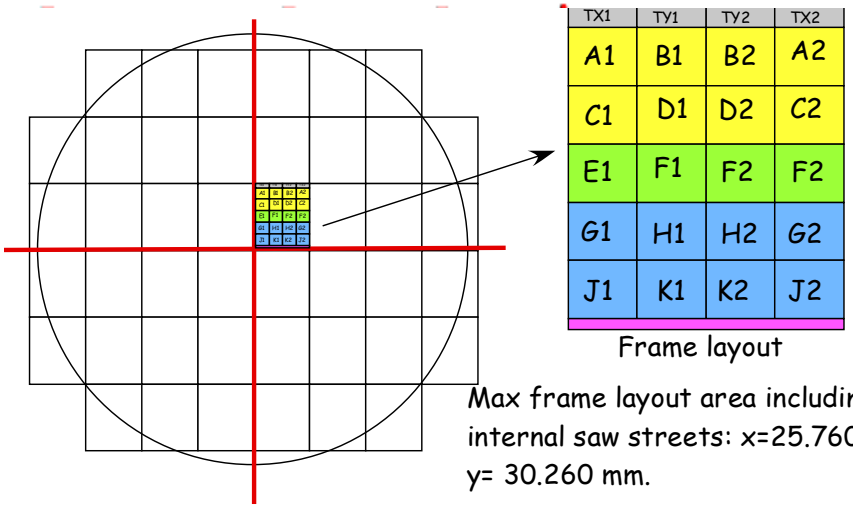
Functionally similar to VIP2a

- 2 Tiers of 0.13 μm CMOS
- 24 μm pixel pitch
- Will be integrated with detector using oxide bonding process

Multiproject run status

- Processing complete BUT the foundry did not center the reticule pattern on the wafer, making 3D bonding impossible
- Being rerun in "express line"
- 2D chip from misaligned run will be available this month for testing





Max frame layout area including internal saw streets: x=25.760 mm y= 30.260 mm.

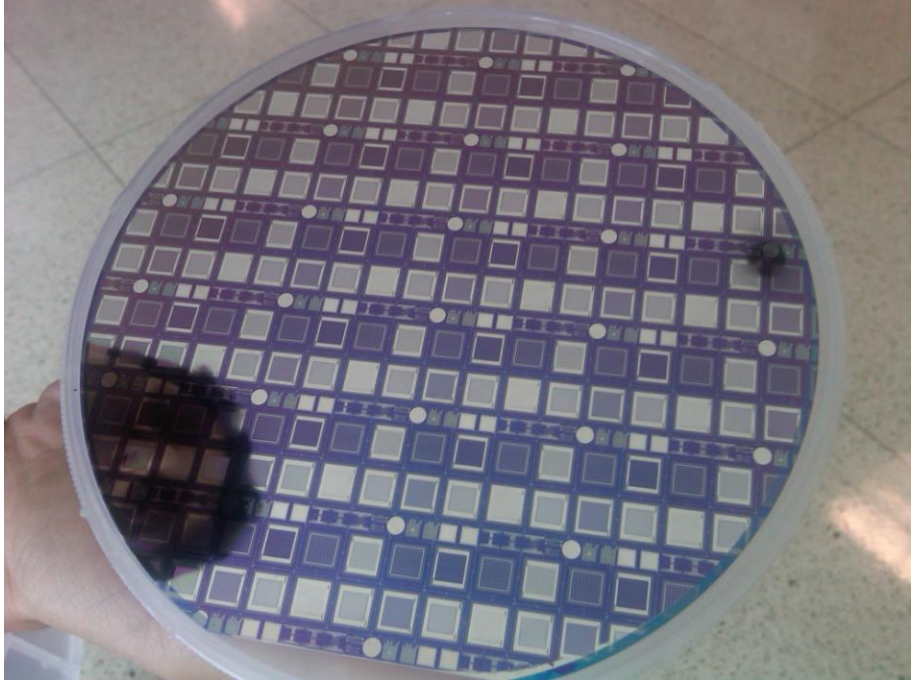
Wafer Map

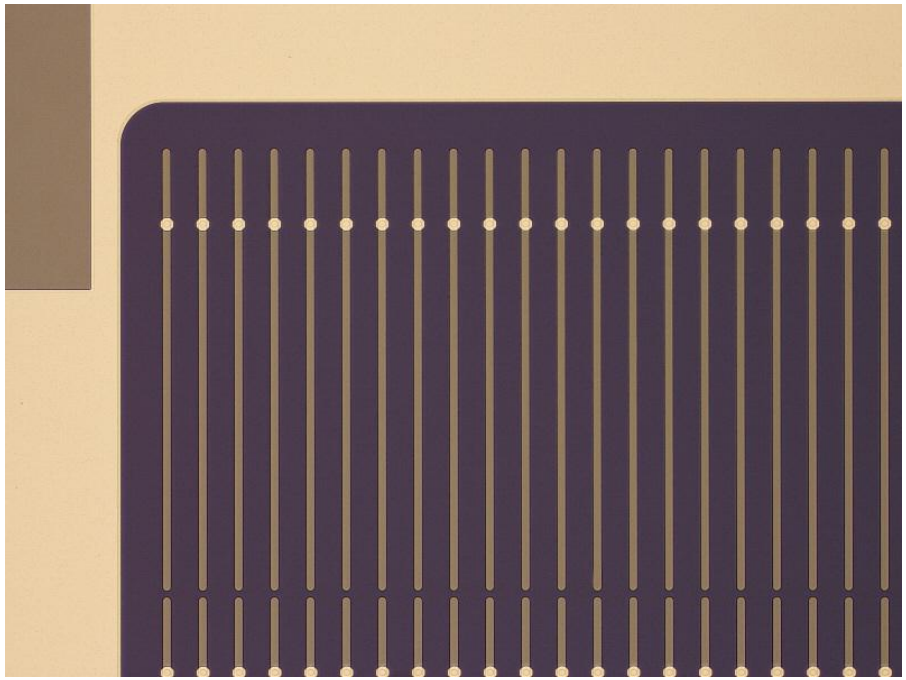
Sensor Integration

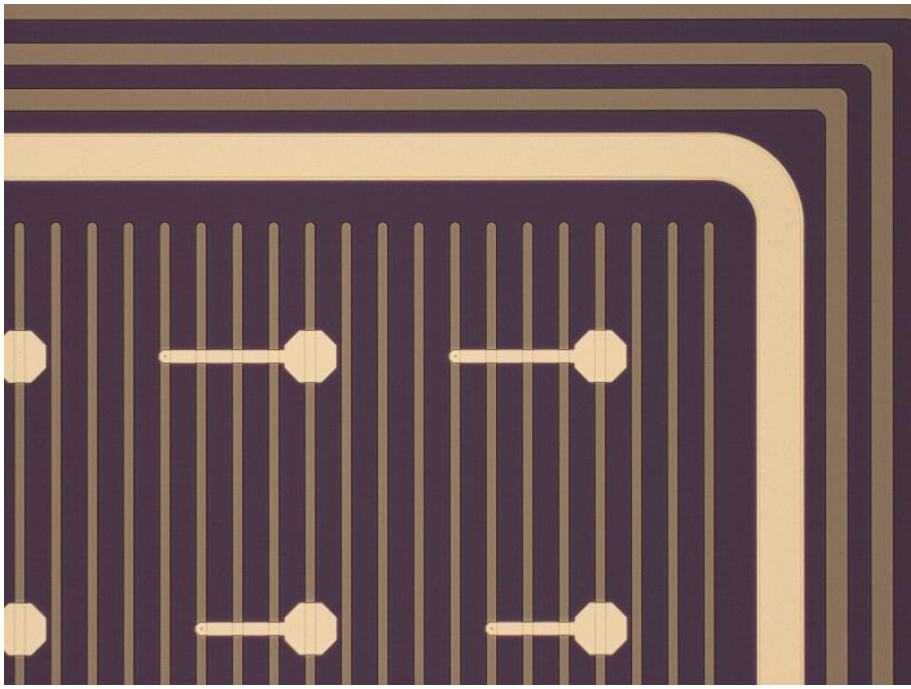
The first, pre-series set of sensors have been fabricated at BNL

- CV, IV, topography look good
- Two will be sent to Ziptronix to access planarity and topography
- One to FNAL for probe testing

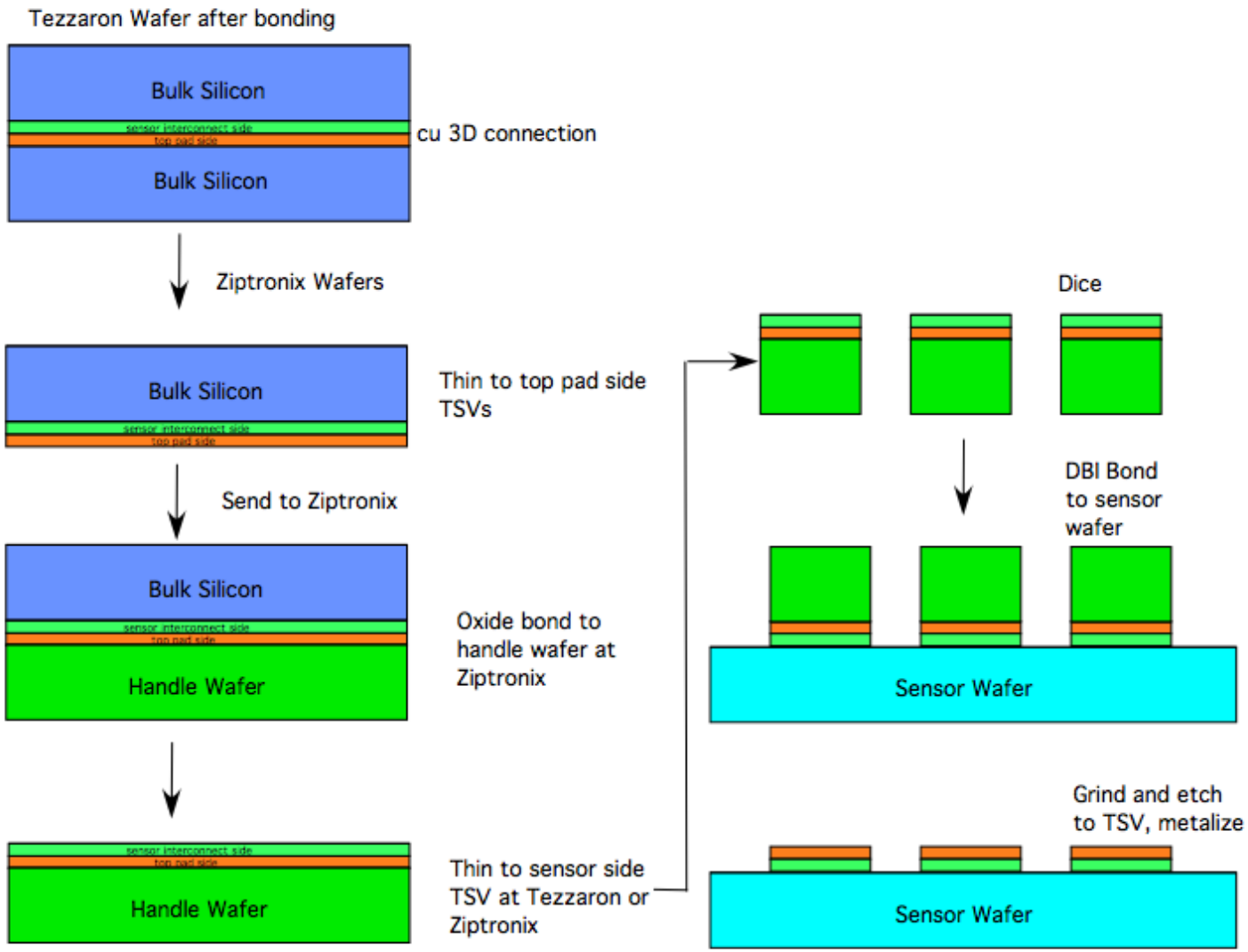
Second set for VIP integration will take 3-4 months







Detector Integration



3D Process Status

Good news - In June 2010, CMP/CMC/MOSIS partnered to offer a 3D-IC process

- Based on Tezzaron Super contact technology and Chartered/Global Foundries 130 nm CMOS process
- 2 tier face to face bonded wafers. Top tier is thinned to expose TSVs and backside metal added for wire bonding
- A design kit supporting 3D-IC design with standard cells and I/O libraries produced by CMP.

Bad news - Chartered to stop TSVs on 8 inch 0.13 CMOS wafers for the foreseeable future – IC industry is busy equipment moved to production lines

- Chartered agreed to process wafers from FEOL through M4
- Tezzaron will have SVTC add TSVs from M4 down into the substrate and complete the BEOL processing including the bond interface metalization
- Implication is that space will need to be left open on M1-M4 for the vias to pass through.
- Future potential benefit will be that wafers from other foundries can use the Tezzaron 3D process

Conclusions

- It appears that the VIP2a has solved most, if not all, of the problems encountered with VIP1.

- An established CMOS process is preferable to the MIT-LL process which is run on an R&D line.

- Development of the Tezzaron process and multiproject run has been a “learning experience”, however we are hopeful that wafers will be available this year and we can begin to test sensor integration with 3D ICs.