LePIX: monolithic detectors in advanced CMOS

K. KLOUKINAS, M. CASELLE, W. SNOEYS, A. MARCHIORO
CERN CH-1211, Geneva 23, Switzerland
A. RIVETTI, V. MANZARI, D. BISELLO, A. POTENZA, N. DEMARIA, M. COSTA, P. GIUBILATO
I.N.F.N.
A. DOROKHOV, C. HU, C. COLLEDANI, M. WINTER
IPHC Strasbourg
P. CHALMET, H. MUGNIER, J. ROUSSET
MIND-MicroTechnologies-Bât. Archamps
M. BATTAGLIA
UC Santa Cruz

LePIX

- Collaboration between CERN, IReS in Strasbourg, INFN, C4i-MIND in Archamps and interest from Imperial College, UC Santa Cruz, Rutherford

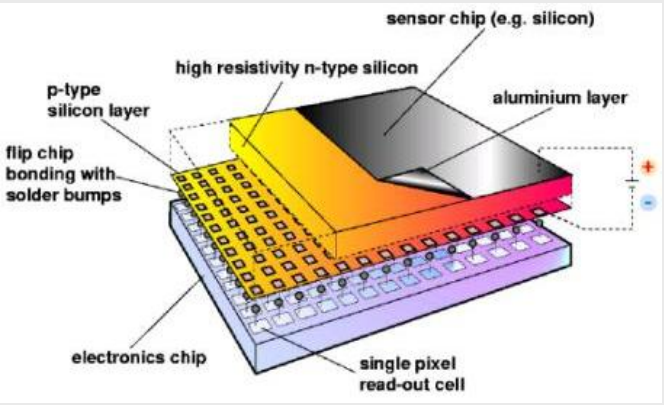
- Within INFN project funded by the R&D scientific committee (Torino, Bari, Padova), also help from UC Santa Cruz

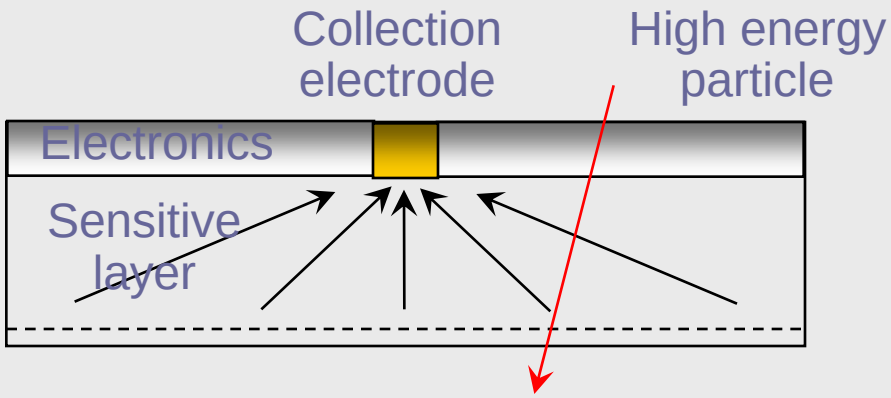
- C4i-MIND is financed by the Dept. de la Haute Savoie through a collaboration with CERN.

- CERN, IPHC, INFN and Imperial College participate in the prototype production cost

- CERN funding is from generic RD

LePIX: monolithic detectors in advanced CMOS





- Scope:
  - Develop monolithic pixel detectors integrating readout and detecting elements by porting standard 90 nm CMOS to wafers with moderate resistivity.
  - Reverse bias of up to 100 V to collect signal charge by drift
- Key Priorities:
  - Develop and optimize the sensor
  - Design low power (~ 1uW/pixel or less) front end electronics using low detector capacitance
  - Assessment of radiation tolerance
  - Assessment of crosstalk between circuit and detecting elements (may require special digital circuitry
- Need to carry development to a large matrix for correct evaluation

MOTIVATION

‘Traditional’ monolithic detectors:

non-standard processing on very high resistivity substrate

or

MAPS based with serial readout not necessarily always compatible with future colliders, and with collection by diffusion very much affected by radiation damage

Feedback from foundry that substrate sufficiently lowly doped is available in very deep submicron technologies (130 nm and beyond), 10 micron depletion no problem, strong perspectives to obtain significantly more (now even higher resistivity available !)

MOTIVATION

Exploiting very deep submicron CMOS to obtain:

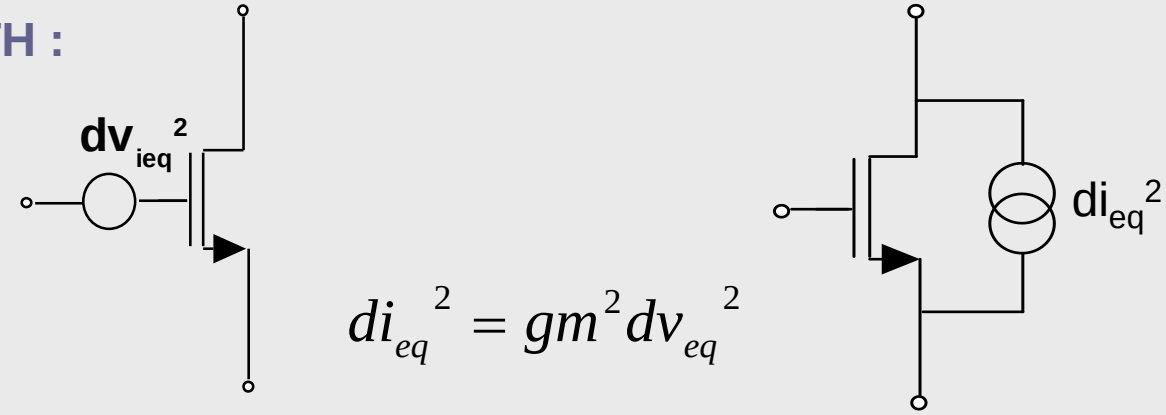
- Good radiation hardness (charge collection by drift).
- High speed: parallel signal processing for every pixel, time tagging at the 25ns level.
- Low power consumption: target 20 mW/cm^2 in continuous operation.
- Monolithic integration -> low capacitance for low power & low mass
- High production rate (20 m^2 per day…) and cost per unit area less than traditional detectors
- Low K dielectrics in the metal stack beyond 130 nm

OUTLINE

- Analog power, low capacitance and benefit of segmentation
- Device design
- Digital power and circuit architecture
- First submission: description and first results
- Conclusions

ANALOG POWER : NOISE IN A MOSFET

EQUIVALENT WITH :



$$di_{eq}^{\ 2} = gm^2 dv_{eq}^{\ 2}$$

WHERE :

$$dv_{eq}^{\ 2} = (K_F / (WLC_{ox}^{\ 2} f^{\alpha}) + 4kT\gamma / g_m)df \text{ in SI}$$

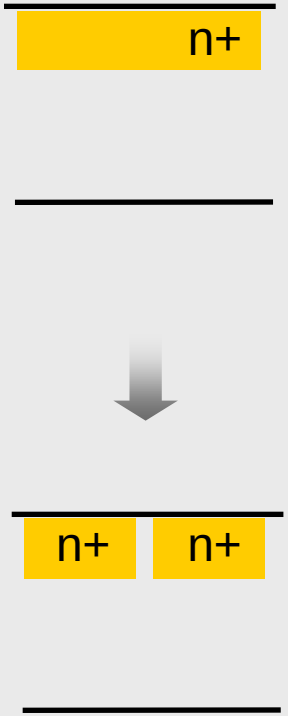
AND

$$dv_{eq}^{\ 2} = (K_F / (WLC_{ox}^{\ 2} f^{\alpha}) + 2kTn / g_m)df \text{ in WI}$$

$$\text{Noise} \sim \frac{1}{\sqrt{gm}} \sim \frac{1}{I^m} \text{ where } m < 1/2 \quad \text{Signal-to-Noise} \sim \frac{Q \times I^m}{C}$$

Weak dependence of the noise on current !

THE BENEFITS OF SEGMENTATION



Divide one detector element into two

- Collected charge remains the same
- Capacitance divided by 2 (up to a certain point)
- Power to obtain same signal to noise gets divided by at least a factor two due to the weak dependence of the noise on the current

S/N increases up to the point when:

- Charge is shared over more electrodes
- The decrease of the electrode capacitance slows down

Conclusion : segment until increase in S/N starts to saturate

For constant total power S/N increases with segmentation

$$\left[\frac{S}{N}\right]_{new} = \frac{Q(I/2)^m}{C/2} = 2^{(1-m)}\left[\frac{S}{N}\right]_{old} > \left[\frac{S}{N}\right]_{old} \quad m < 1/2$$

THE BENEFITS OF SEGMENTATION

Noise $\sim \frac{1}{\sqrt{gm}} \sim \frac{1}{I^m}$ where $m < 1/2$ Signal-to-Noise $\sim \frac{Q \times I^m}{C}$

Strong dependence of the current on the noise !

For constant signal to noise

Current I per channel : $I^{-m} \sim \frac{Q}{C}$ or $I \sim (C/Q)^{2\ldots4}$

Weak…Strong inversion

Segmentation

Number of elements N, C~1/N: Total analog Power ~ $N(C/Q)^{2\ldots4} \sim (1/N)^{1\ldots3}$

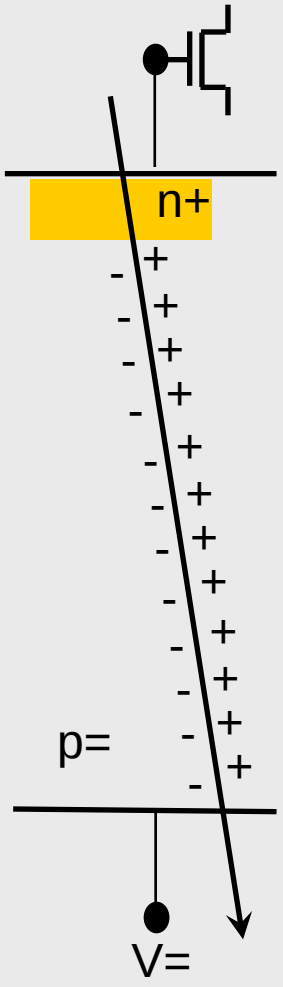
Higher segmentation is (very) good

Decreased depletion layer thickness -> need to segment in proportion

Xd ÷ 2 -> C ÷ 2

For constant signal-to-noise, the analog power decreases with segmentation (will saturate at high segmentation) !

LOW C for ANALOG POWER



Take transistor noise at 40 MHz BW for 1 uA
(1uA/100x100 um pixel = 10 mW/sq cm)

$$Veq \approx 0.16mV$$

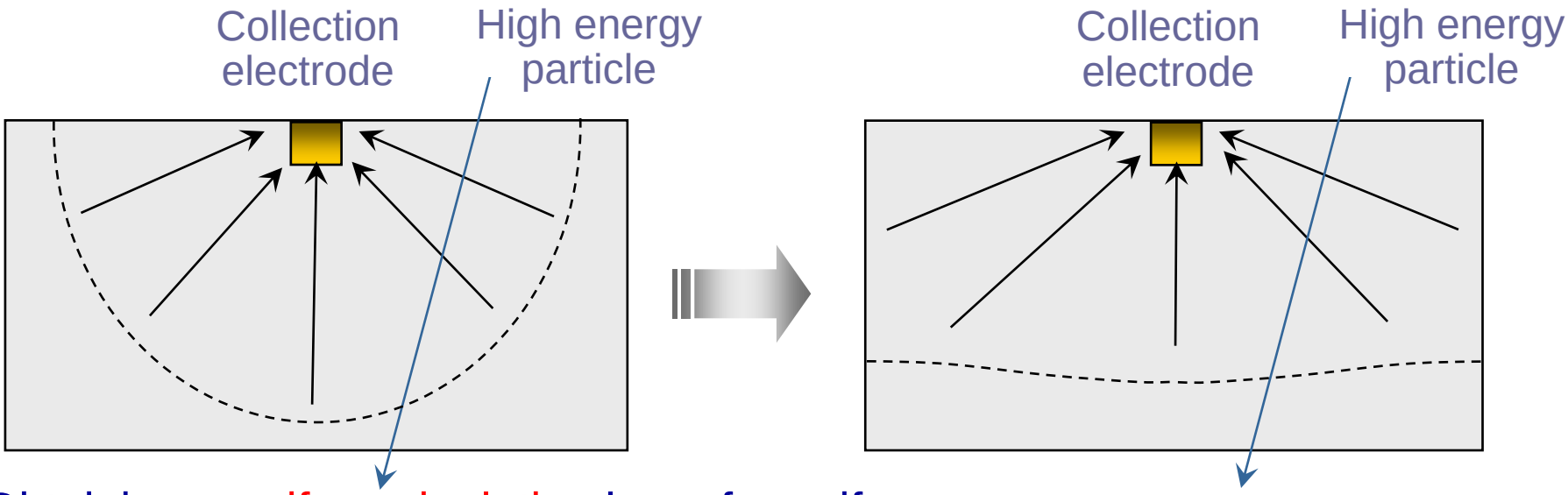
$$\frac{S}{N} = 25 \Rightarrow \frac{Q}{C} = 4mV \quad \boxed{= \frac{4\,fC}{1pF}} \quad \boxed{= \frac{0.4\,fC}{0.1pF}} \quad \boxed{= \frac{0.04\,fC}{10\,fF}}$$

Collection depth 300 μm 30 μm 3 μm

If more signal available or lower capacitance can take advantage to obtain lower power

Valid for monolithic and non-monolithic approach !

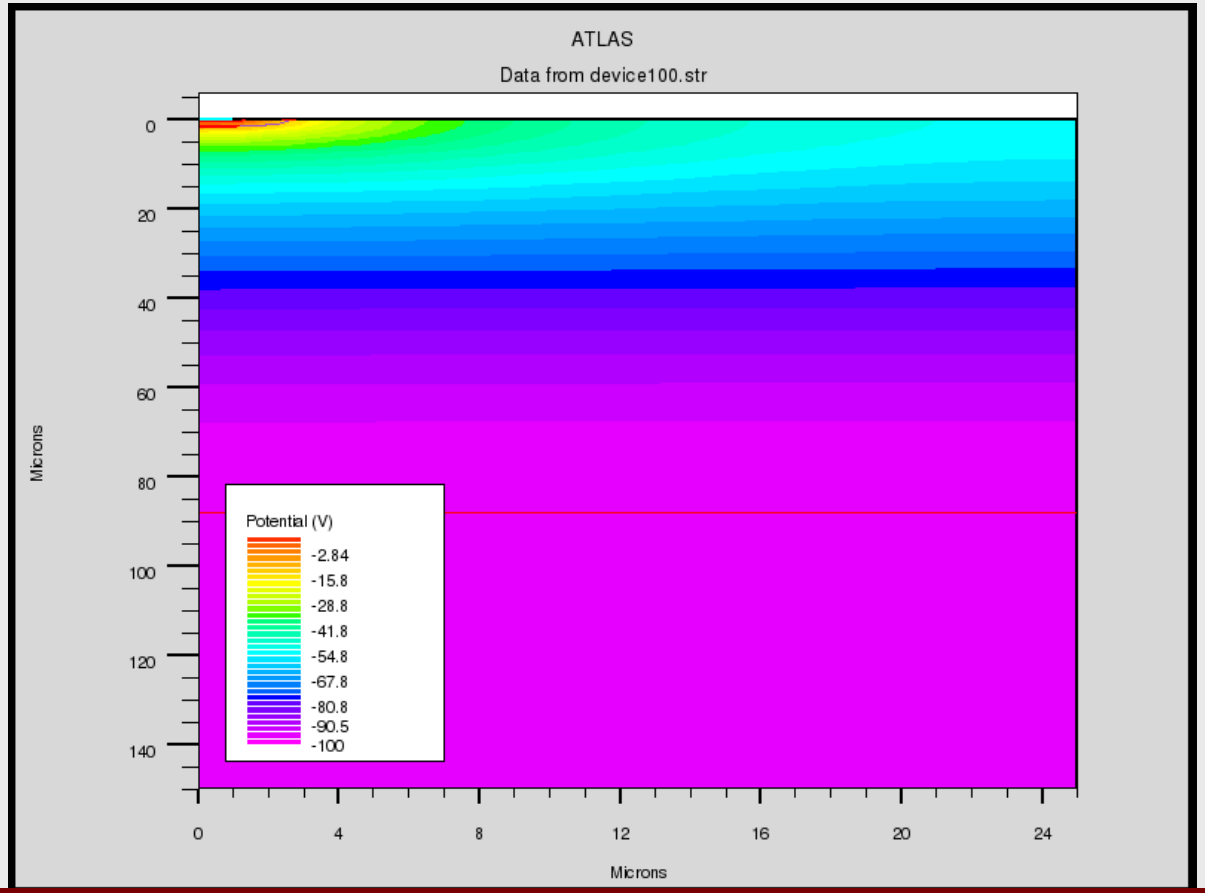
Device design challenge: uniform depletion layer with a small collection electrode



- Obtaining a uniform depletion layer for uniform response
- Optimal geometry and segmentation of the read-out electrode (Minimum C)
- Effective charge resetting scheme robust over a large range of leakage currents
- Pattern density rules in very deep submicron technologies very restrictive.
- Insulation of the low-voltage transistors from the high voltage substrate.

Sensor needs to be designed in close contact with the foundry!

Device design challenge: uniform depletion layer with a small collection electrode



✓Pixel pitch used in this 2D simulation was 50 μm.

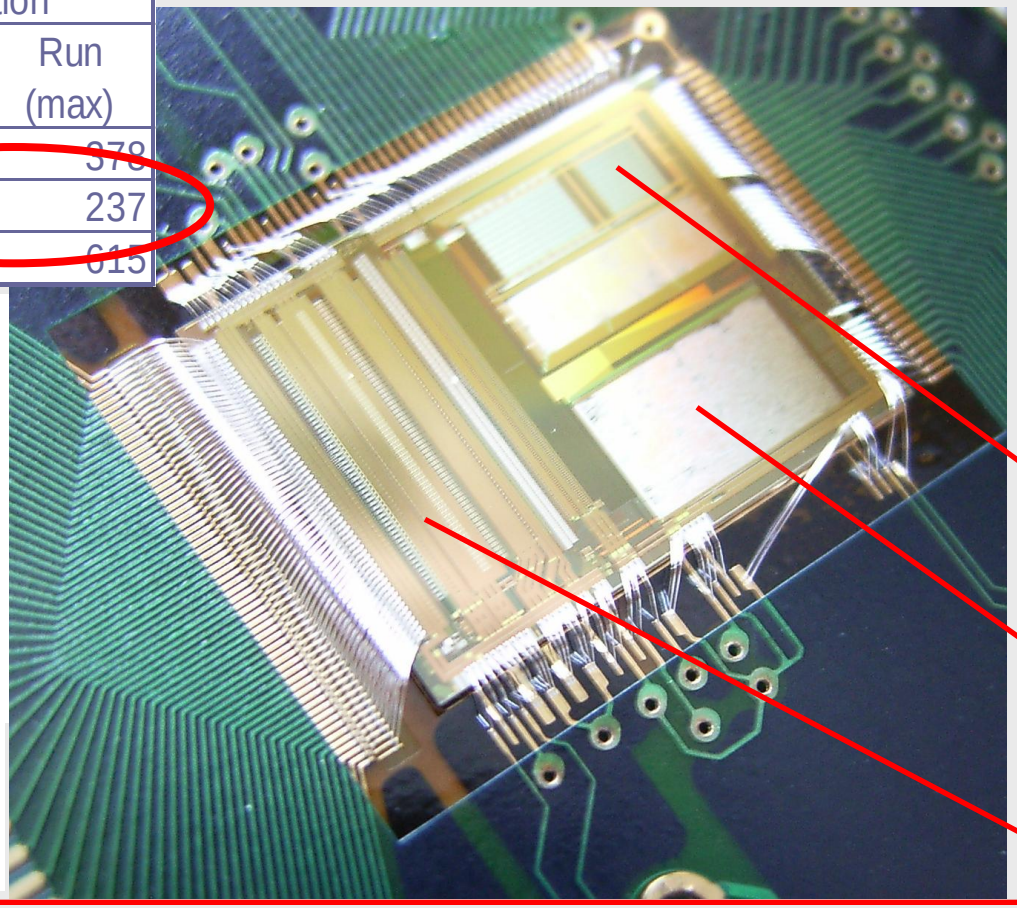
✓For highest resistivity substrate 80 μm depletion with 100 V

Digital power consumption has to optimized as well !!
Example TOTEM VFAT chip

VFAT power consumption			
(mW)	Sleep	Run (nominal)	Run (max)
Analog	33	378	378
Digital	135	194	237
Total	168	572	615

VFAT sends digital data to GOH hybrid, which serializes and optically transmits this data

P. Aspell et al. TWEPP 2007



Designers :
Paul Aspell
Giovanni Anelli
Walter Snoeys
Herve Mugnier
Jan Kaplon
Kostas Kloukinas
Pierre Chalmet

CERN C4i

Data treatment and memories

Slow Control Registers

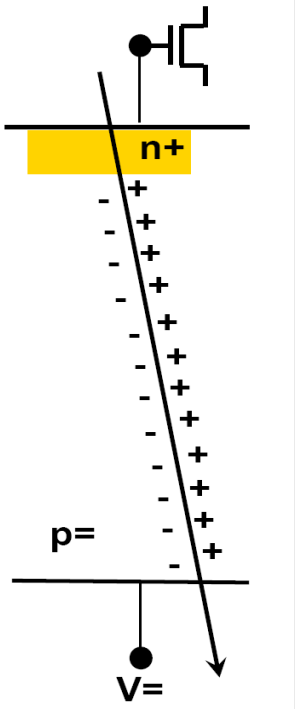
Frontend

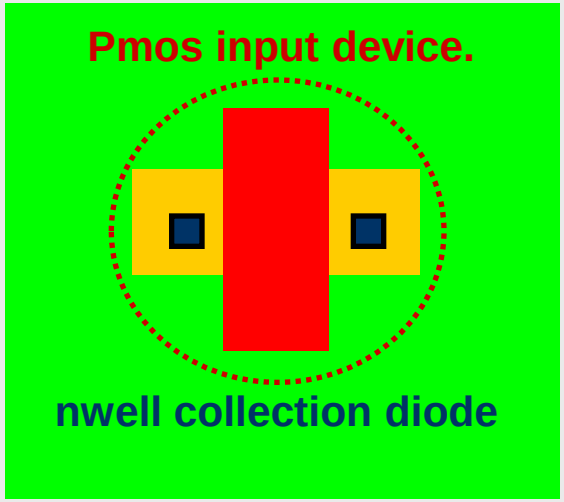
128 channels of tracking front end with digital storage and data transmission
8 programmable trigger outputs, designed for radiation tolerance

CIRCUIT ARCHITECTURE

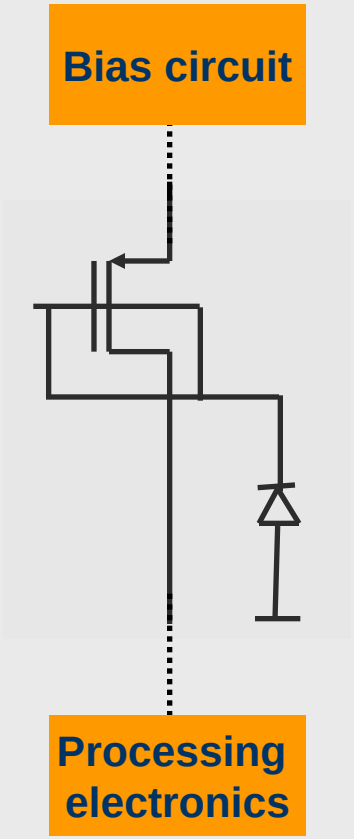
- Most of the collection electrode capacitance to ground (or at least not to the neighboring pixel) -> no capacitive channel-to-channel cross-talk
- Use open loop amplifier (like MAPS), but need time tagging at the 25ns level
- Distributing the clock to every pixel will cost significant power 10fF*10000 elements in one square cm at 40MHz 1V swing = 4mW per square cm already
- Therefore use analog power to send signal to the periphery
-

CIRCUIT ARCHITECTURE



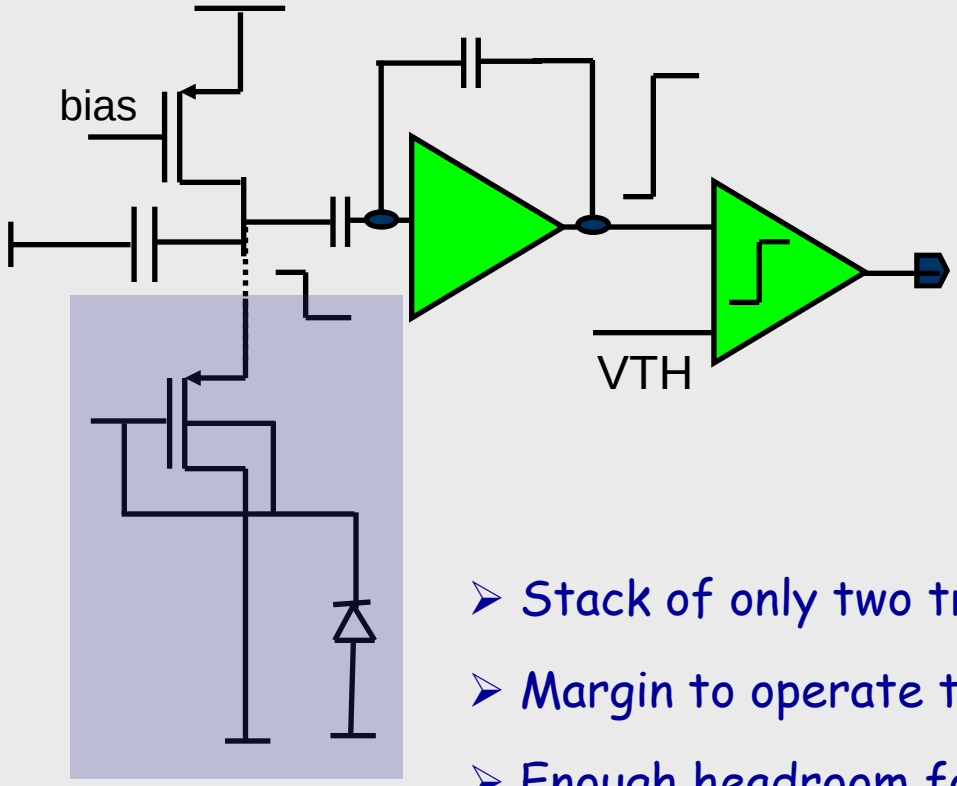


- Charge to voltage conversion on the sensor capacitance
- For 30 μm depletion and 10fF capacitance: 38 mV for 1 mip.



- ✓ Only one PMOS transistor in the pixel (or maybe very few…)
- ✓ Each pixel is permanently connected to its front-end electronics located at the border of the matrix.
- ✓ Each pixel has one or two dedicated lines: need of ultra fine pitch lithography => 90 nm CMOS.

For first submission: voltage output front end



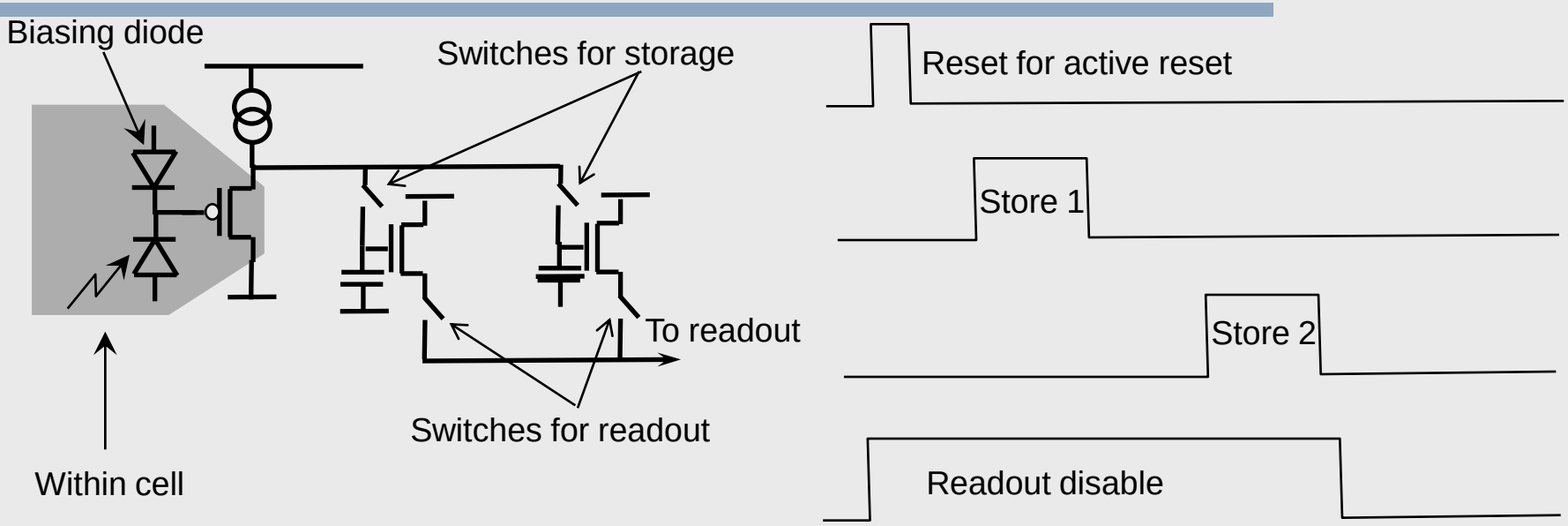
✓ The current signal is converted to a voltage step by integration on the input parasitic capacitance (~ 10 fF).

✓ The voltage step is sensed at the source and fed to a preamplifier-shaper-discriminator chain .

- Stack of only two transistors.
- Margin to operate the sensor at low power supply (0.6 V).
- Enough headroom for leakage induced DC variations.

- Only one external line per pixel.
- The rise time of the signal, but not its final amplitude sensitive to the parasitic capacitance of the line.

Other type of readout used in first submission robust against detector leakage



① Can store analog value twice, once after reset (bias diode can be replaced by reset transistor) and once a bit later. The difference between the two values is the signal collected in that time interval.

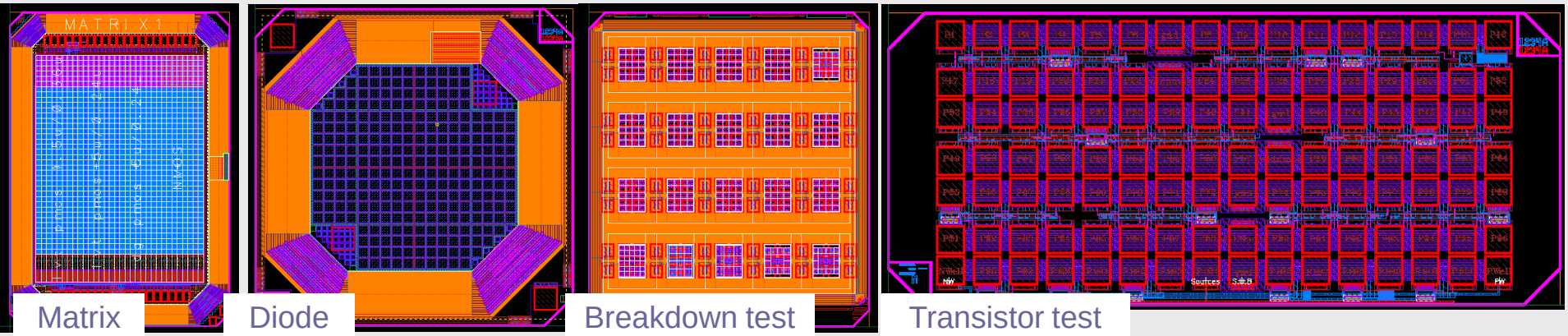
② This storing is done for all elements in the matrix in parallel.

③ Afterwards both values for all pixels are readout sequentially.

④ This mechanism allows to externally control the sensitive period independently of the readout.

LePIX: SUBMISSION FOR FABRICATION

- Non-standard: ESD protection, special layers, mask generation, guard rings
- Received chips on standard substrate, put lot on high resistivity on hold
- 7 chips submitted :
  - 4 test matrices
  - 1 diode for radiation tolerance
  - 1 breakdown test structure
  - 1 transistor test: already submitted once in test submission

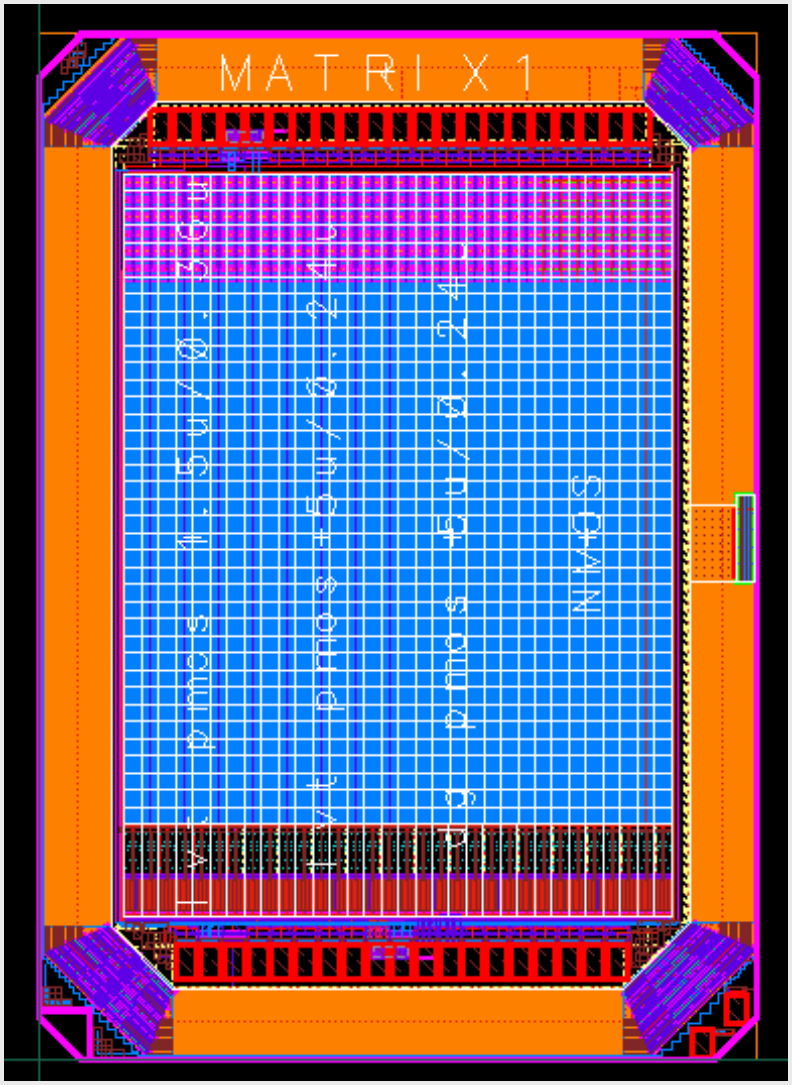


Matrix 1 | Diode | Breakdown test | Transistor test

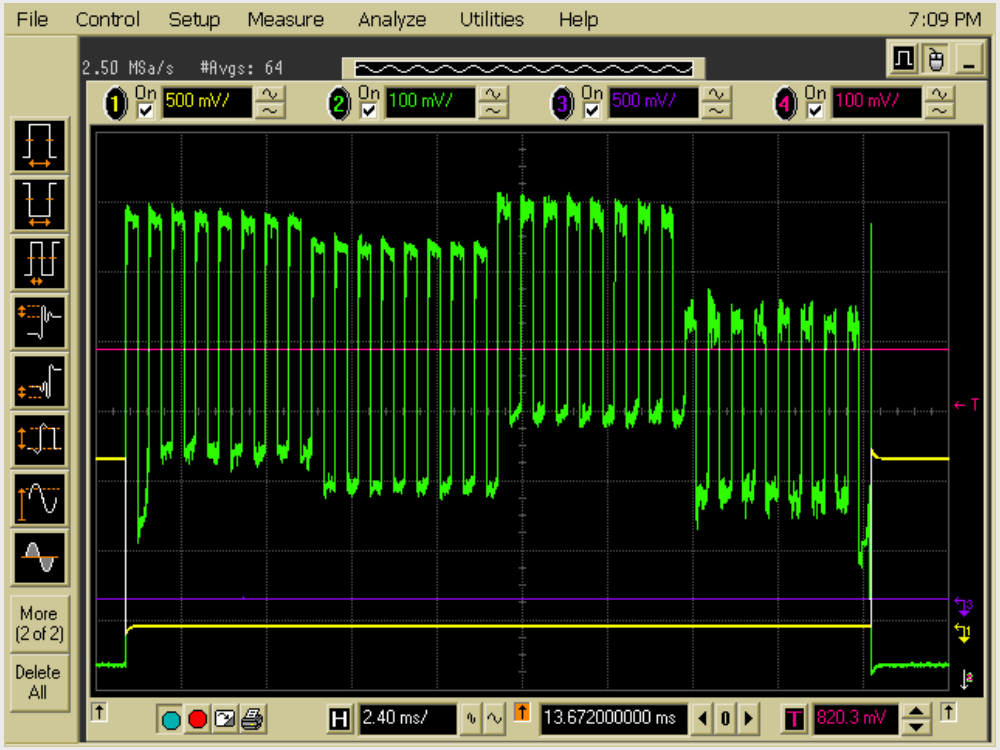
The bad news: short due to mask generation issue

- The guard ring received p+ implant creating a short (which transforms into a ~80 ohm resistor due to series resistance)
- Discovered on standard substrate, exists on all structures (4 matrices, diode and breakdown structure)
- Lot on high resistivity on hold before this step, discussion with foundry on fix.
- In the mean time trying to learn as much as possible from lot on standard substrate.

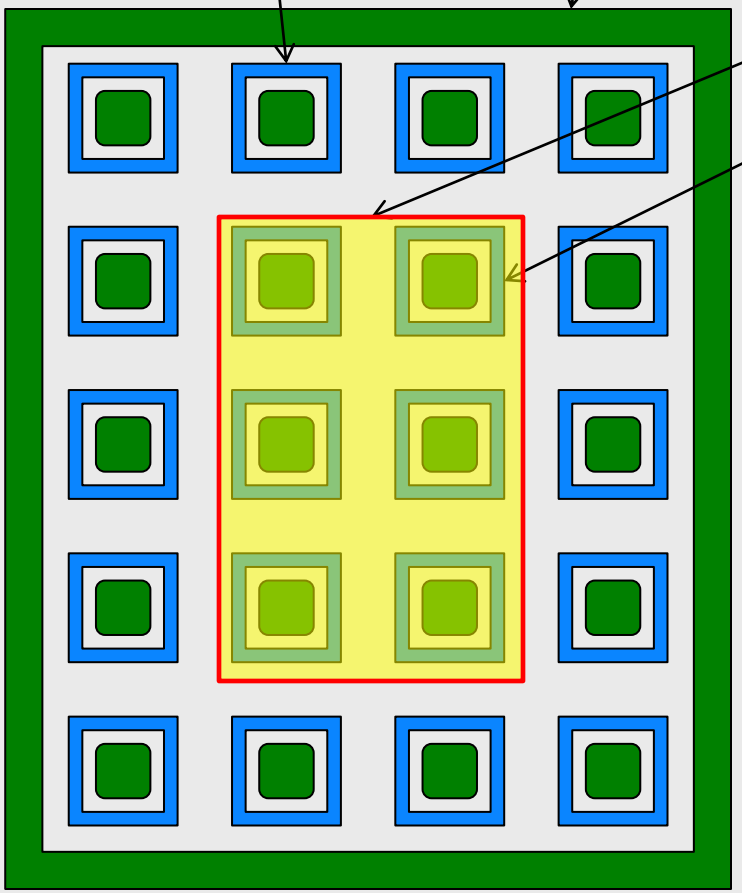
The good news: circuitry of first matrix 1 operational

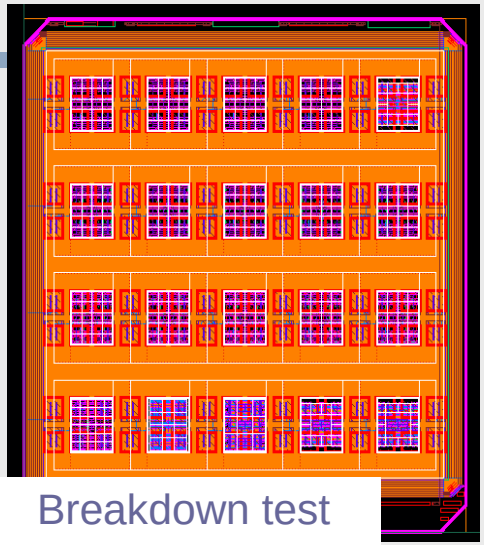


- 4 zones of 8 columns with different input transistor clearly visible
- Difference between active and diode reset



Measurement on breakdown structure

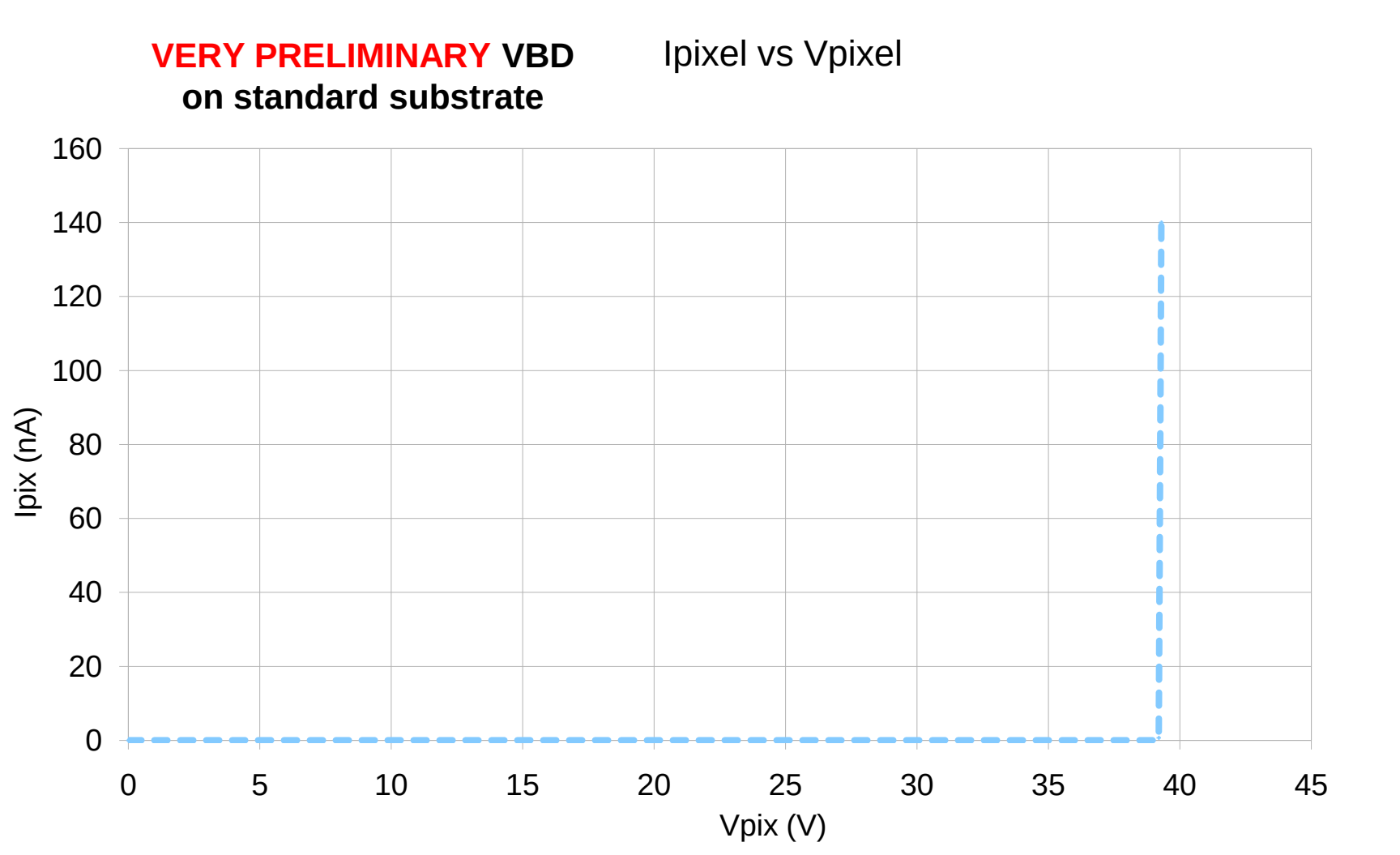




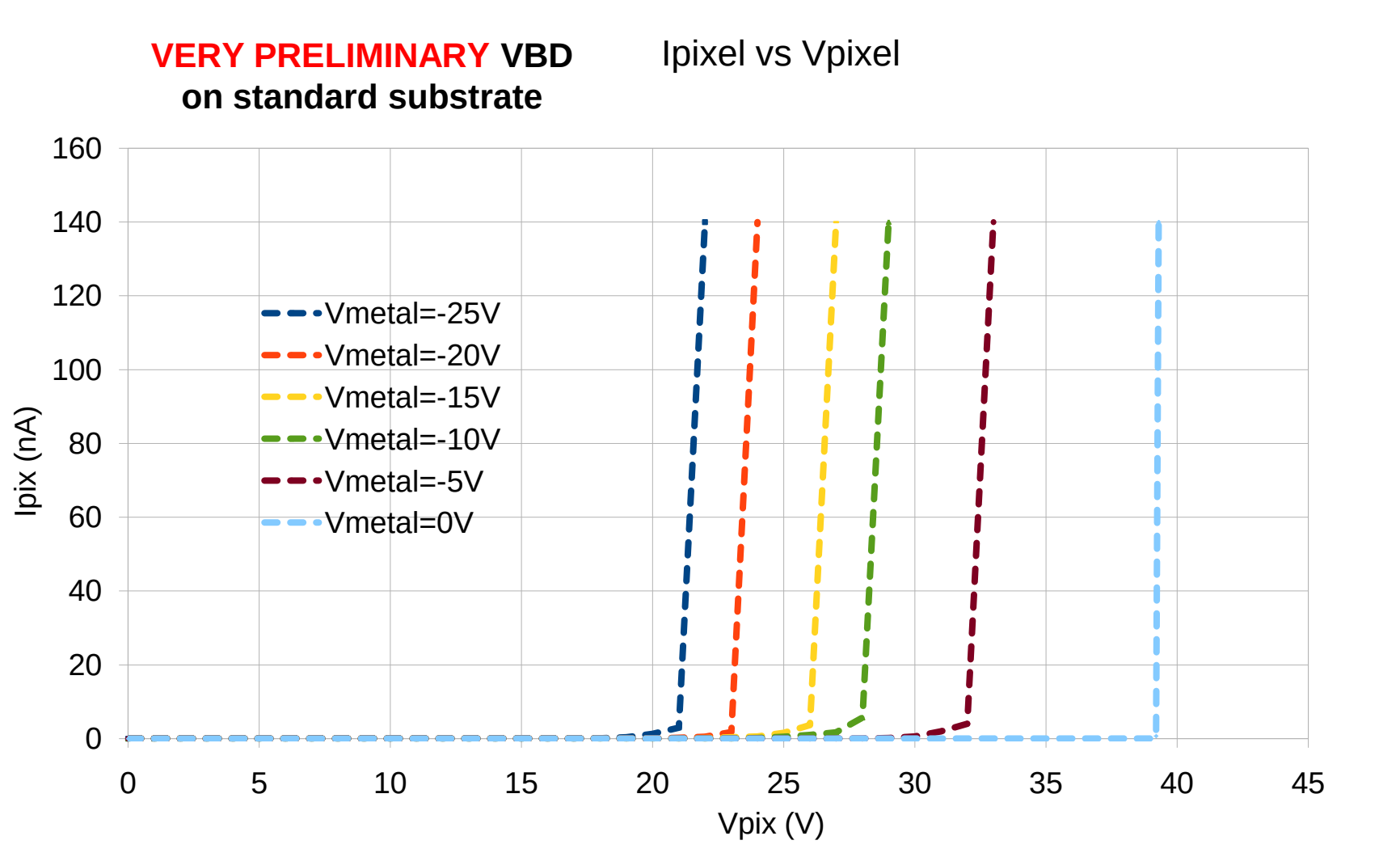
Breakdown test

- Same problem with guard here, but the central pixels can be reverse biased alone maintaining the guard at the same potential as the substrate
- The test structure contains a matrix of 2x3 pixels surrounded by a ring of pixels and guard, schematically represented on the left.

Breakdown > 30 V … on standard substrate, close to expected value for planar junction



Can be modulated using metal gate



CONCLUSIONS

- LePIX tries to exploit very deep submicron CMOS on moderate resistivity:
  - Radiation hardness (charge collection by drift).
  - Low power consumption: target 20 mW/cm^2 in continuous operation.
  - Monolithic integration -> low capacitance for low power & low mass (needs work on digital part to fully take advantage of the gain in the analog)
  - High production rate (20 m^2 per day…) and cost per unit area less than traditional detectors
- Power consumption will be key.
- Breakdown voltage > 30V promising
- First submission has shown the exercise is not easy, proof of principle not before next year.

THANK YOU