Silicon Tracking System Status

ILD Software & Integration Workshop 2010

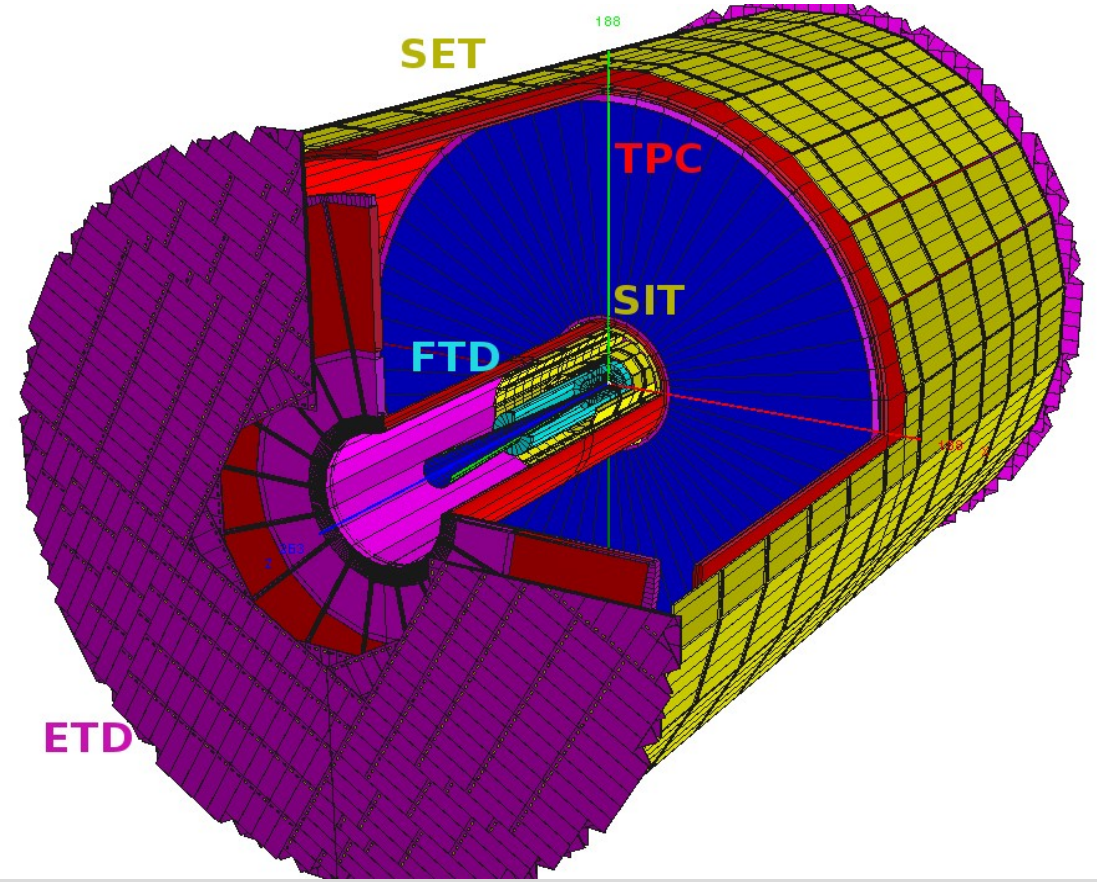
Alexandre Charpy
Konstantin Androsov

Full Geometry Description

Full description of the silicon tracker in the ILD concept

Goal:
- transition IlcRoot to Mokka with many improvements
- developping the mechanical structure according the workshop meeting (ILD inner region integration meeting)

- SIT (HEPHY - INFN Turin - KEK - Korea – LPNHE)
- SET (INFN Turin - LPNHE)
- ETD (LPNHE)
- FTD (IFCA-IFIC)



SiLC Framework

Main Goals:

- Generate different kind of geometry very easily (number of silicon layers, false/true double-sided, technology …) => automation
- Optimization of the geometry for physics studies (b-tagging, vertexing ...)
- Possibility to introduce mis-alignement studies according a mechanical structure
- Materiel budget effects induce by the support
- Customization for specific request (ILD ...)

Inputs:

- XML configuration
- Mokka Database

SiLC Framework

<u>Design concept</u>

- Split the forward and the barrel region

- Both are created into several steps
  - build the silicon module
  - build the super-module
  - build the layer
  - build a detection element
  - build the sub-detectors

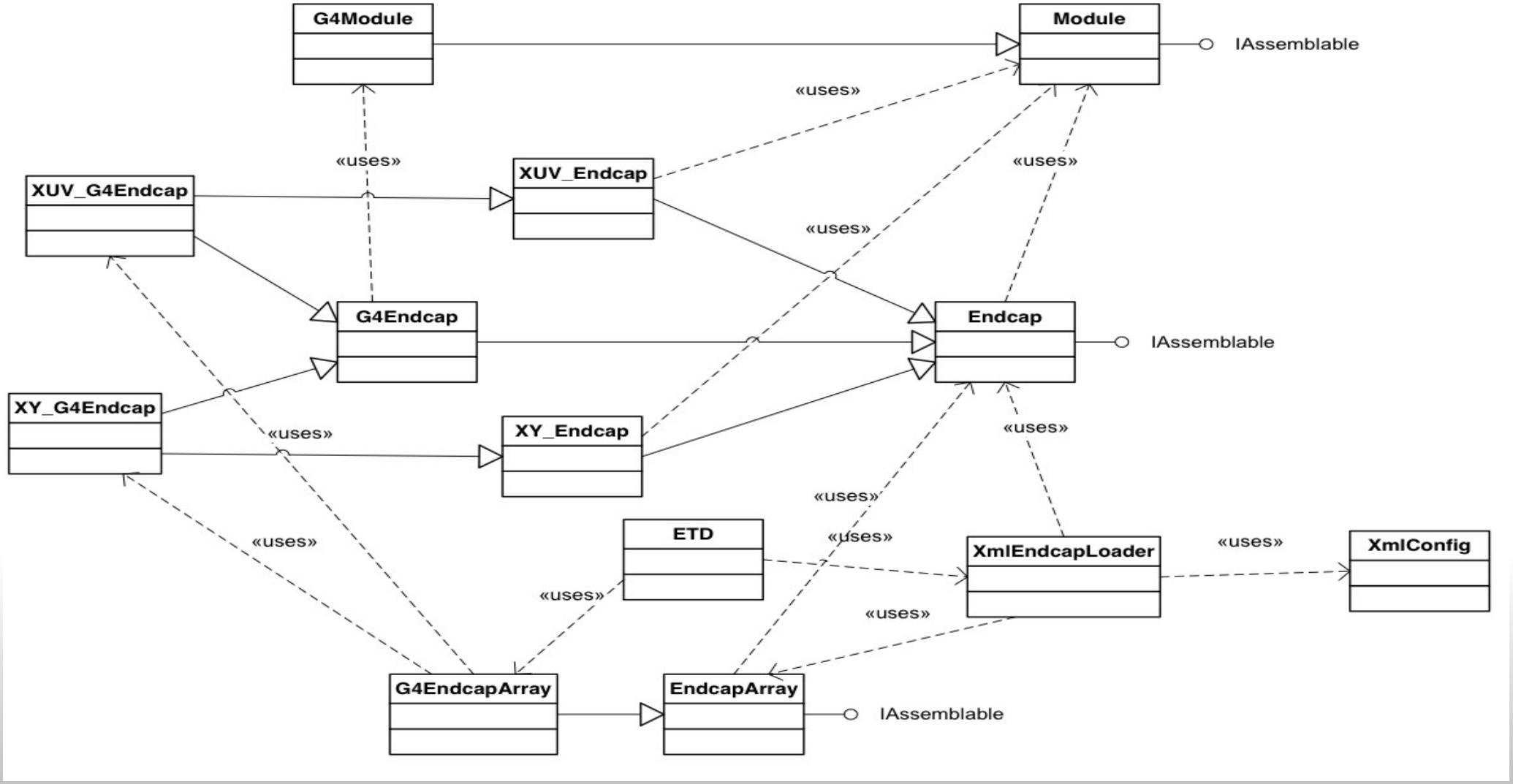
=> generic hierachy in the volume → misalignement studies ?

- Supports/cables builder could be disconnected to the active area builder

- Flexibility -> Interface to create dedicated geometry trough virtual methods

SiLC Framework

Partial design pattern



SiLC Framework

Example of application

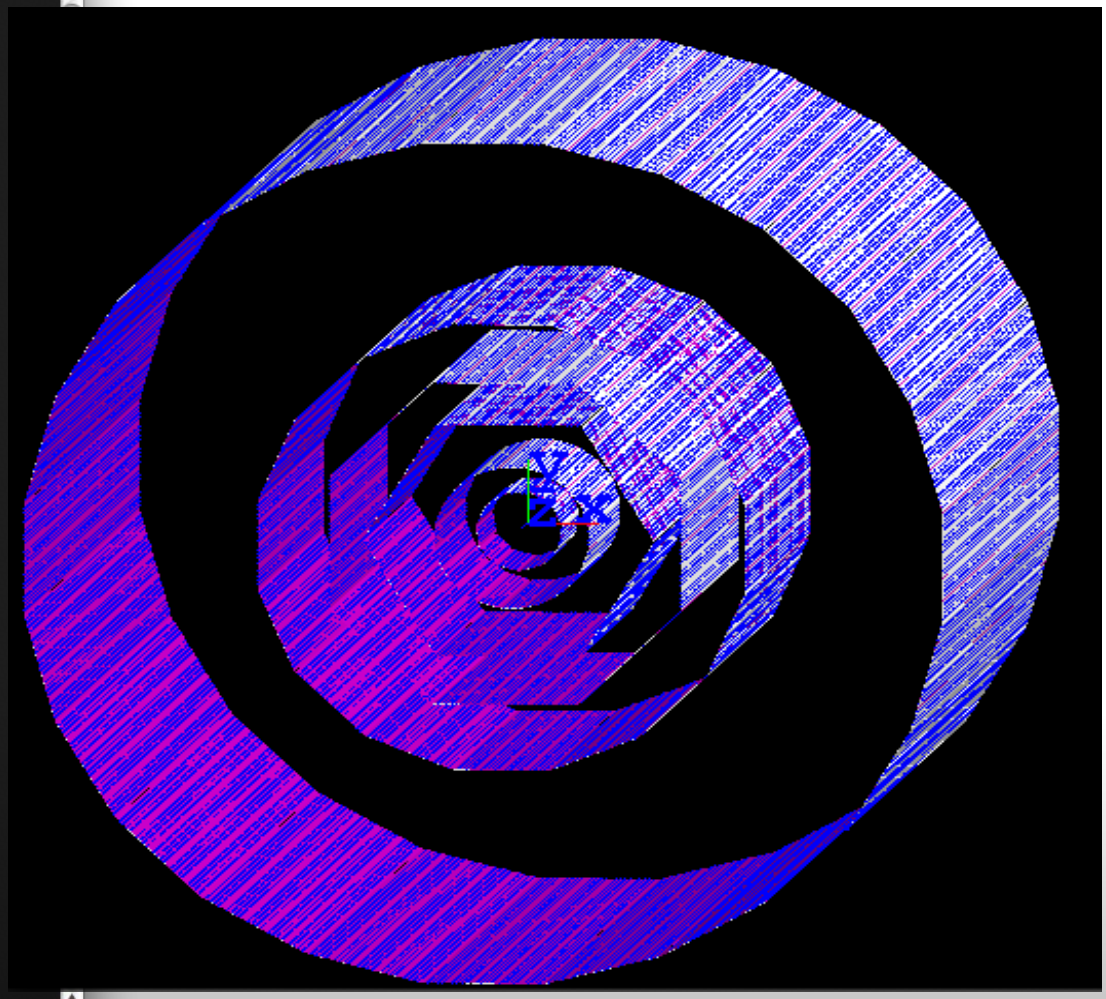
Terminal — emacs-i386 — bash — ⌘4

```xml
<?xml version="1.0" encoding="UTF-8"?>
<!-- All dimension are in mm-->
<GeomParam>
  <ConceptName>SiLC</ConceptName>
  <BarrelConfig>
    <NbBarrels>5</NbBarrels>
    <NbLayers>5</NbLayers>
    <Barrel id="0" name="Sit1">
      <!-- General information -->
      <BarrelParam>
        <BarrelShape>cylinder</BarrelShape>
        <NbFace>0</NbFace> <!-- Only need for polygon shape-->
        <RadiusMin>165</RadiusMin>
        <ZLength>642</ZLength>
        <NbSection>1</NbSection>
        <SupportType>v1</SupportType>
      </BarrelParam>
      <!-- Module information -->
      <ModuleParam>
        <SensorTechnology>strip</SensorTechnology>
        <SensorSize splitId="1" layer="0" dimx="101.2" dimy="101.2" dimz="0.15"/>
        <NbSensor isplitId="1" layer="0" x="1" y="1"/>
        <Chip nbchips="16" nbchannel="128" chiprow="4" dimx="10." dimy="5." dimz="0.3."/>
        <ModuleDirection splitId="1" layer="0" phi="0." theta="0." psi="0."/>
        <ModuleShift splitId="1" layer="0" x="0." y="0." z="0."/>
      </ModuleParam>
      <!-- Chip Information -->
      <ChipParam>
        <NbChannelsPerChip>128</NbChannelsPerChip>
        <NbChips>16</NbChips>
        <ChipNbRow>4</ChipNbRow>
        <ChipSize splitId="1" dimx="10." dimy="5." dimz="0.3."/>
      </ChipParam>
    </Barrel>

    <Barrel id="1" name="Sit2">
      <!-- General information -->
      <BarrelParam>
        <BarrelShape>cylinder</BarrelShape>
        <NbFace>0</NbFace> <!-- Only need for polygon shape-->
        <RadiusMin>309</RadiusMin>
        <ZLength>1290</ZLength>
        <NbSection>1</NbSection>
```

-uuu:---F1 **sit02.xml** Top L1 SVN:7 (XML)----------

Loading vc...done



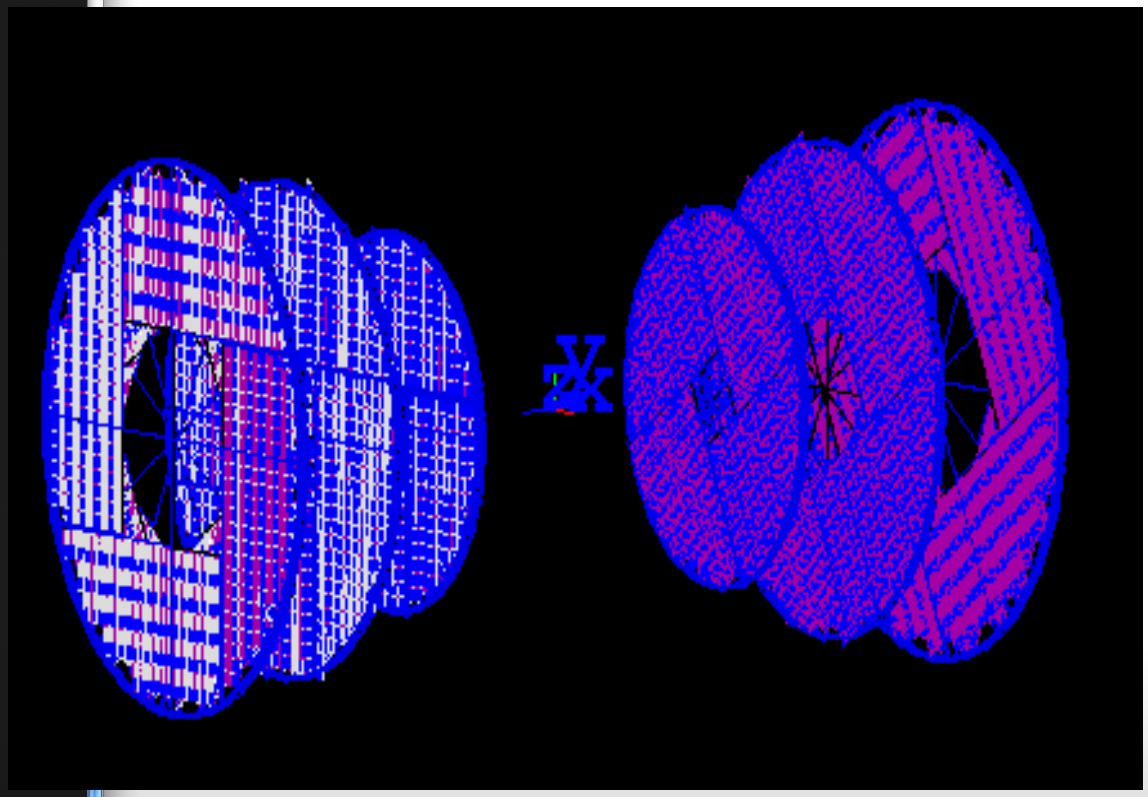
SiLC Framework

Example of application

Terminal — emacs-i386 — bash — ⌘4

```
<?xml version="1.0" encoding="UTF-8"?>
<!-- All dimension are in mm-->
<BeamParam>
    <ConceptName>SiLC</ConceptName>
        <EndcapsConfig>
                <NbEndcaps>3</NbEndcaps>
                <NbLayers>9</NbLayers>
                <Endcap id="0" name="Etd">
                        <!-- General information -->
                        <EndcapType>XUV_ILD</EndcapType>
                        <InnerRadius>200</InnerRadius>
                        <OuterRadius>1300</OuterRadius>
                        <ZPosition>1500</ZPosition>
                        <NbZone>1</NbZone>
                        <ZoneConfig id="0" angle="-1">
                                <!-- Module information -->
                                <ModuleParam>
                                        <SensorTechnology>strip</SensorTechnology>
                                        <SensorSize splitId="1" layer="0" dimx="101.2" dimy="101.2" dimz="0.15"/>
                                        <NbSensor isplitId="1" layer="0" x="1" y="1"/>
                                        <Chip nbchips="16" nbchannel="128" chiprow="4" dimx="10." dimy="5." dimz="0.3."/>
                                        <ModuleDirection splitId="1" layer="0" phi="0." theta="0." psi="0."/>
                                        <ModuleShift splitId="1" layer="0" x="0." y="0." z="0."/>
                                        </ModuleParam>
                                </ZoneConfig>
                        </Endcap>

                <Endcap id="1" name="Etd">
                        <!-- General information -->
                        <EndcapType>XUV_ILD</EndcapType>
                        <InnerRadius>400</InnerRadius>
                        <OuterRadius>1700</OuterRadius>
                        <ZPosition>2500</ZPosition>
                        <NbZone>1</NbZone>
                        <ZoneConfig id="0" angle="-1">
                                <!-- Module information -->
                                <ModuleParam>
                                        <SensorTechnology>strip</SensorTechnology>
                                        <SensorSize splitId="1" layer="0" dimx="101.2" dimy="101.2" dimz="0.15"/>
                                        <NbSensor isplitId="1" layer="0" x="1" y="1"/>
                                        <Chip nbchips="16" nbchannel="128" chiprow="4" dimx="10." dimy="5." dimz="0.3."/>
                                        <ModuleDirection splitId="1" layer="0" phi="0." theta="0." psi="0."/>
                                        <ModuleShift splitId="1" layer="0" x="0." y="0." z="0."/>
                                        </ModuleParam>
-uuu:---F1  etd01.xml     Top L1    SVN:1  (XML)----------------------------------------------------------------
Loading vc...done
```



SiLC Framework for ILD concept

Baseline:

- LOI

SIT characteristics (current baseline = false double-sided Si microstrips)					
Geometry			Characteristics		Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	Time [ns]	RL[%]
165	371	0.910	R: σ=7.0,	307.7 (153.8)	0.65
309	645	0.902	z: σ=50.0	σ=80.0	0.65

SET characteristics (current baseline = false double-sided Si microstrips)					
Geometry			Characteristics		Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	Time [ns]	RL[%]
1833	2350	0.789	R: σ=7.0,	307.7 (153.8)	0.65
1835	2350	0.789	z: σ=50.0	σ=80.0	0.65

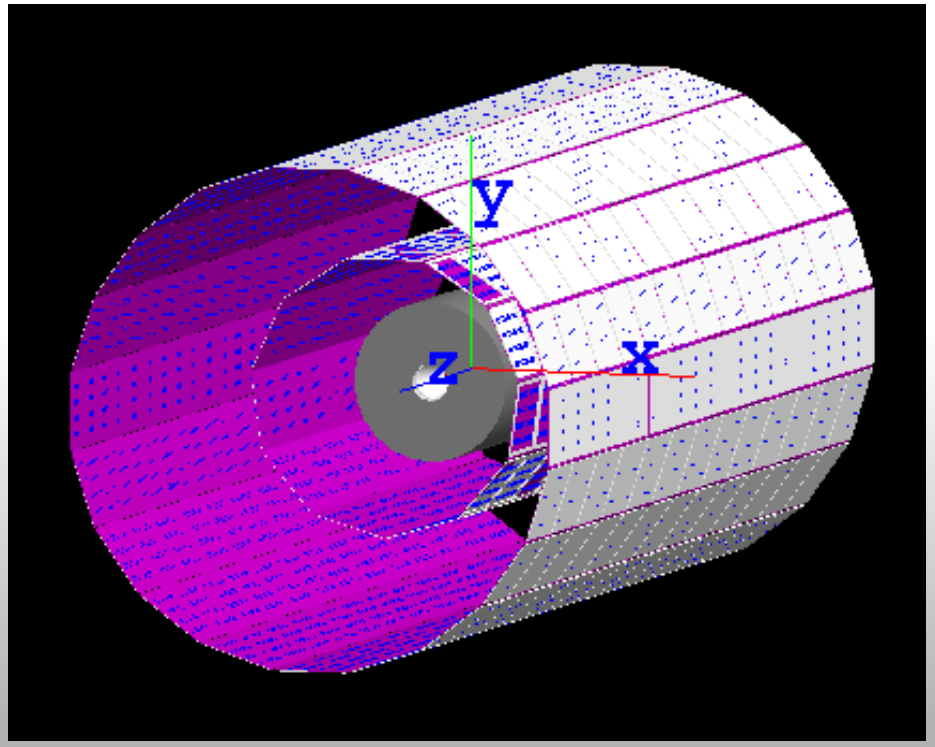
- Silicon modules (will change according the results of next silicon tests)
  - sensors of 10.12*10.12 mm2, edge-less technology
  - 2048 strip, 50 microns pitch, 200 microns of thickness
  - 16 SiTr read-out chips + one level concentrator + optical fiber output
  - power supply: kapton cable

Silicon Inner Tracker (SIT)

LOI data

SIT characteristics (current baseline = false double-sided Si microstrips)					
Geometry			Characteristics		Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	Time [ns]	RL[%]
165	371	0.910	R: σ=7.0,	307.7 (153.8)	0.65
309	645	0.902	z: σ=50.0	σ=80.0	0.65

From Simulation



Simple layer with false double sided with 6° angle - Cf A.Savoy-Navarro

Minimum Radius (mm)	Maximum Radius (mm)	Z Length (mm)
172.3	179.6	708.4
319.5	323.5	1315.6

Number of modules along Z	Number of modules along φ
7	11
13	20

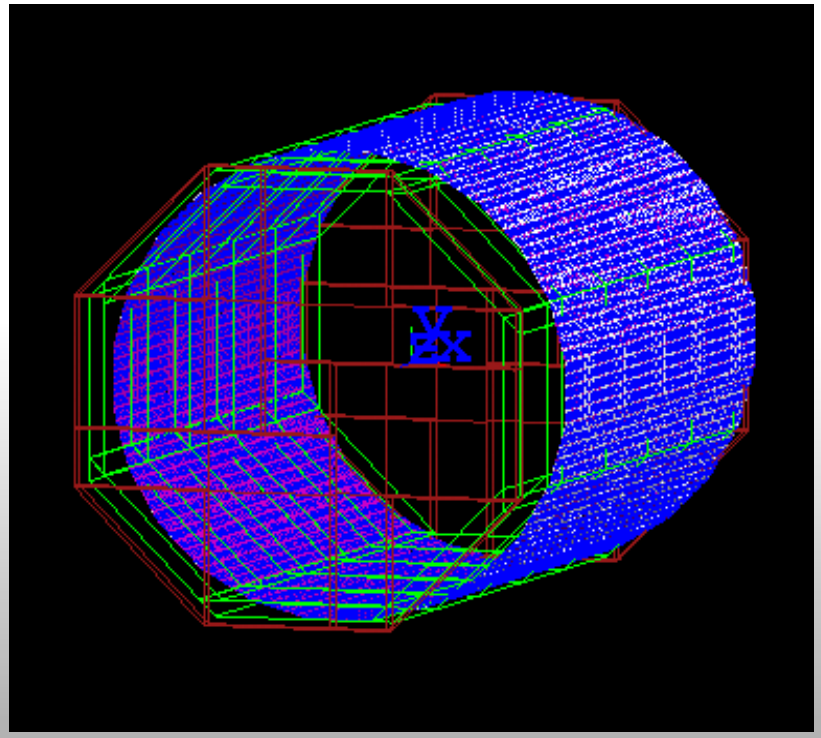
Support under mechanical studies

Silicon External Tracker (SET)

LOI data

SET characteristics (current baseline = false double-sided Si microstrips)					
Geometry			Characteristics		Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	Time [ns]	RL[%]
1833	2350	0.789	R: σ=7.0,	307.7 (153.8)	0.65
1835	2350	0.789	z: σ=50.0	σ=80.0	0.65

From Simulation



Simple layer with false double sided with 6° angle - Cf A.Savoy-Navarro

Number Of Super Module	Number of modules along Z	Number of modules along φ
24	48	120

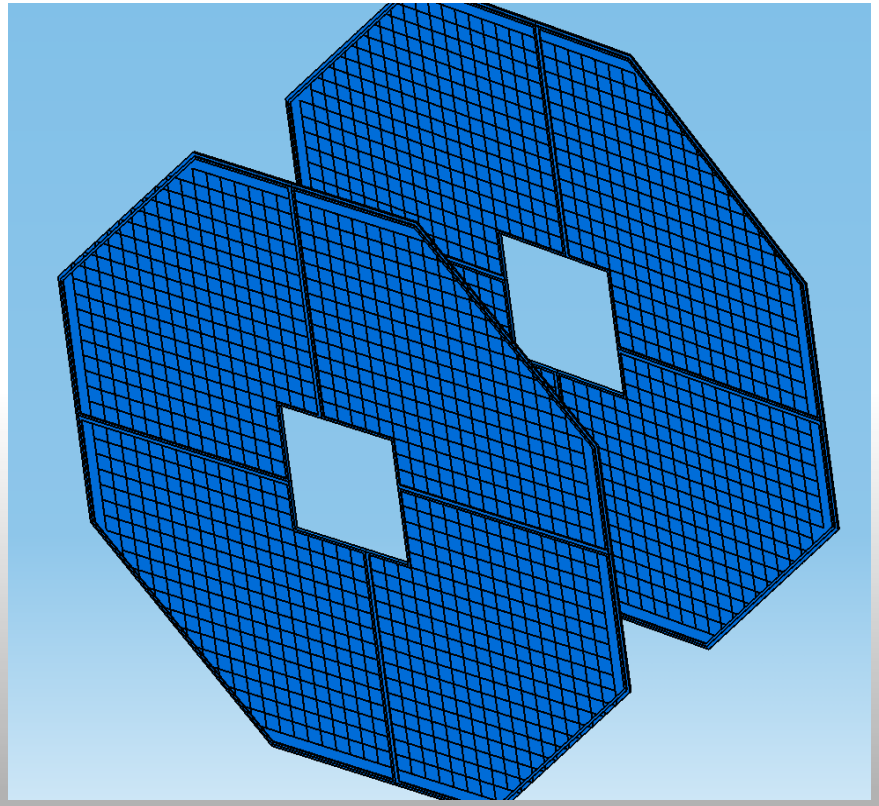
Minimum Radius (mm)	Maximum Radius (mm)	Z Length (mm)
1921 mm	1938 mm	4857 mm

Support under mechanical studies

Endcap Tracking Detector (ETD)

LOI data

ETD characteristics (current baseline = single-sided Si micro-strips, same as SET ones)				
Geometry			Characteristics	Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	RL[%]
419.3-1822.7	2426	0.985-0.799	x:σ=7.0	0.65
419.3-1822.7	2428	0.985-0.799	y:σ=7.0	0.65
419.3-1822.7	2430	0.985-0.799	z:σ=7.0	0.65



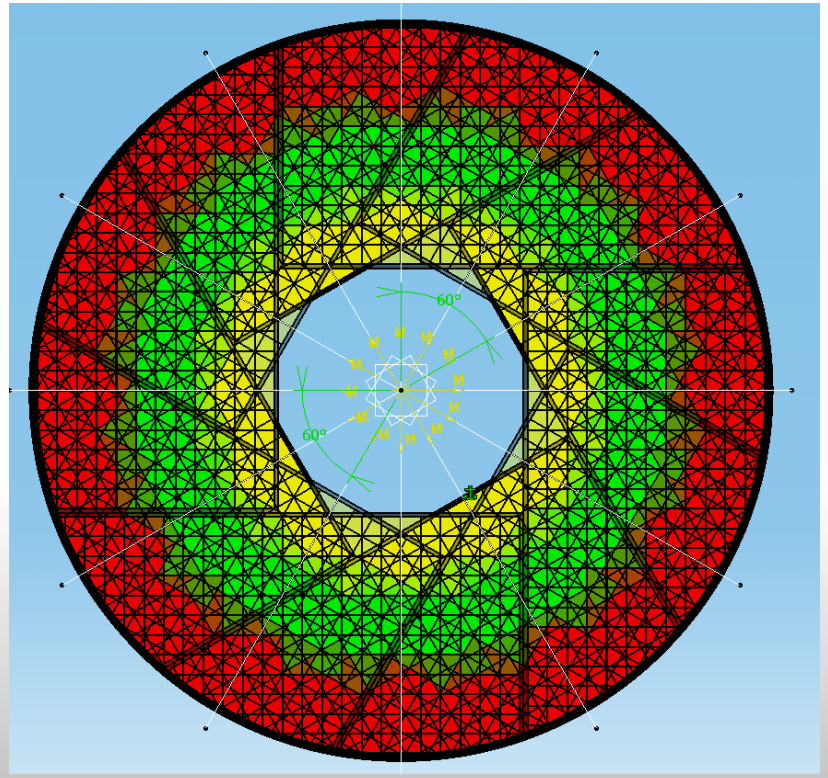
Multiple ETD versions:
- XUV version
- one layer of double sided sensors with stereo-angle
- and one more

-> the limits are strictly fixed by the ECAL endcaps
=> need to evaluate the surface of non active area, make many adjustments and study effect on the reconstruction

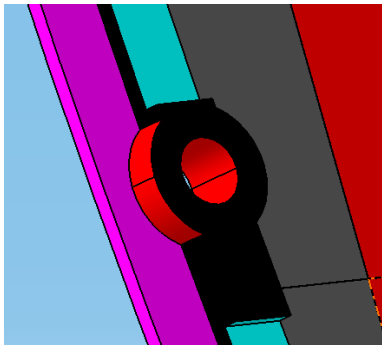
Endcap Tracking Detector (ETD)

<u>XUV concept</u>

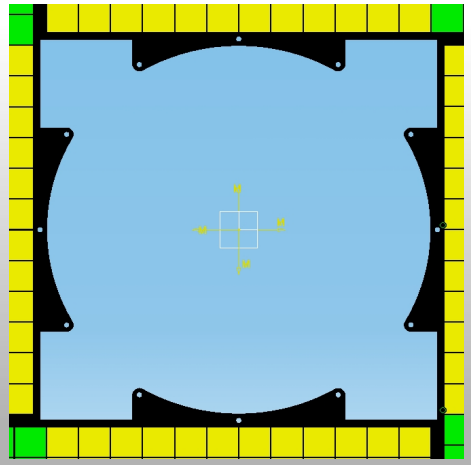
- pixels is required at forward rapidity
- Small details have to be completed

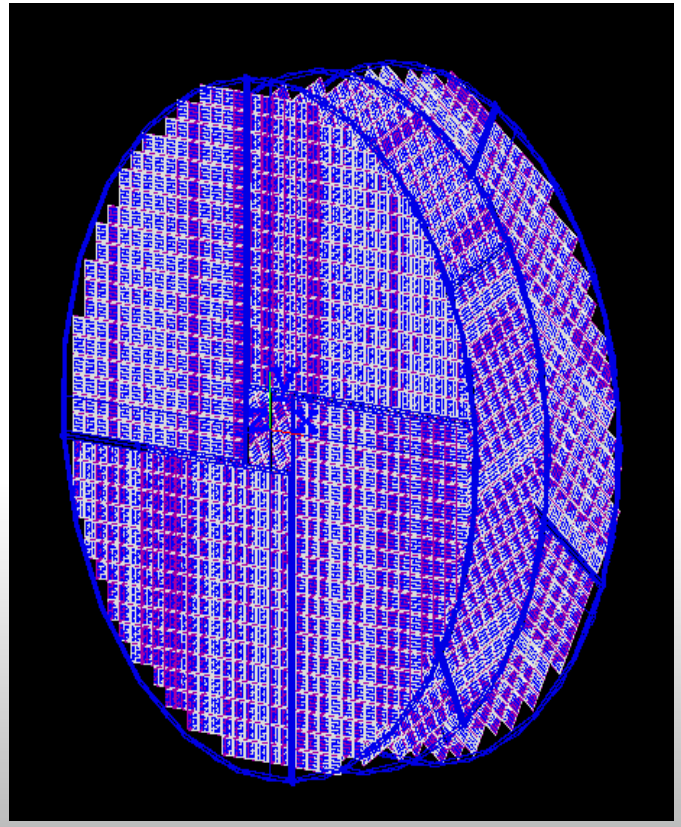


CATIA



to





GEANT 4

Silicon Tracking System Status

Overview

TODO list

- Check the overlapping for different configurations and fix the exceptions
- Creation and link with the Mokka database (thanks to Paulo Mora de Freitas)
- Manual writing (important)
- Complete the mechanical structure and the cable path according the dedicated engineers

- Commit of the source code under a SiLC directory

Expected End of July

- For reconstruction: what is required ?
- Link with the digitization

Thanks for your attention