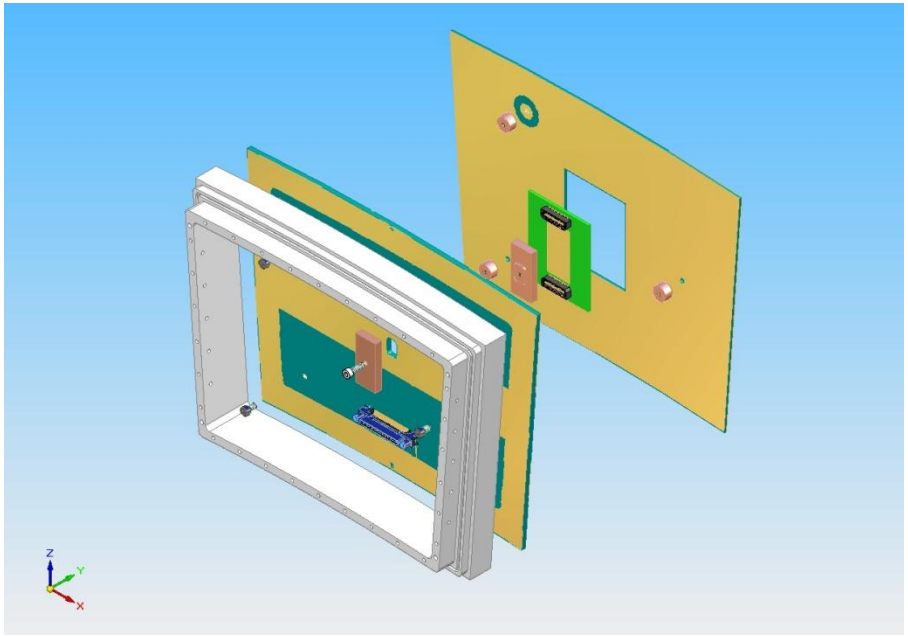
Irfu

cea

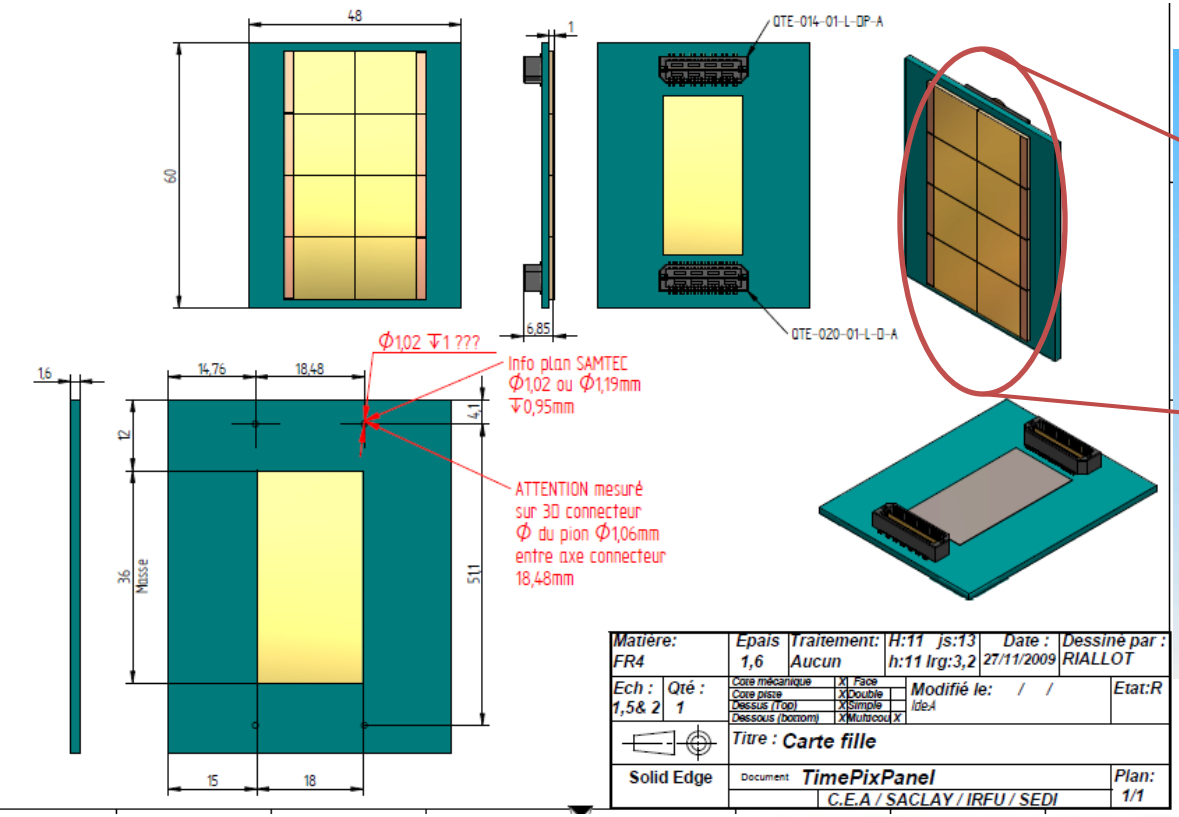
saclay

News from 8 InGrid Board

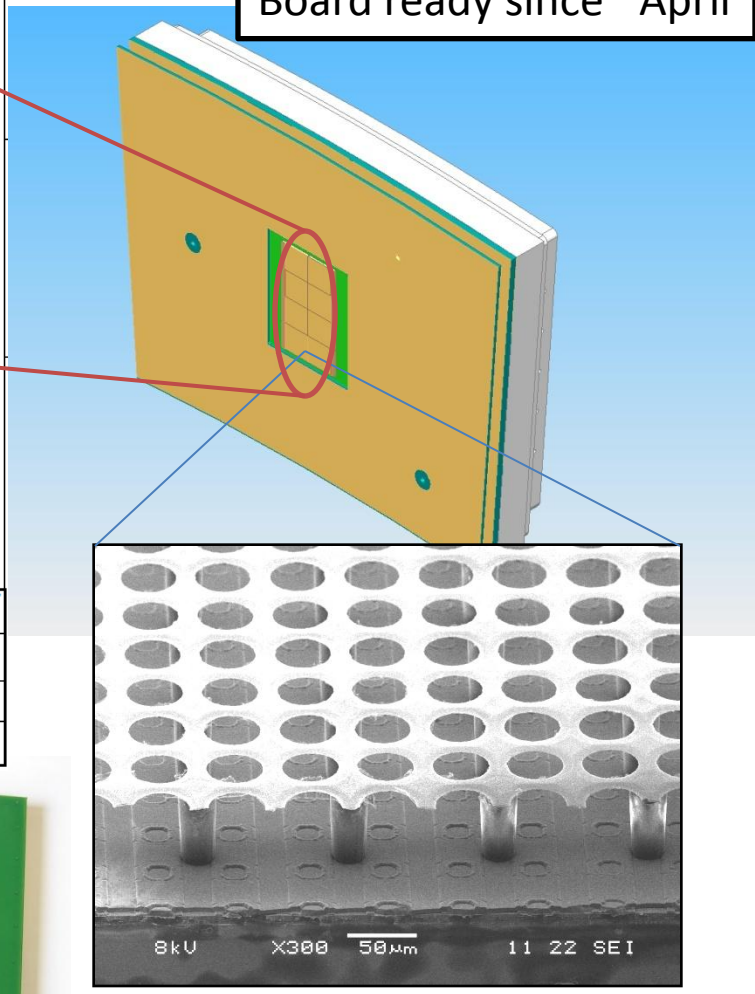
Michael Lupberger



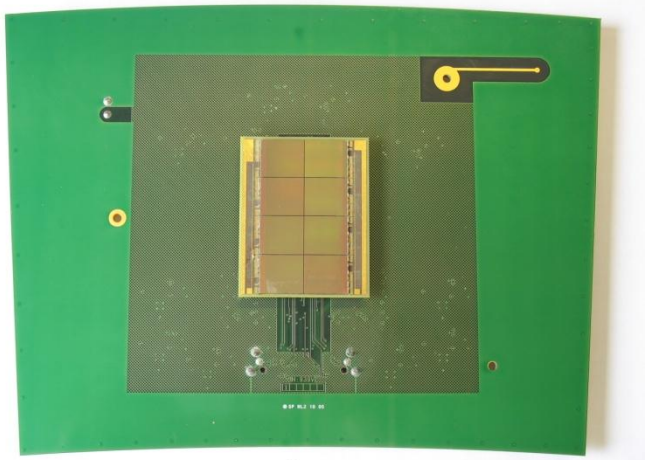
Aim: A panel with 8 Timepix+Ingrid Chips for the large TPC prototyp



Board ready since ~April

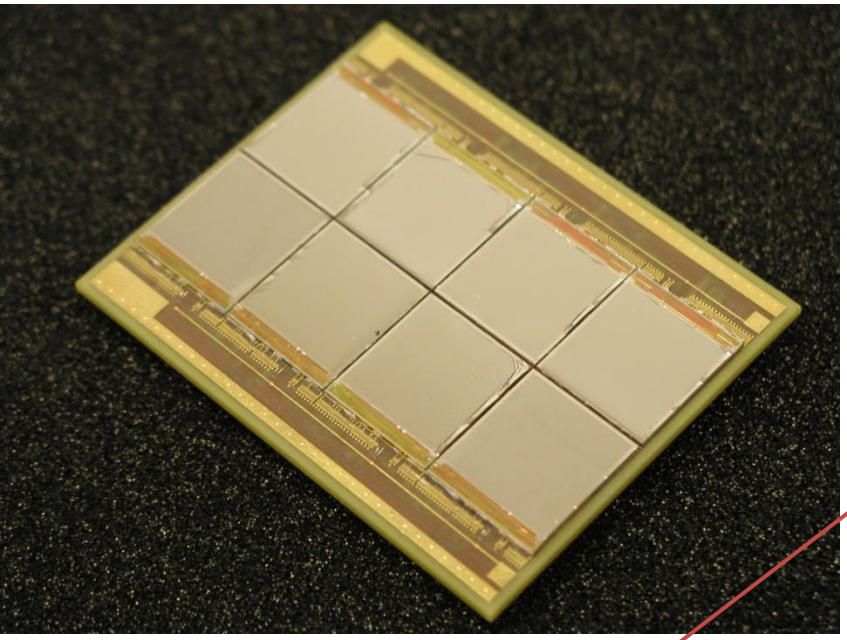


First equipped with 8 naked Timepix chips in NIKHEF bonding lab by Joop Rövekamp

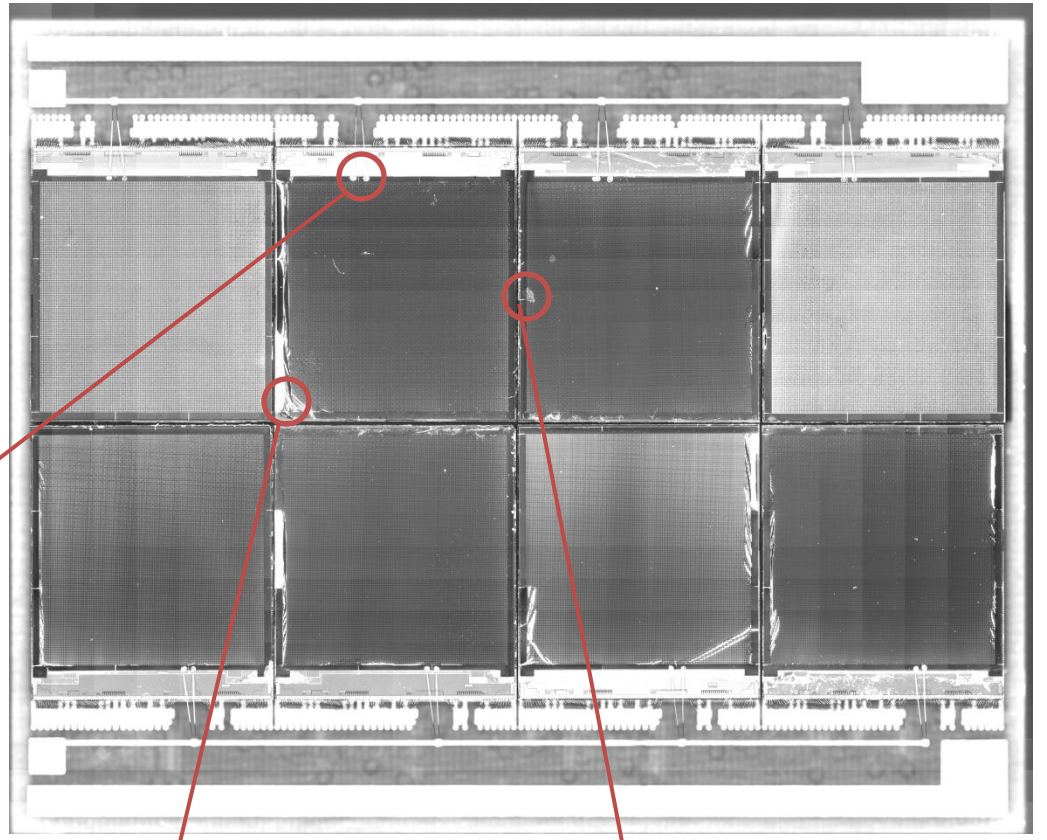


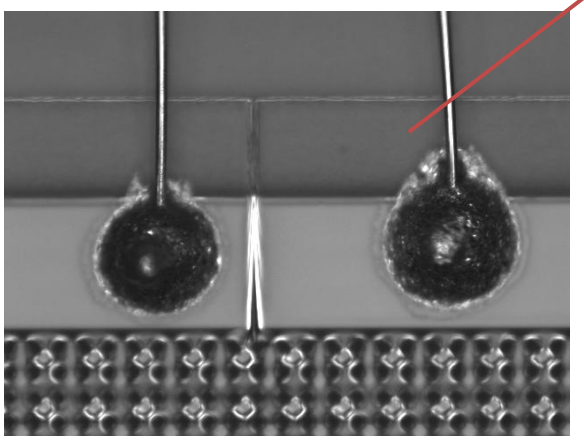
⇒to ensure operability

29.04.2010: 8 Timepix + InGrid Chips glued and bonded daughterboard by Joop

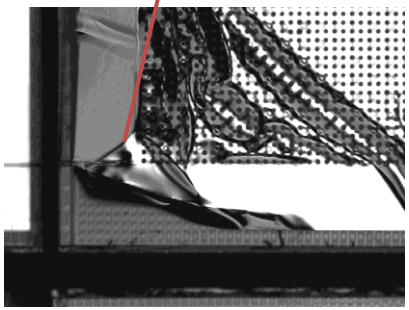


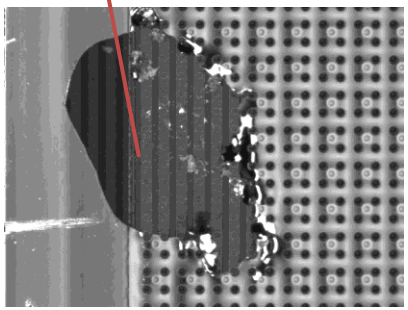
Microscope: Grids not perfect, but very good



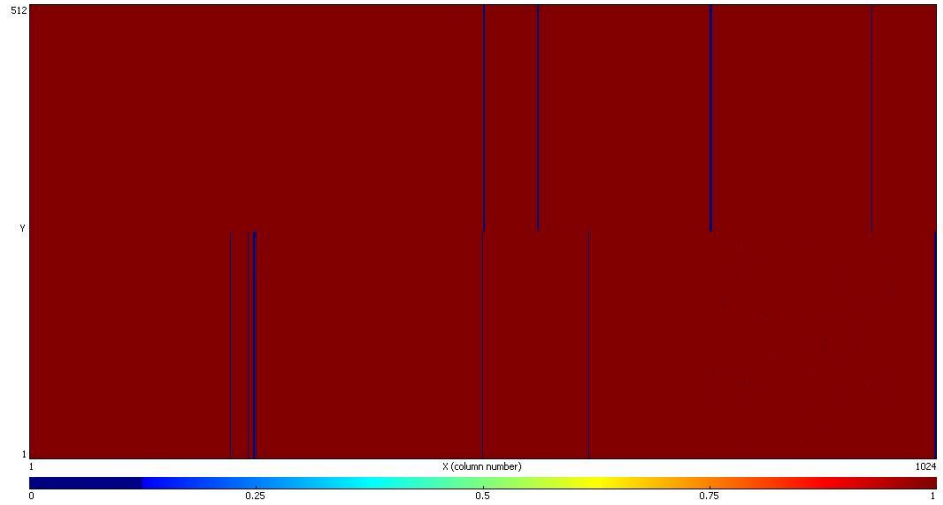


Grid HV bonds fixed with silver glue

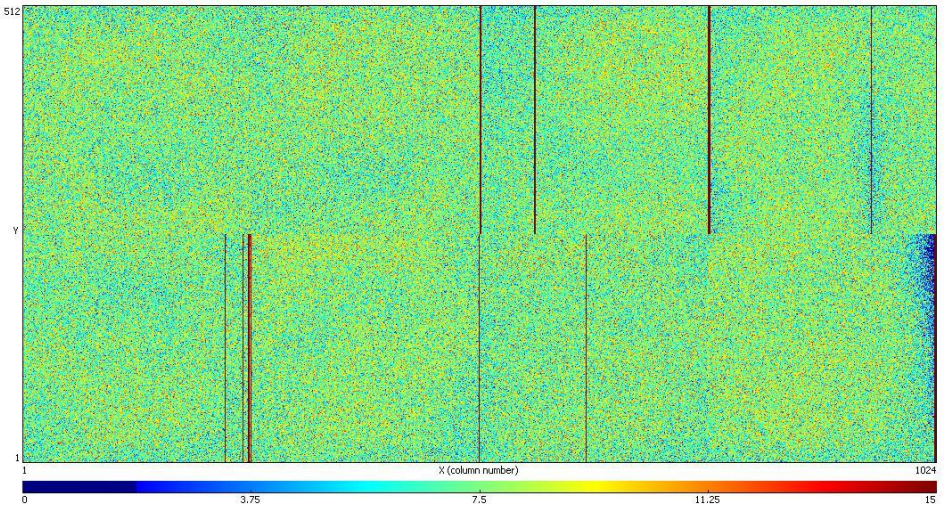




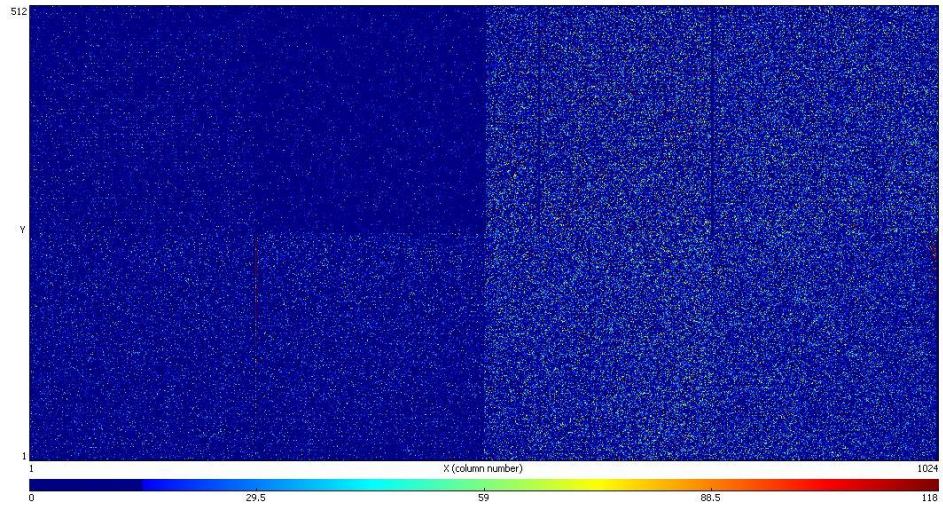
18.05.2010: all 8 chips detected on board and electronically tested
Images from Pixelman



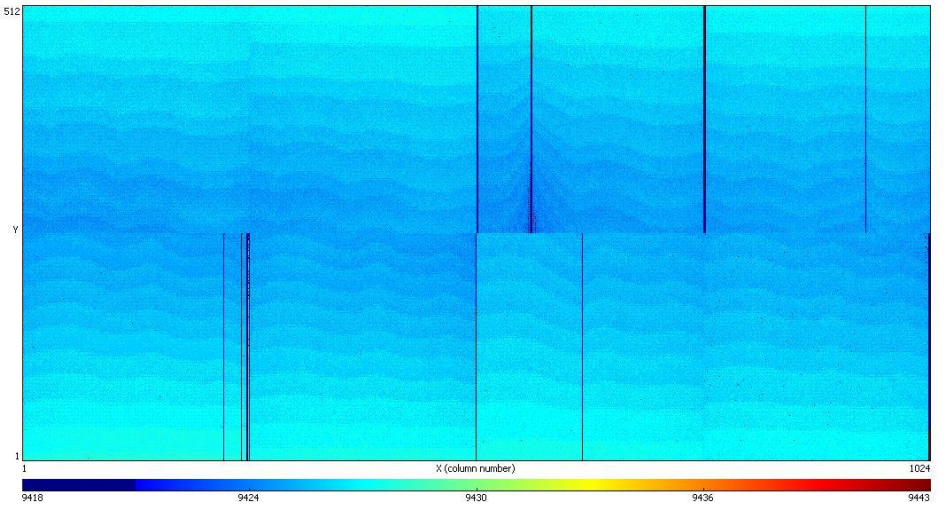
Mask map:4352 pad pixels⇒519937 channels



Threshold adjustment map



Noise (different threshold for chips to see them)



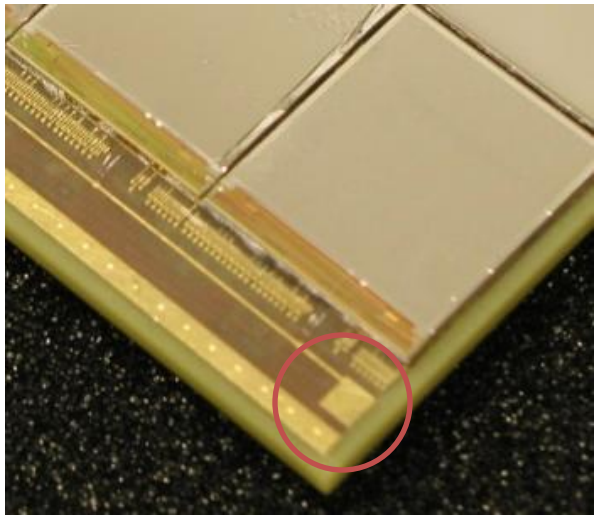
Test pulses in TIME mode

Next steps:

-Connect HV ring

-Apply voltage to the grid

-Hope that there is no current between a grid and a chip



-Calibrate chip (noise, threshold, TOT↔#e- calibration)
-Tests in lab with cosmics and Fe55 (gas chamber is ready)

-Go for test beam at LP TPC