Advanced Endplate Dummy Bd. Progress Report

LCTPC WP5 MTG on May/20/2010

Takahiro Fusayasu, Nagasaki Institute of Applied Science Purpose of the Test with the Dummy AEP Board

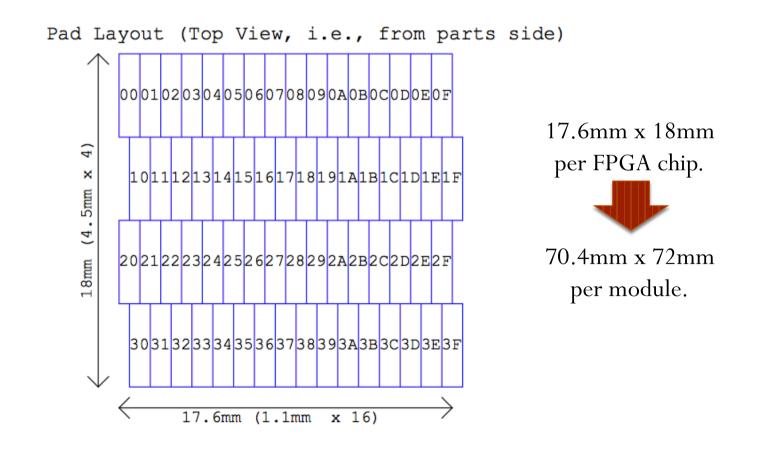
- Thermal test (CO2 cooling).
- Power pulsing test.
- Power pulsing test in magnetic field.

Current Status

- Schematic design was submitted to a layout designer (company) in Mar/2010.
- However, number of parts were too much to be included in the requested area (64mm x 64mm per module).
- Therefore, I changed or removed some parts.
- Still, the area had to be enlarged (see next slides).
- The final schematic was re-submitted just yesterday! I will put the final schematic sheets somewhere later, so please have a look.
- Layout design is underway based on the final schematics.

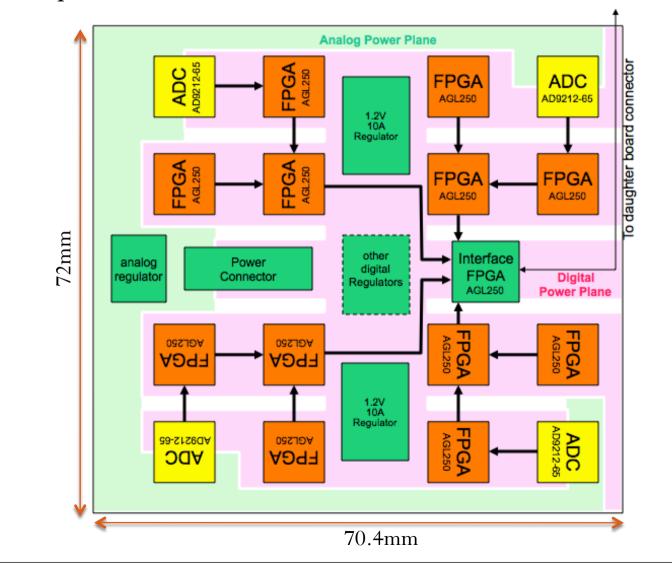
Dimension of Pads

• Because of layout restriction, pad pitch was increased to 1.1mm x 4.5mm (it was 1.0mm x 4.0mm before).



Dimension of One Module

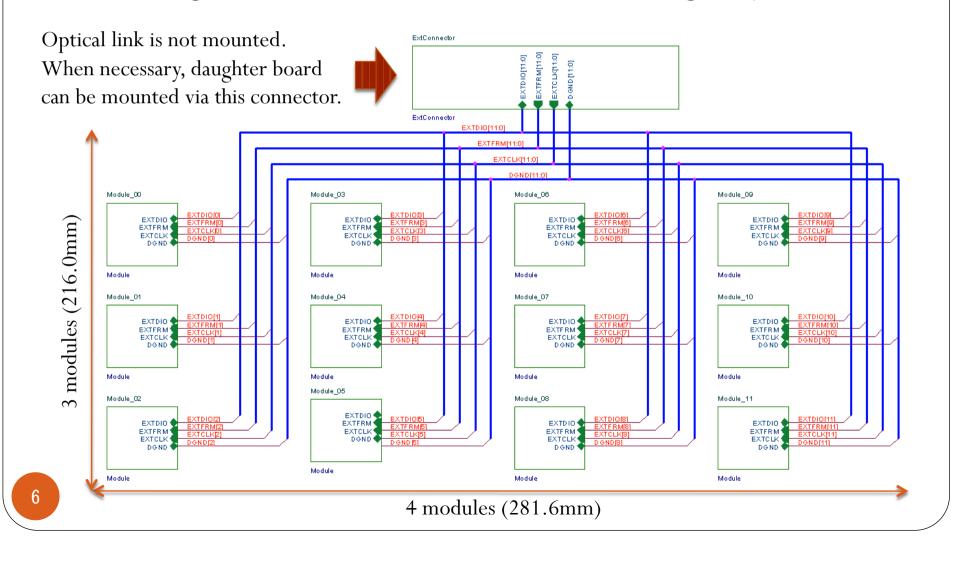
• Concept is not different from before but the size.

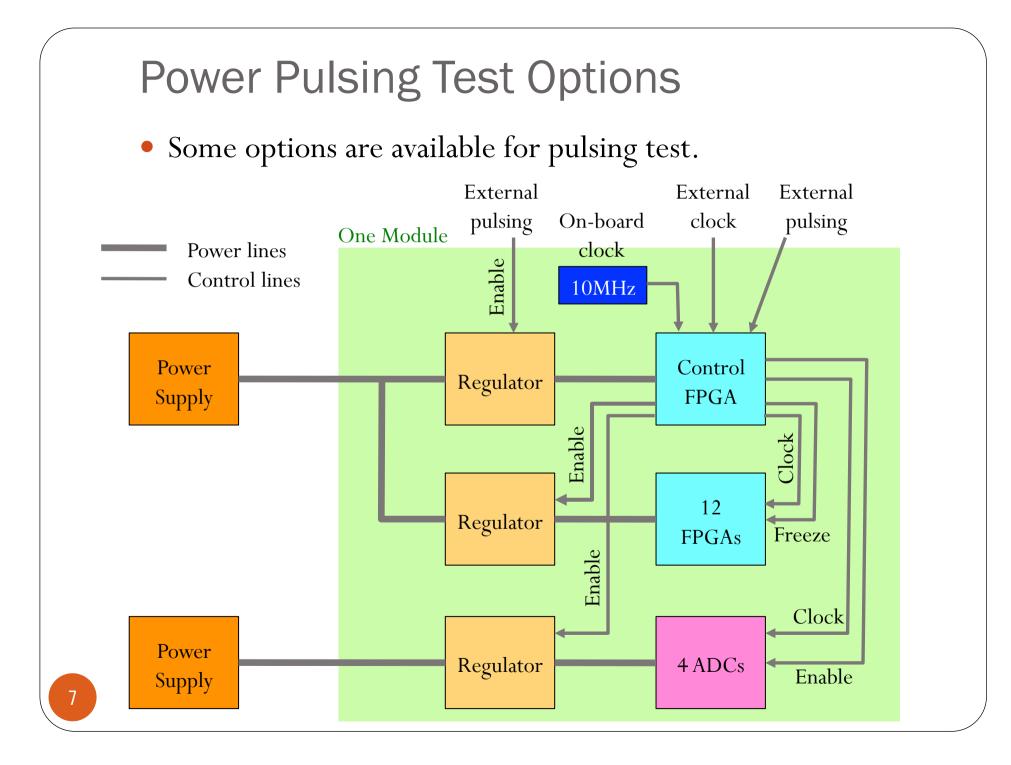


5

Dimension of the Board

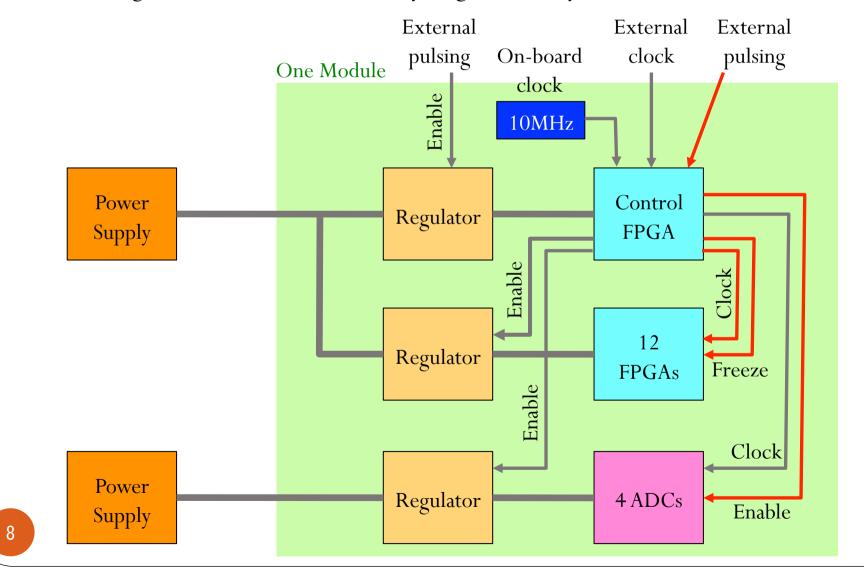
• As the cost is fixed already, number of modules per board is changed to 12 modules/board (it was 16 originally).





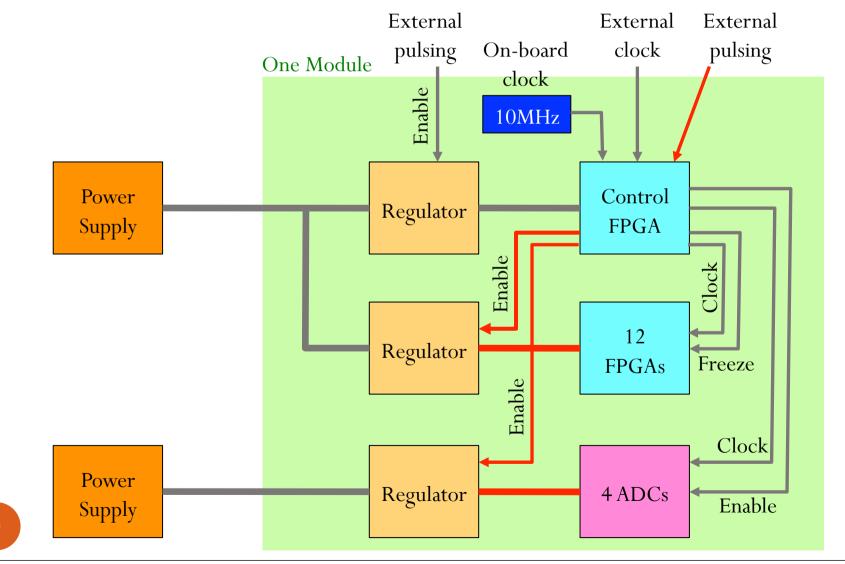
Power Pulsing Test: Option A

• Switch clock or freeze for FPGA and enable for ADC using control FPGA. Pulsing can be either feed externally or generated by control FPGA.

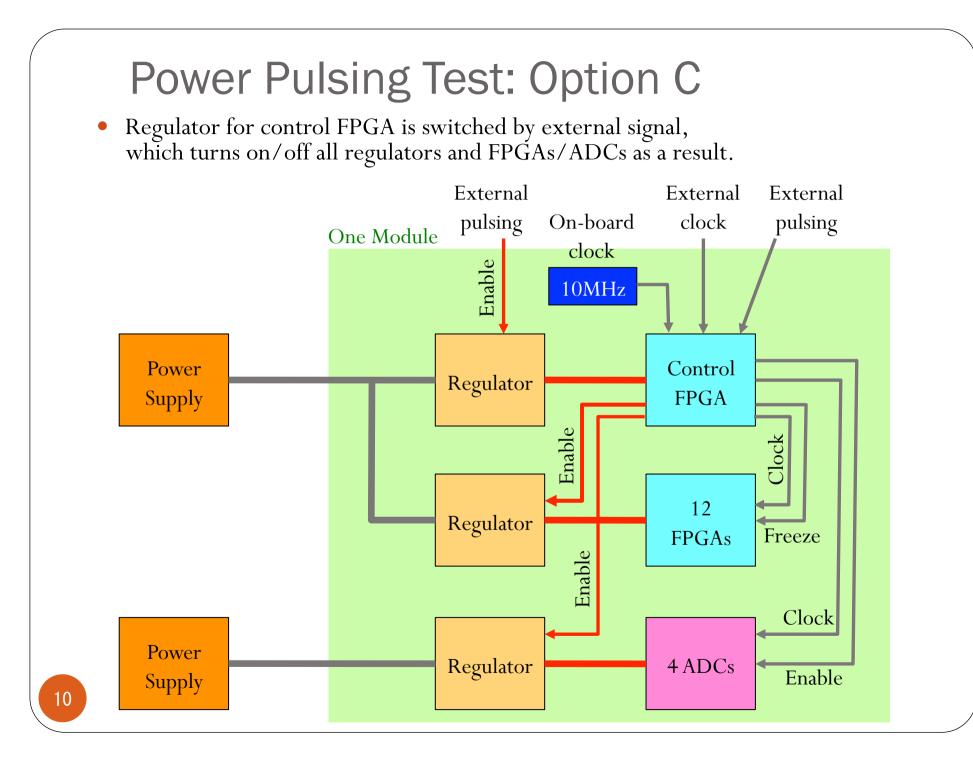


Power Pulsing Test: Option B

• Power regulators are switched by FPGA via enable pins. Pulsing can be either feed externally or generated by control FPGA.

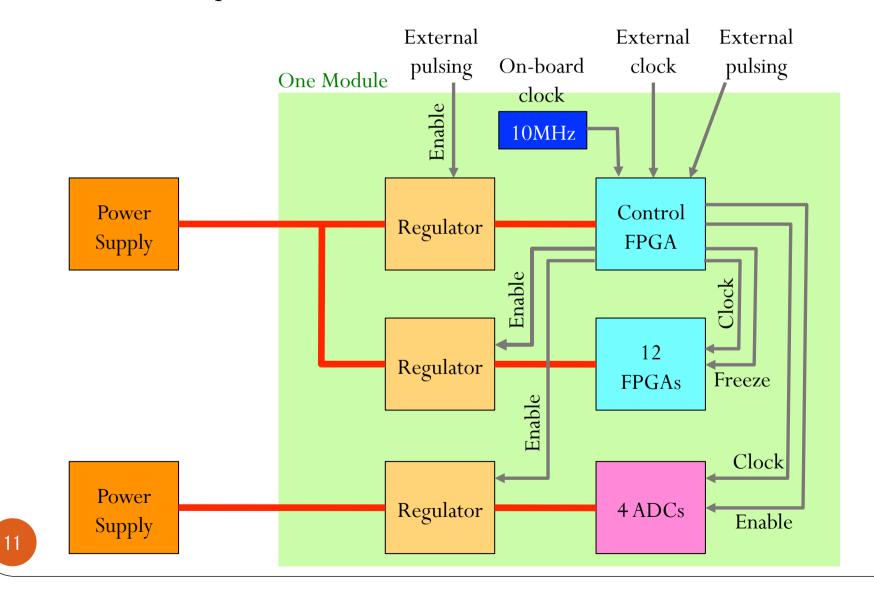


9



Power Pulsing Test: Option D

• Switch the power sources.



Plan

- The board will be available in the end of June or beginning of July.
- Test with normal condition, i.e. water cooling etc., will be performed in July ~ August/2010.
- I hope we can perform CO_2 cooling test at NIKHEF in Autumn this year.