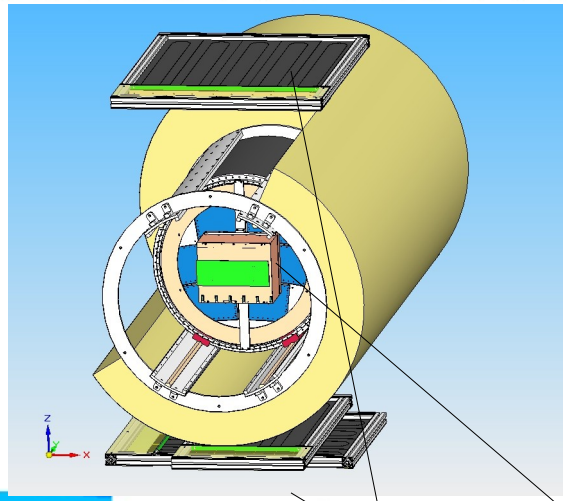
TPC Task: the Past and the Present

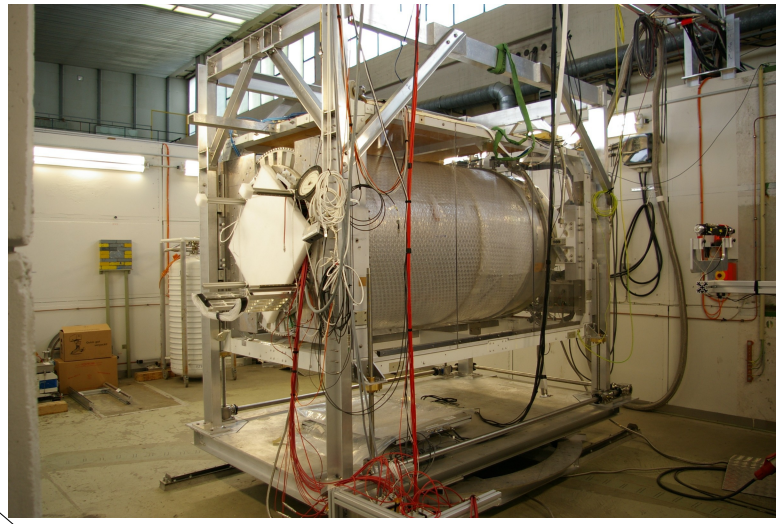
Klaus Dehmelt
DESY

EUDET Annual Meeting in Hamburg
Plenary Session JRA2
September 30th, 2010

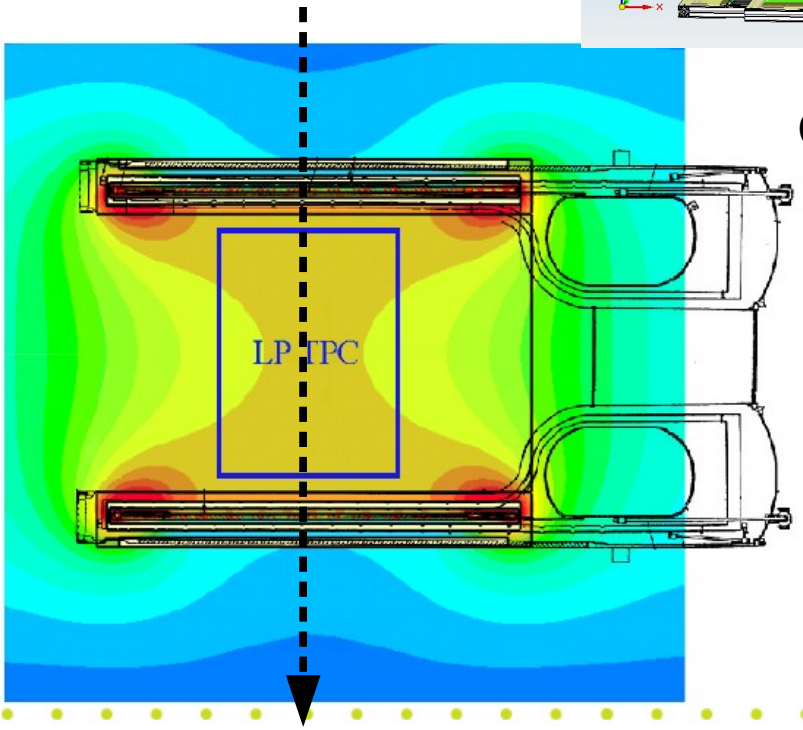
The Present

- *PCMAG:* superconducting magnet, up to 1.25 T
- e^- test beam @DESY (1GeV/c<p<6GeV/c)

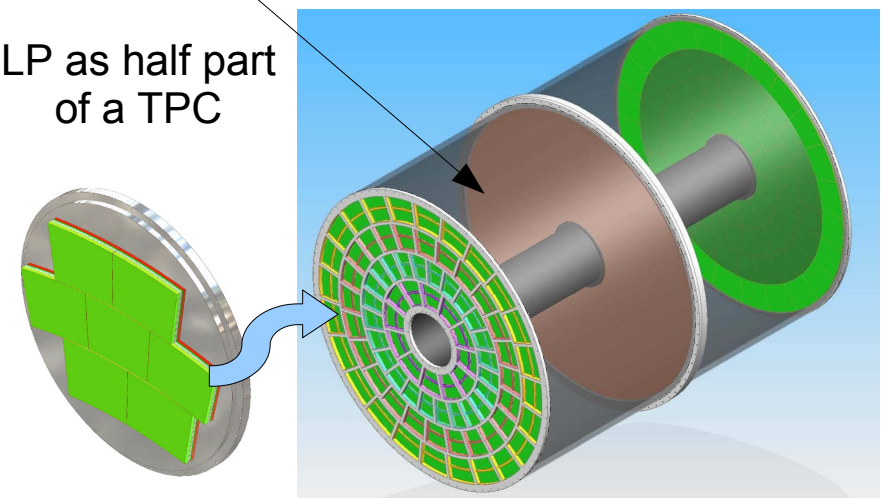




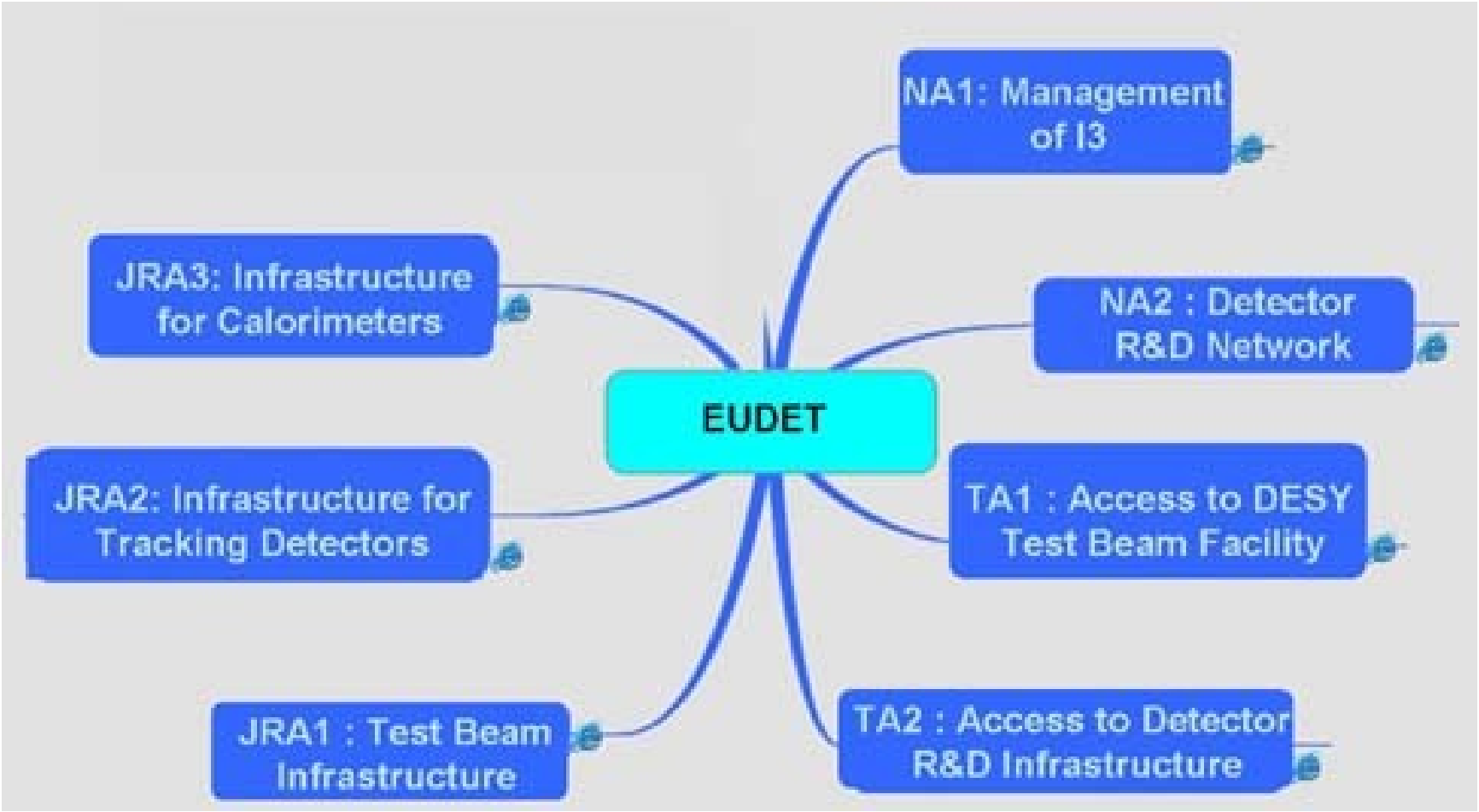
Cosmic Trigger Setup



LP as half part of a TPC



EUDET and Scientific Activities



EUDET and JRA2

Joint Research Activities (JRA) 1/2/3

JRA2 wants to integrate the efforts of European institutions working on tracking detectors for the ILC. This includes the improvement of existing infrastructures for tracking detectors, the developments of common prototypes, and the development of novel techniques for Si based tracking detectors.

For the TPC-task:
Infrastructure for Time Projection Chamber Research and Development

The TPC and the ILC

- Performance goals and design parameters for a TPC with standard electronics at the ILC detector

Size (LDC–GLD average)	$\phi = 3.6$m, L = 4.3m outside dimensions
Momentum resolution (B=4T)	$\delta(1/p_t) \sim 10 \times 10^{-5}$/GeV/c TPC only; × 0.4 incl. IP
Momentum resolution (B=4T)	$\delta(1/p_t) \sim 3 \times 10^{-5}$/GeV/c (TPC+IT+VTX+IP).
Solid angle coverage	Up to at least $\cos\theta \sim 0.98$
TPC material budget	$< 0.03X_0$ to outer fieldcage in r
	$< 0.30X_0$ for readout endcaps in z
Number of pads	$> 1{\times}10^6$ per endcap
Pad size/no.padrows	~ 1mm×4–6mm/~200 (standard readout)
$\sigma_{\text{singlepoint}}$ in $r\phi$	$\sim 100\mu$m (for radial tracks, averaged over driftlength)
$\sigma_{\text{singlepoint}}$ in rz	~ 0.5 mm
2-hit resolution in $r\phi$	< 2 mm
2-hit resolution in rz	< 5 mm
dE/dx resolution	< 5 %
Performance robustness	> 95% tracking efficiency for all tracks–TPC only)
(for comparison)	(> 95% tracking efficiency for all tracks–VTX only)
	> 99% all tracking[13]
Background robustness	Full precision/efficiency in backgrounds of 1% occupancy
	(simulations estimate < 0.5% for nominal backgrounds)
Background safety factor	Chamber will be prepared for 10 × worse backgrounds
	at the ILC start-up.

with MPGD

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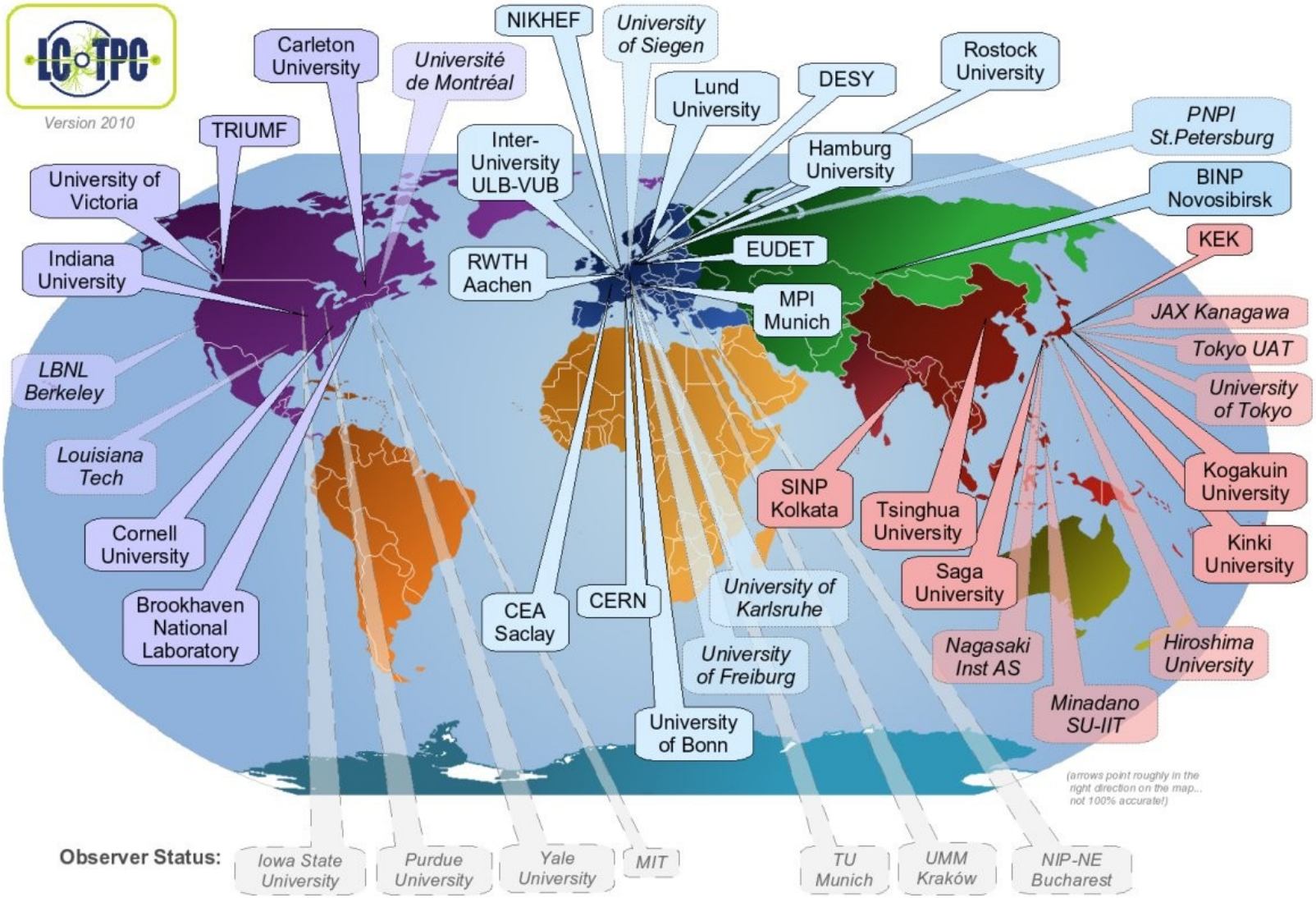
with MPGD

TPC Prototyping

- Large TPC prototype JRA2:
  - $O(\varnothing) \approx 1$ m
  - low mass field cage
  - modular endplate system for large surface GEM and MicroMegas system
  - development of prototype electronics for GEM and MicroMegas
- Large bore magnet PCMAG JRA2:
  - B $\approx$ 1 Tesla, $\varnothing \approx$ 0.85 m, standalone He cooling, provided by KEK
  - infrastructure (control, fieldmapping etc.) through EUDET
- Si-envelope

EUDET & LCTPC


Version 2010
Carleton University
Université de Montréal
NIKHEF
University of Siegen
Lund University
DESY
Rostock University
PNPI St.Petersburg
TRIUMF
Inter-University ULB-VUB
Hamburg University
BINP Novosibirsk
University of Victoria
Indiana University
RWTH Aachen
EUDET
KEK
MPI Munich
JAX Kanagawa
Tokyo UAT
University of Tokyo
LBNL Berkeley
Louisiana Tech
SINP Kolkata
Tsinghua University
Kogakuin University
Cornell University
Saga University
Kinki University
Brookhaven National Laboratory
CEA Saclay
CERN
University of Karlsruhe
Nagasaki Inst AS
Hiroshima University
University of Freiburg
Minadano SU-IIT
University of Bonn
(arrows point roughly in the right direction on the map... not 100% accurate!)
Observer Status:
Iowa State University
Purdue University
Yale University
MIT
TU Munich
UMM Kraków
NIP-NE Bucharest

EUDET & LCTPC

preparing for the test beam

"LP Subsystems Meeting at DESY"

chaired by Klaus Dehmelt (DESY) Participants: Ties Behnke , Paul Colas , Klaus Dehmelt , Ralf Diener , Christian Grefe , Stephan Haensel , Lea Hallermann , Xavier Janssen , Jochen Kaminski , Dean Karlen , Alexander Kaukher , Martin Killenberg , Claus Kleinworth , Diana Linzmaier , Krzysztof Komar , Takeshi Matsuda , Ulf Mjoernmark , Anders Oskarsson , Dan Peterson (VRVS) , Oliver Schaefer , Franck Senee , Ronald Dean Settles , Akira Sugiyama (VRVS) , Jan Timmermans , Peter Wienemann

from **Monday 25 February 2008 (10:00)**
to **Tuesday 26 February 2008 (18:00)**
at DESY Hamburg (*SemRm 4a (Mon) / 5 (Tue)*)

Description : Meeting on status and plans of the LP subsystems for the LP beamtest at DESY in 2008/2009.

Monday 25 February 2008 | Tuesday 26 February 2008 |

Monday 25 February 2008 top

10:00->*10:10* Welcome
Description:
Welcome and Organization of the Meeting (Klaus Dehmelt)

10:10->*10:30* Introduction Klaus Dehmelt
Description:
Goals of the LCTPC tests (Klaus Dehmelt)

10:30->*12:00* Mechanics I Klaus Dehmelt; slides; slides
Description:
Akira Sugiyama (via VRVS):

GEM panels

Klaus Dehmelt:

Field-Cage
Infrastructure/Gas/HV
PCMAG

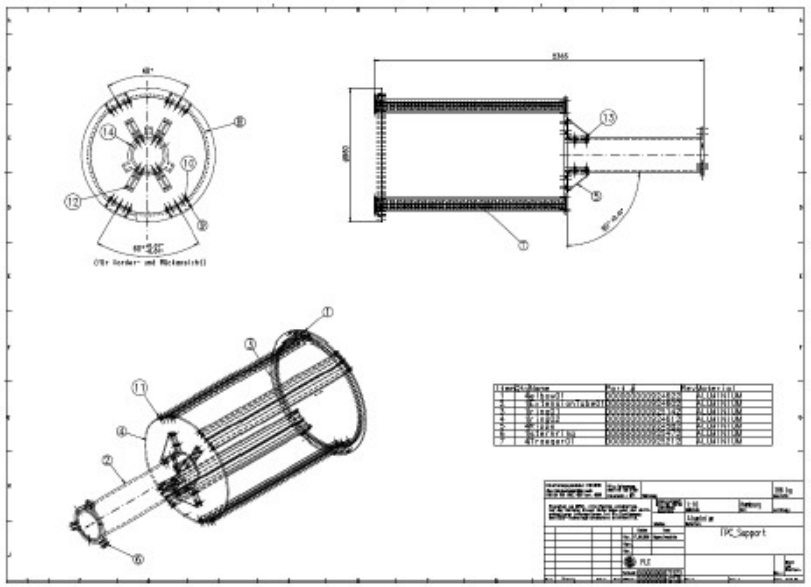
Christian Grefe:

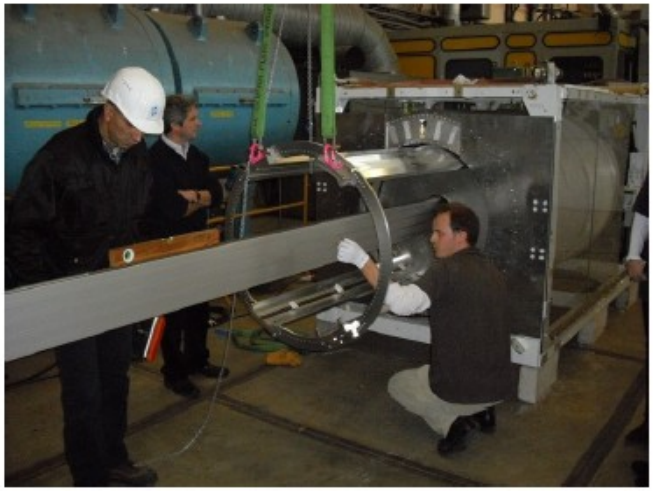
Fieldmap of PCMAG

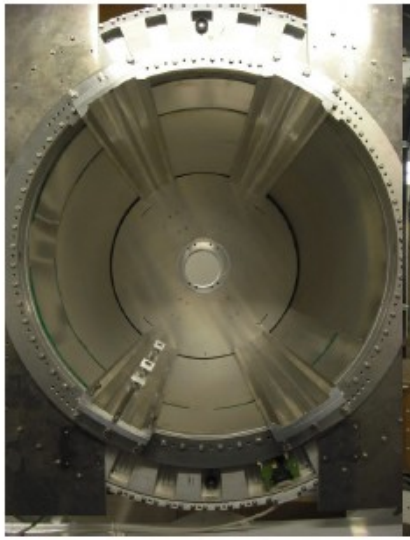
Ulf Mjoernmark:

Readout (RO) / DAQ based on ALTRO

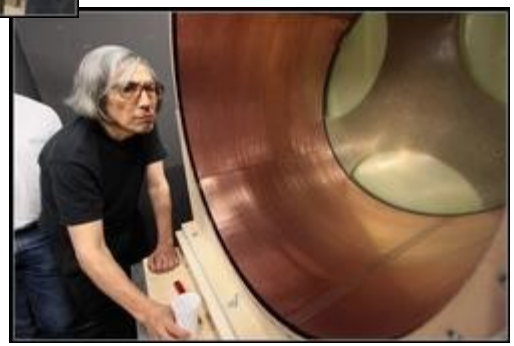
LP needs Support



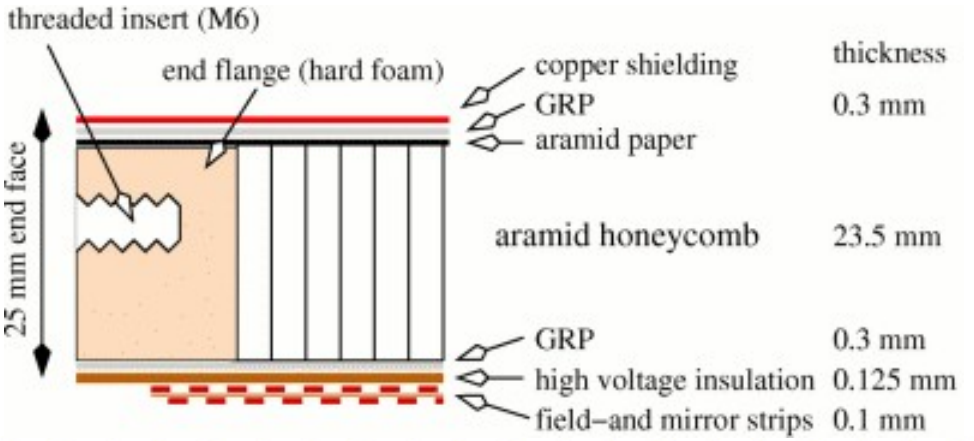




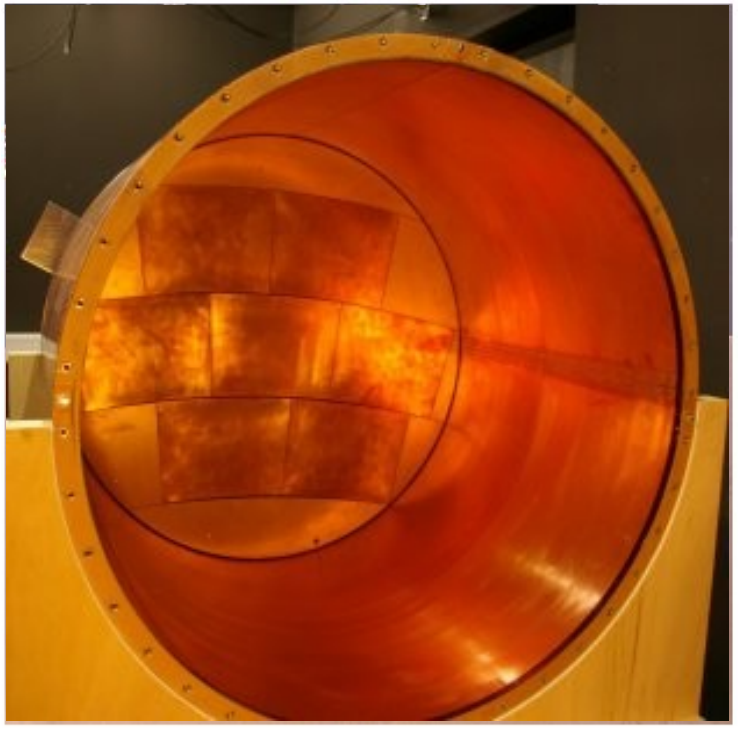
Field Cage



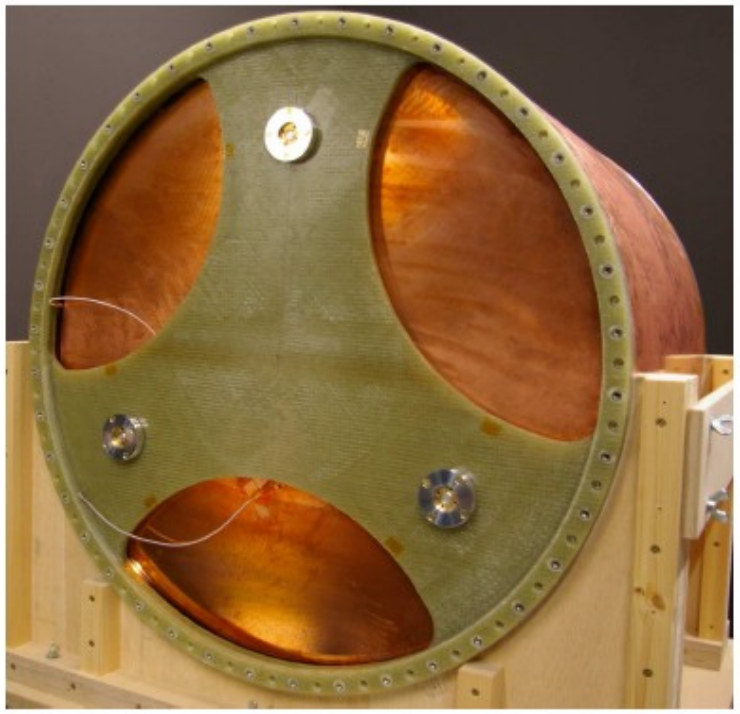
Diameter: Inner 720 mm,
Outer 770 mm
Wall thickness 25 mm
Length 610 mm
HV to be applied: up to 20 kV



Field Cage

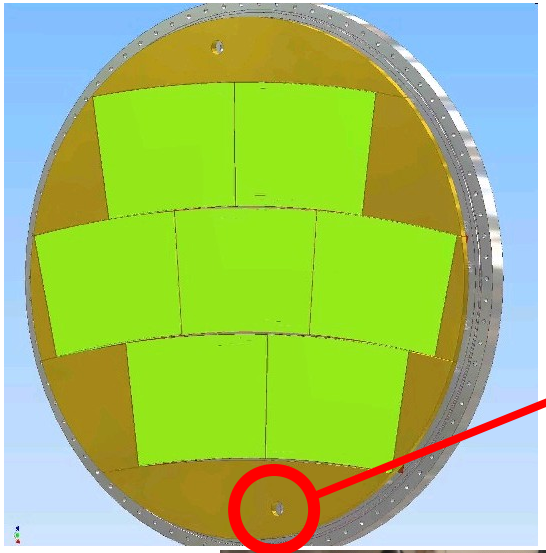


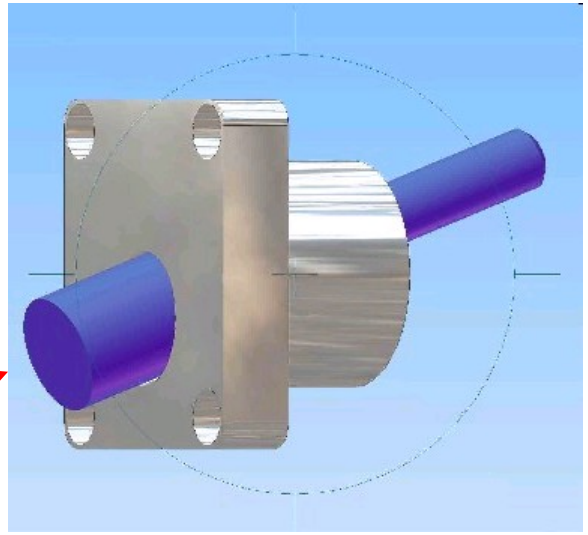
field cage with anode end plate

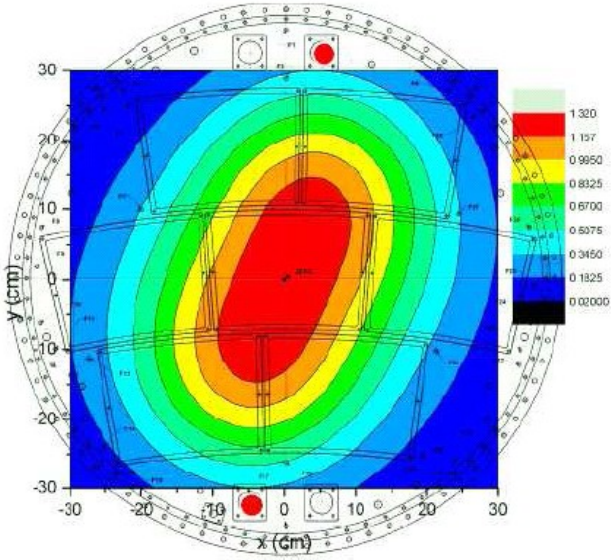


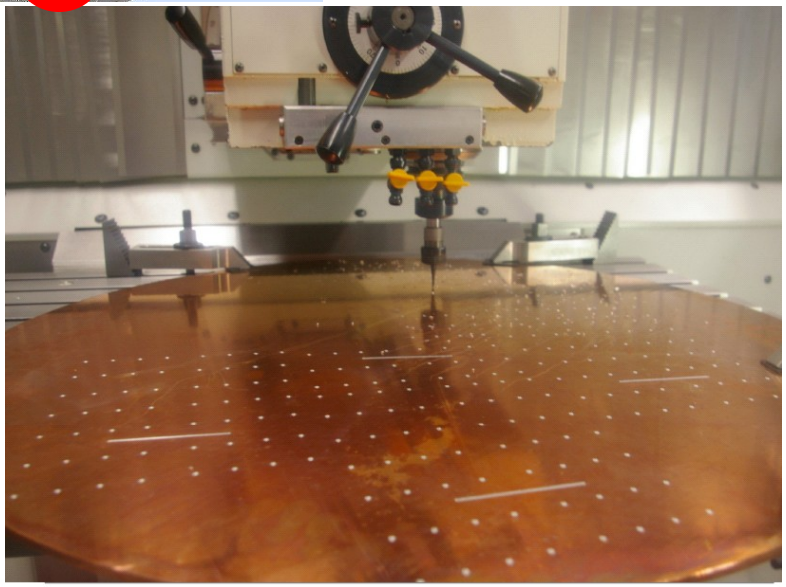
field cage with cathode end plate

Laser Calibration Setup

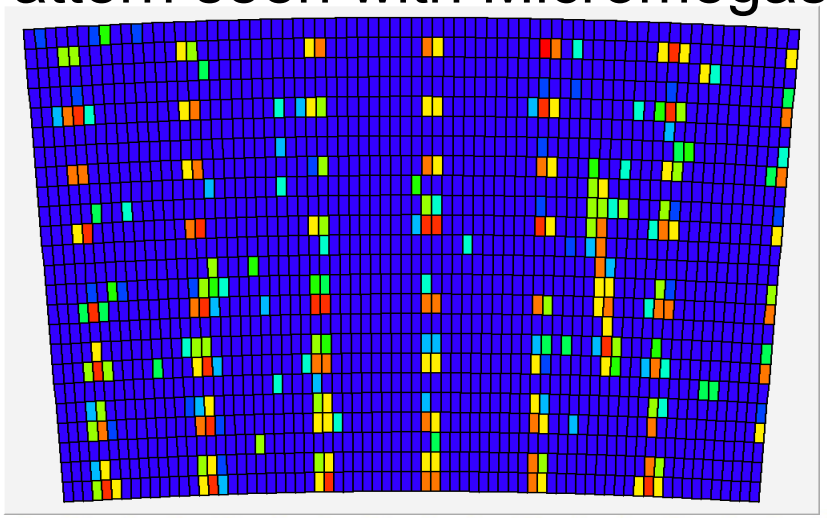




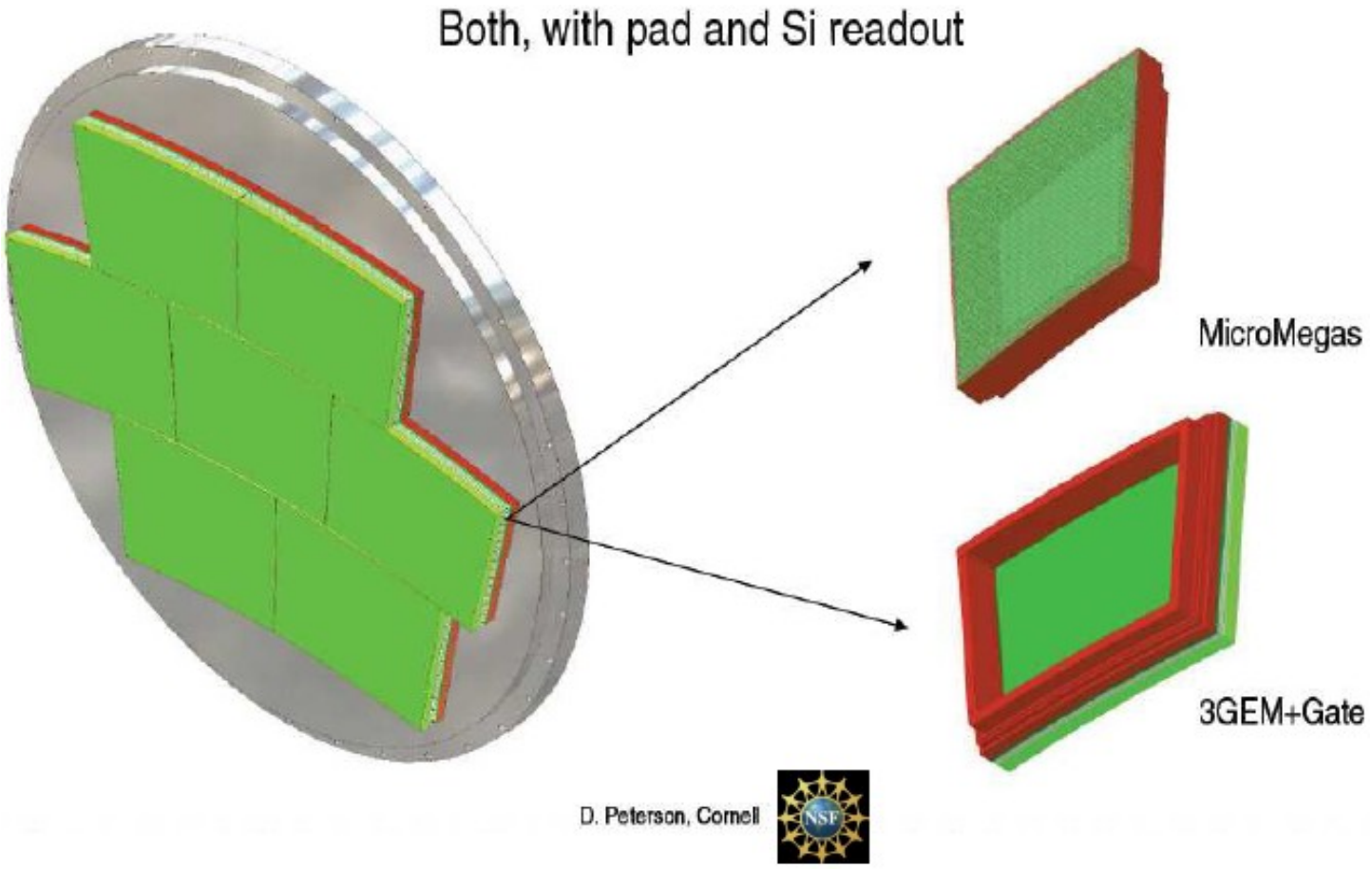




Pattern seen with Micromegas

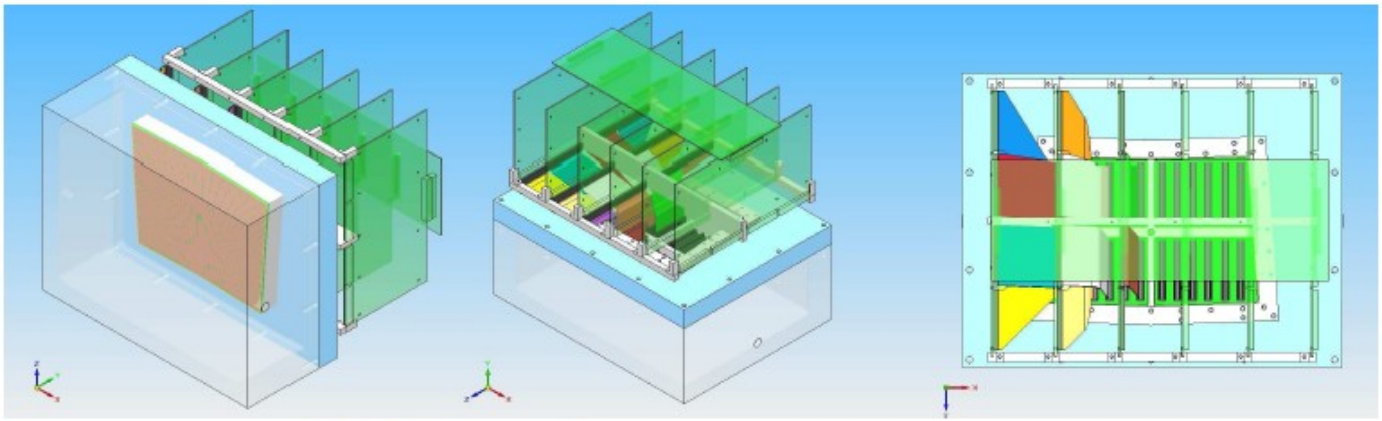


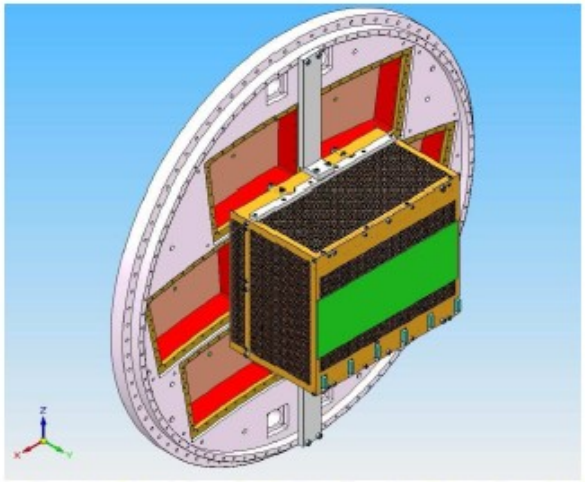
End Plate for Readout Modules



First Readout Module

MicroMegas module + AFTER electronics being finalized for first usage in LP/PCMAG/DESY





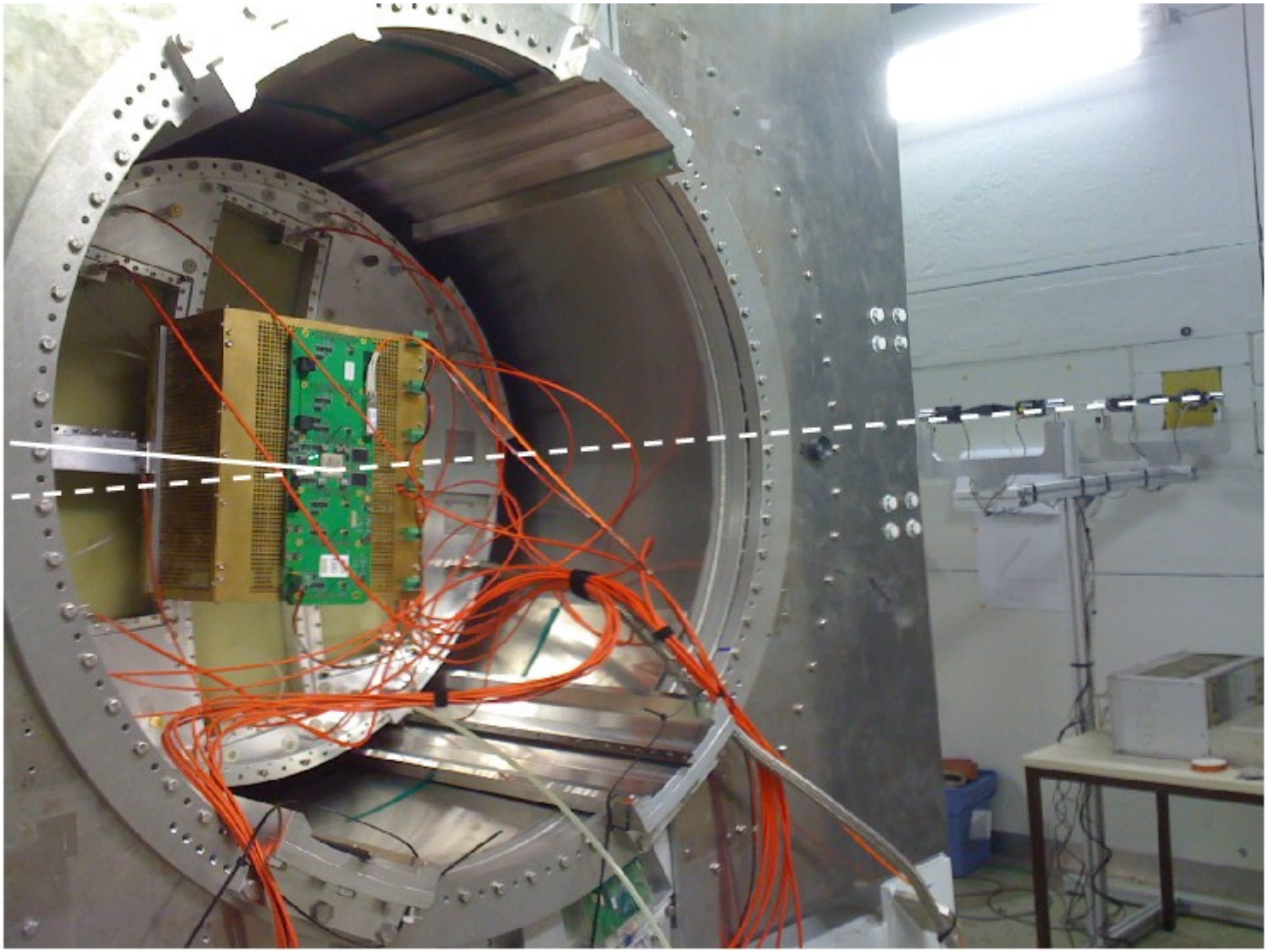
- One module (without resistive layer) is finished
- Received in Saclay and being tested. Others with different resistive coatings should follow.

Parts assembled at DESY

Parts assembled at DESY

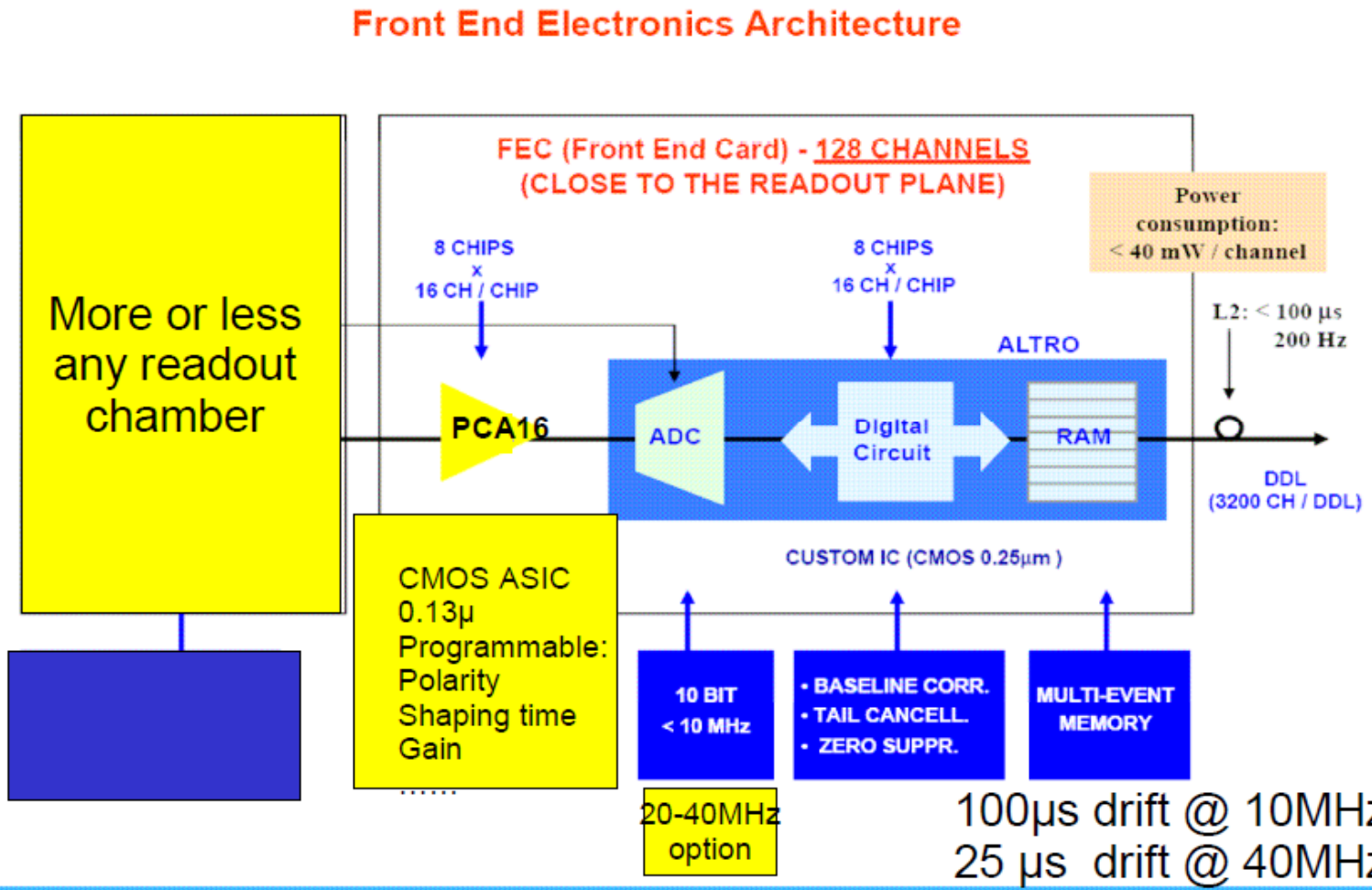
And then there was Beam

Nov. 2008: First beam ~7.7° test with Micro-Megas



Next Readout Module

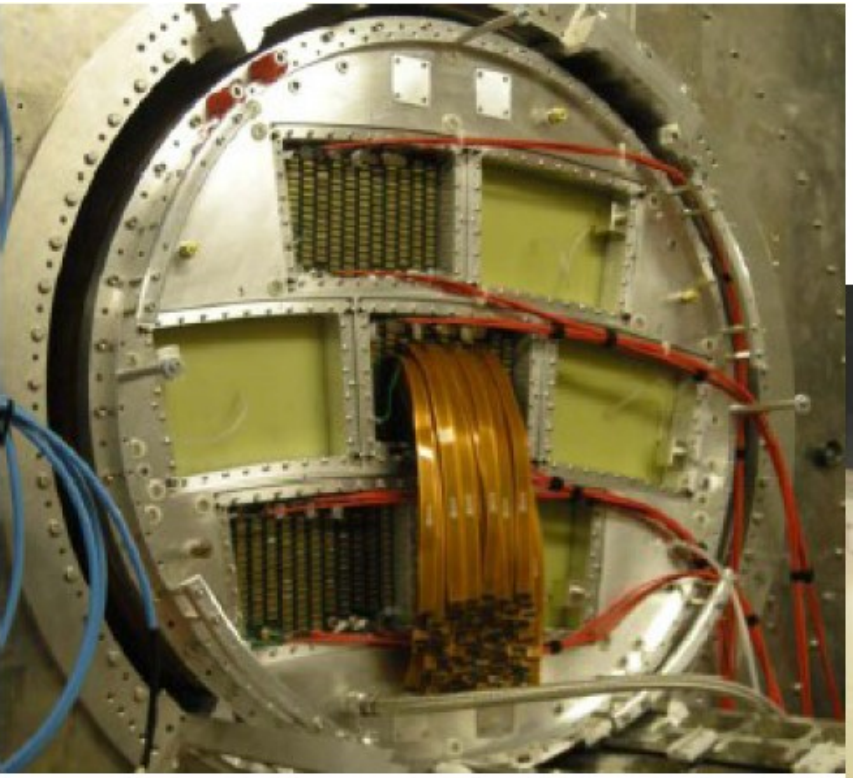
EUDET readout FEC



Next Readout Module

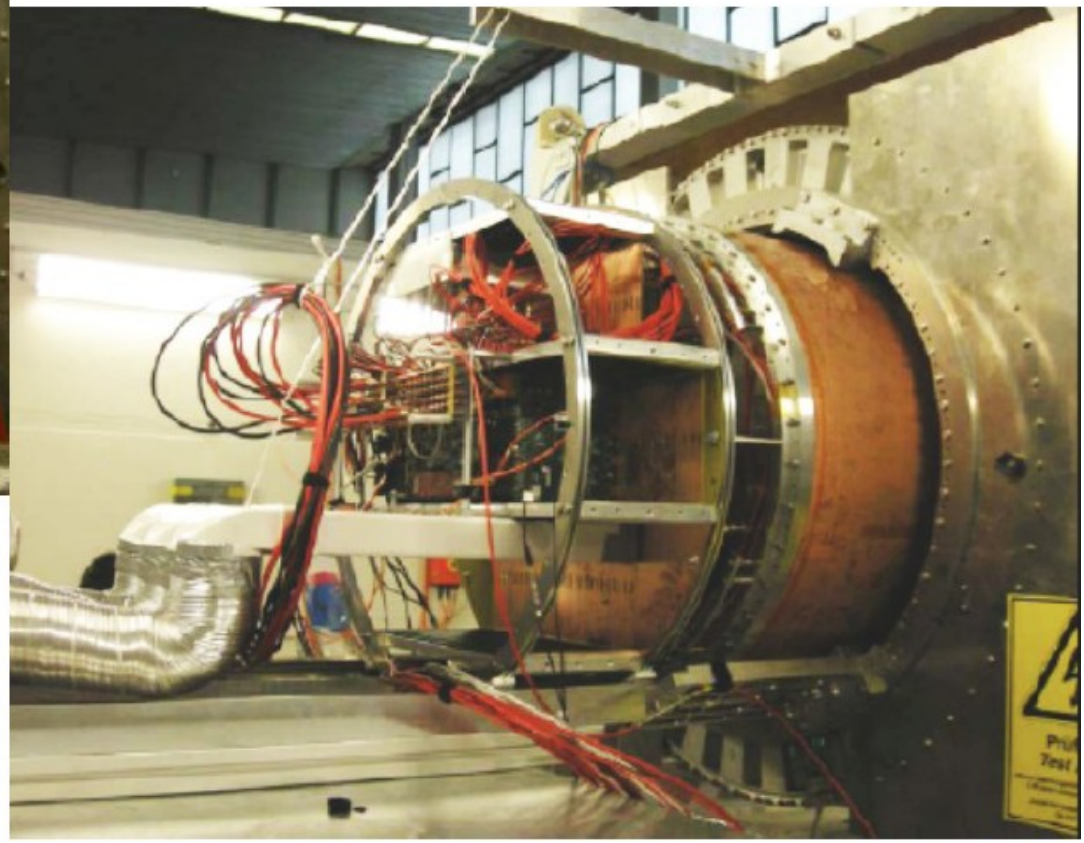
- FADC-based (Lund, CERN)
  - 165 PCA16 chips have been tested in Lund, 17 have not passed the final tests → 2368 channels available
  - 800 remaining PCA16 chips are at CERN
  - Tests of the 2nd prototype FEC performed in Lund: performance as expected → 15 boards being produced
  - 40 MHz ALTRO chips are mounted onto 2nd prototype board
  - 1 DRORC, 1 SIU, 1 optical-cable has been sent to Lund for setting up a system to install the new firmware → system will later be used in the test setup at DESY

And then there was Beam



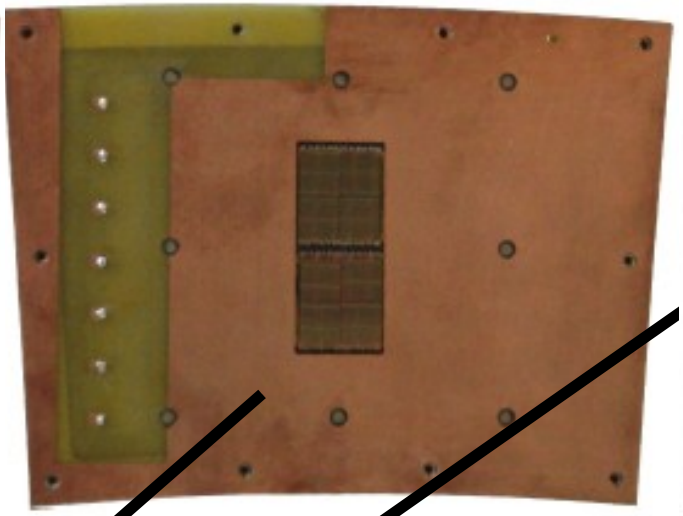
Testbeam with 2-GEM in Mar2009

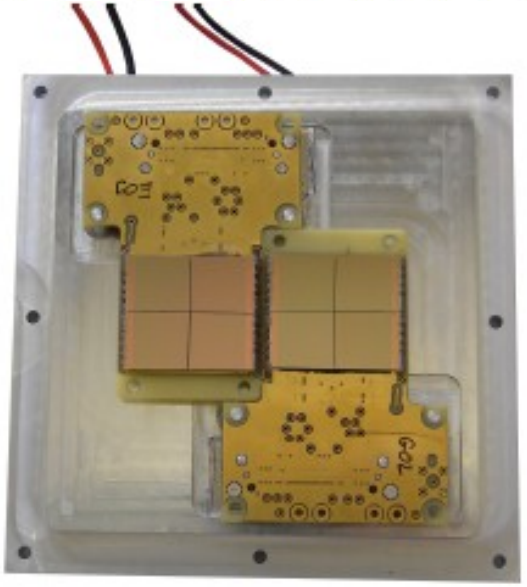
About 3200 channels readout electronics



Readout electronics:
Based on ALTRO (ALICE TPC)
L. Joensson, LUND University

Next Readout Module





anode plane

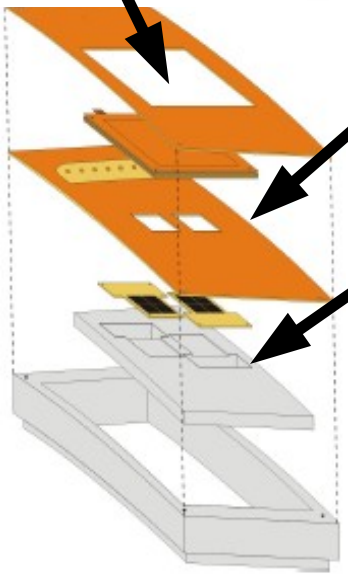
GEMs

readout plane

quad-boards

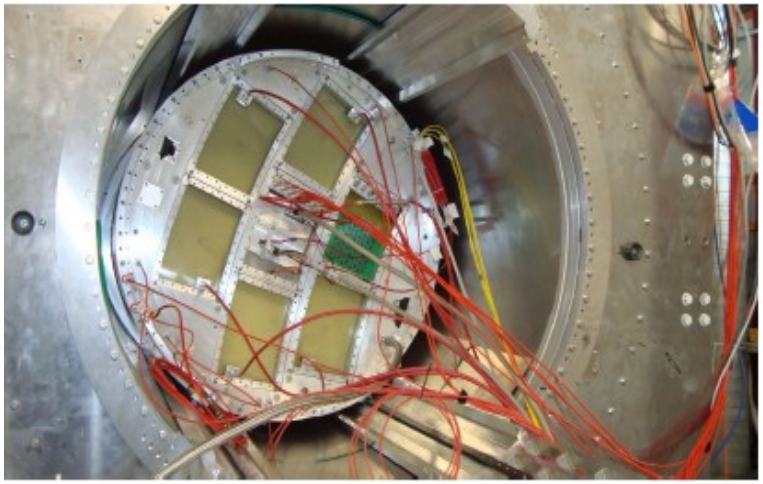
reinforcement of anode plane

redframe



Readout:
2 quadboards
(4 TimePix
Chips each)

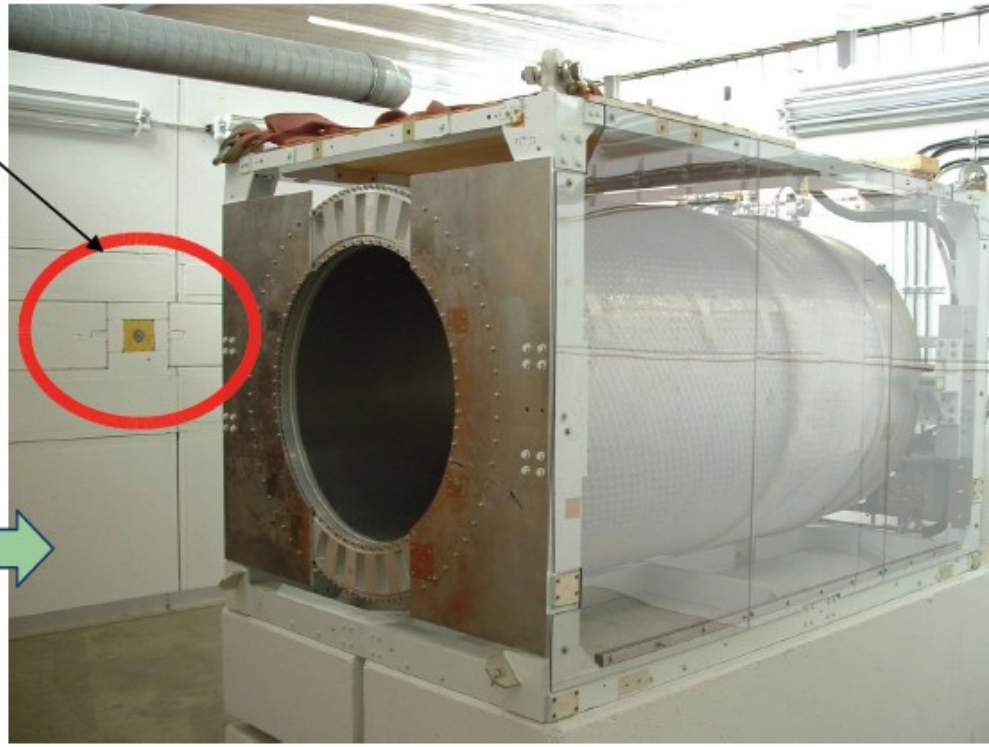
J. Kaminski, Univ. of Bonn



PCMAG on the Block

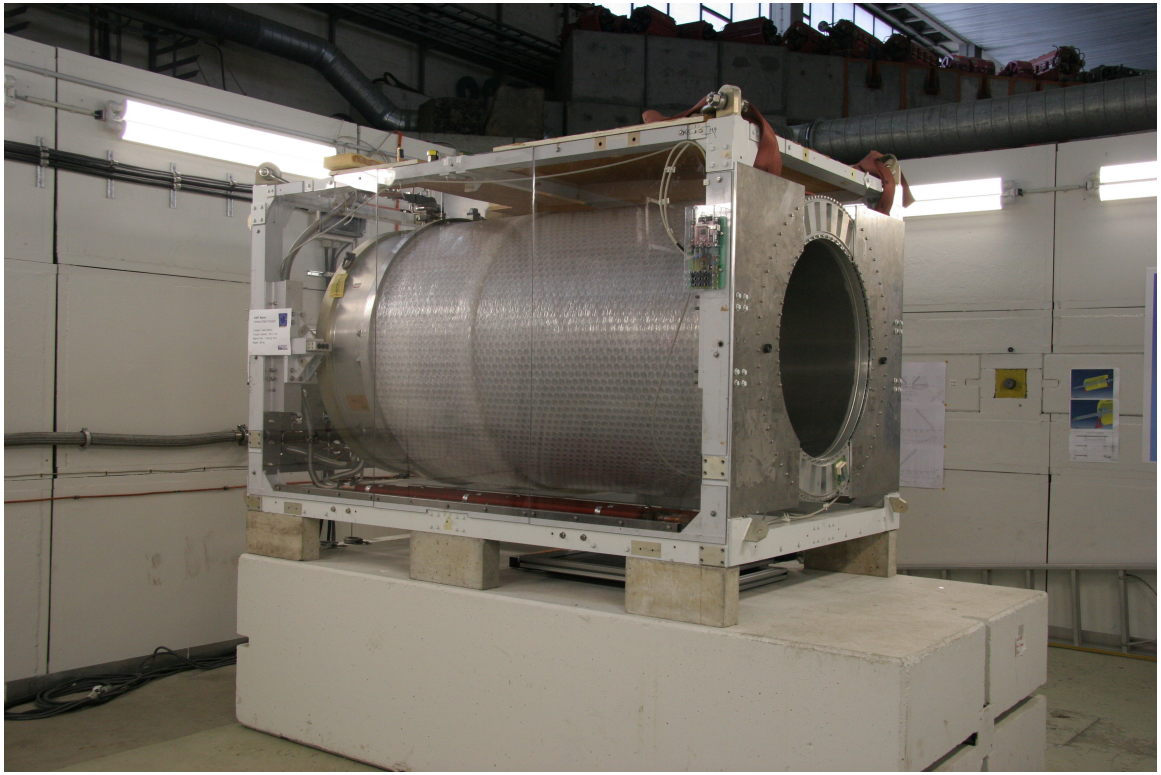
TPC will be adjusted
- horizontally
- vertically
- rotationally

w.r.t. beam line

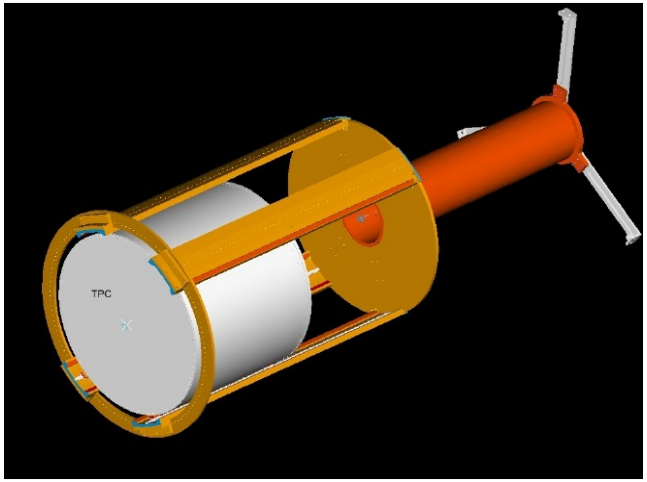


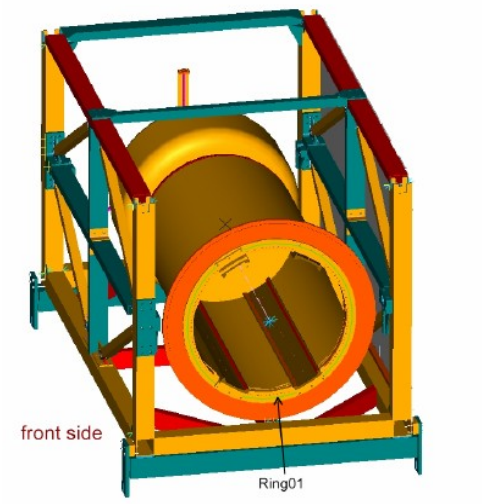
Problem: magnetizable components

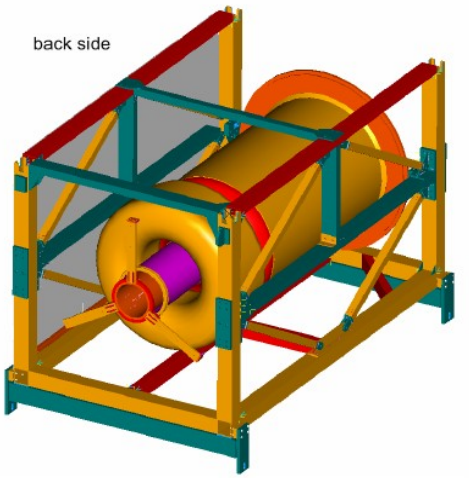
PCMAG on the Block



LP Mechanics



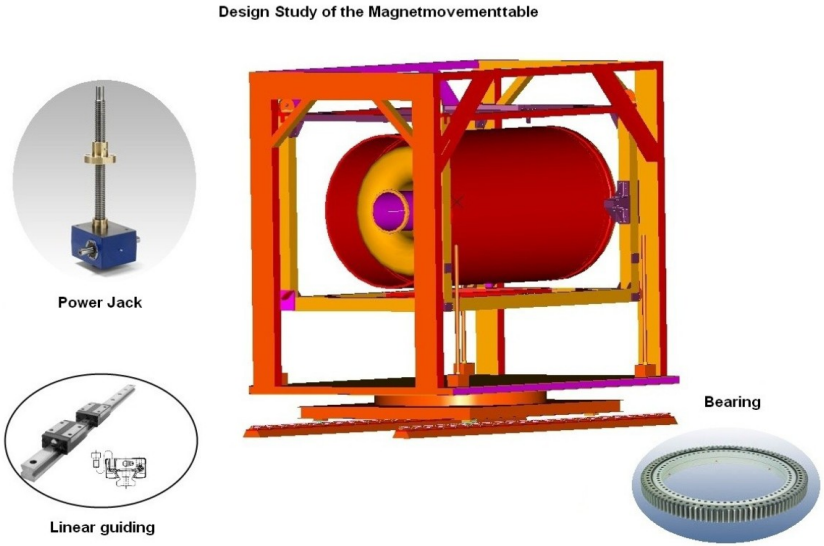




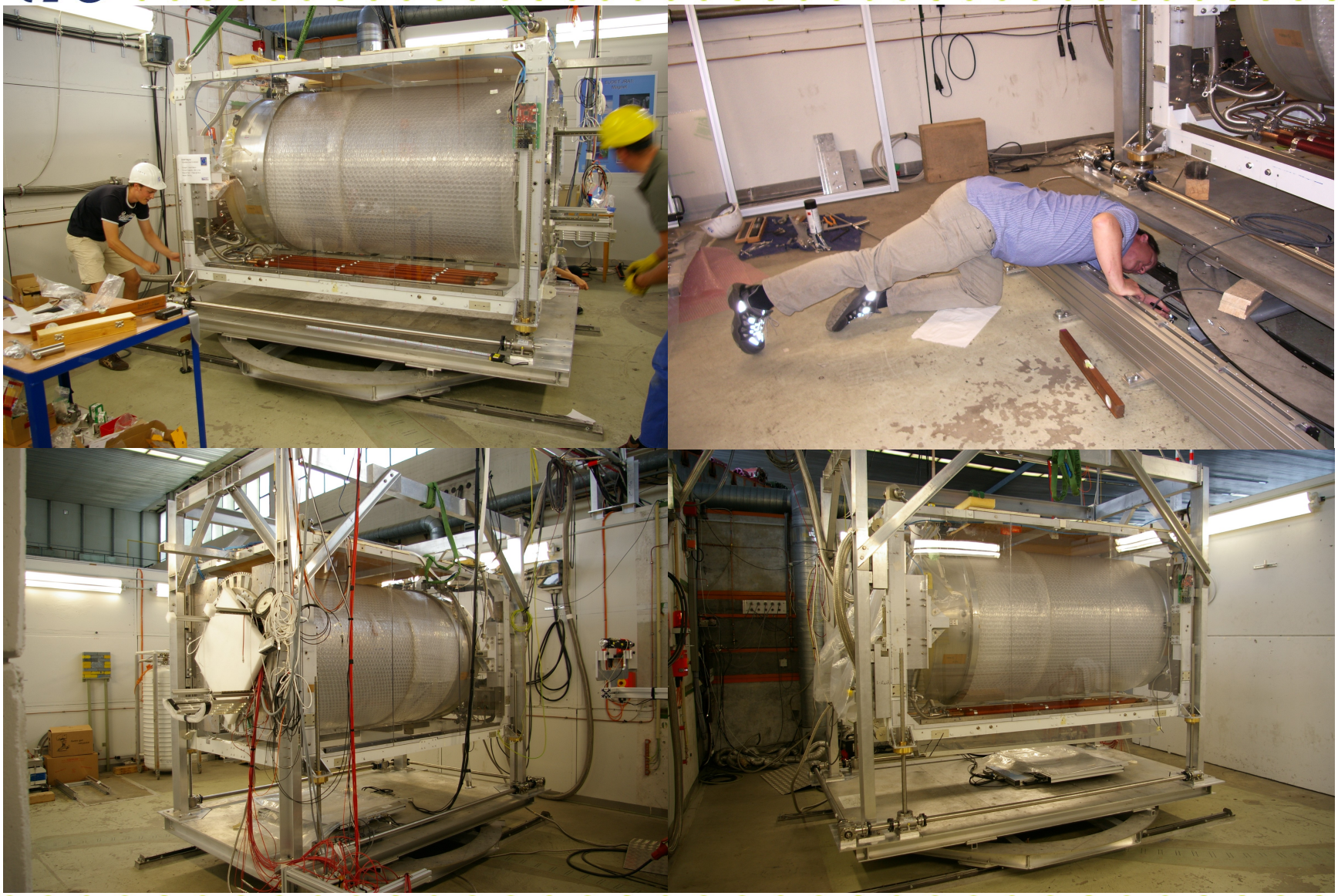
Support structures:

- TPC
- PCMAG

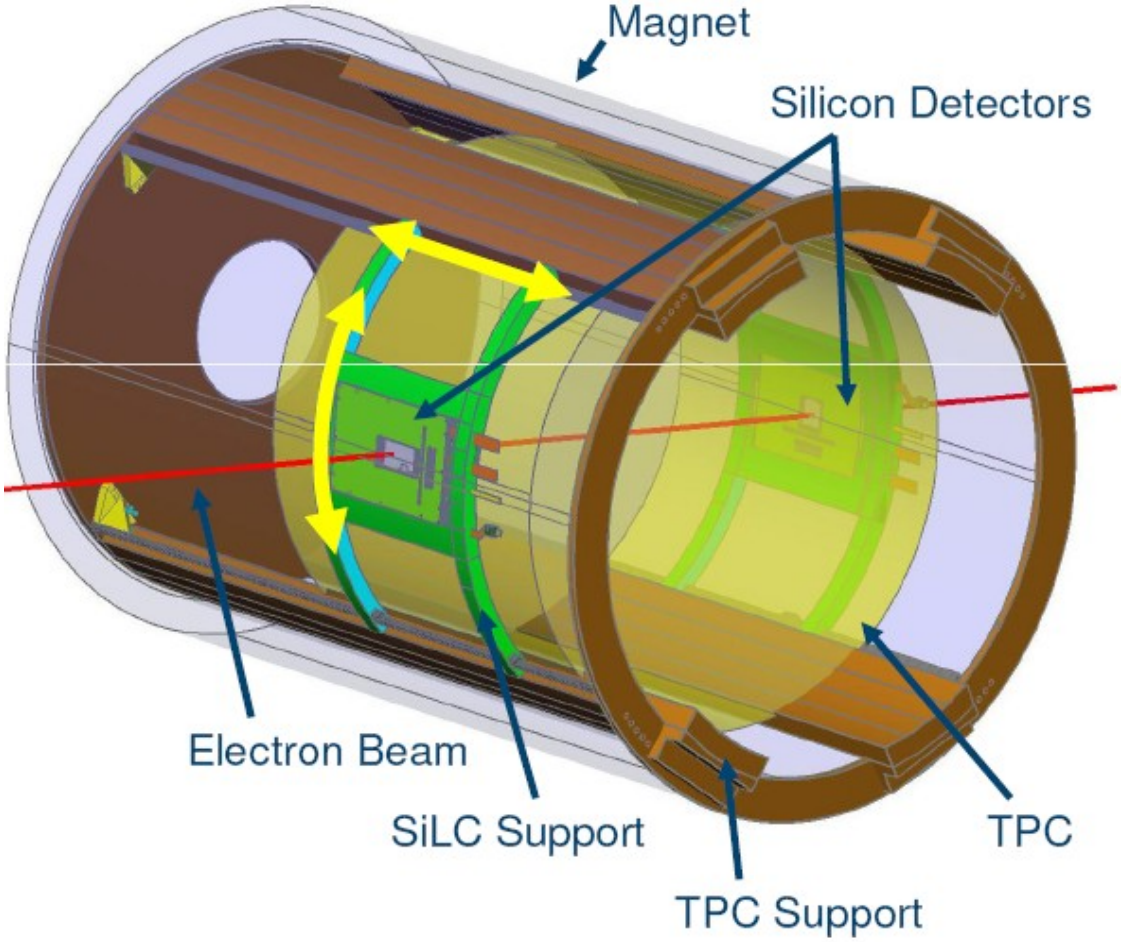
F. Hegner, V. Prahl, R. Volkenborn, DESY

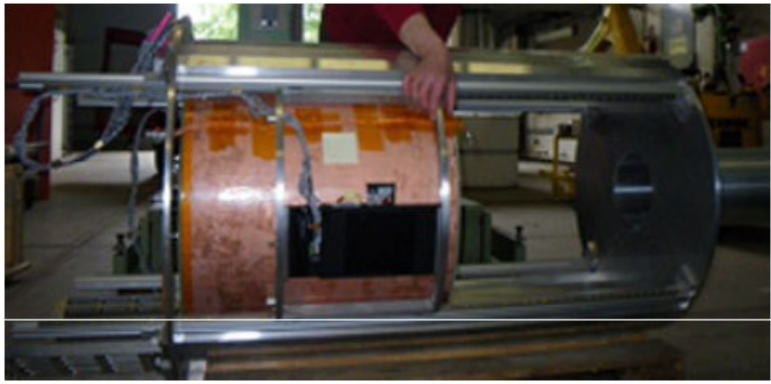


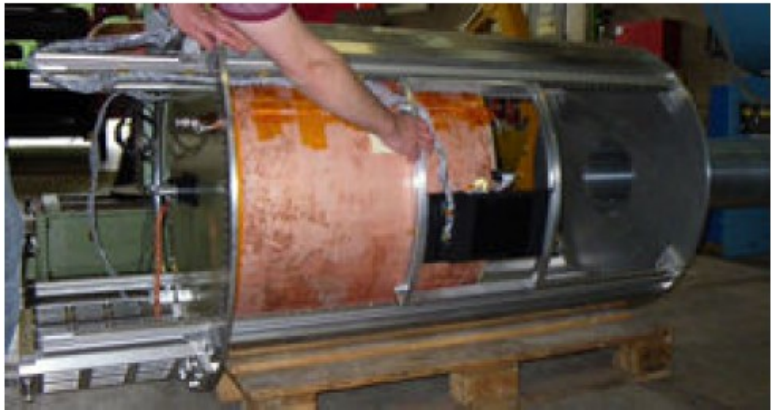
LP Mechanics



Si Envelope

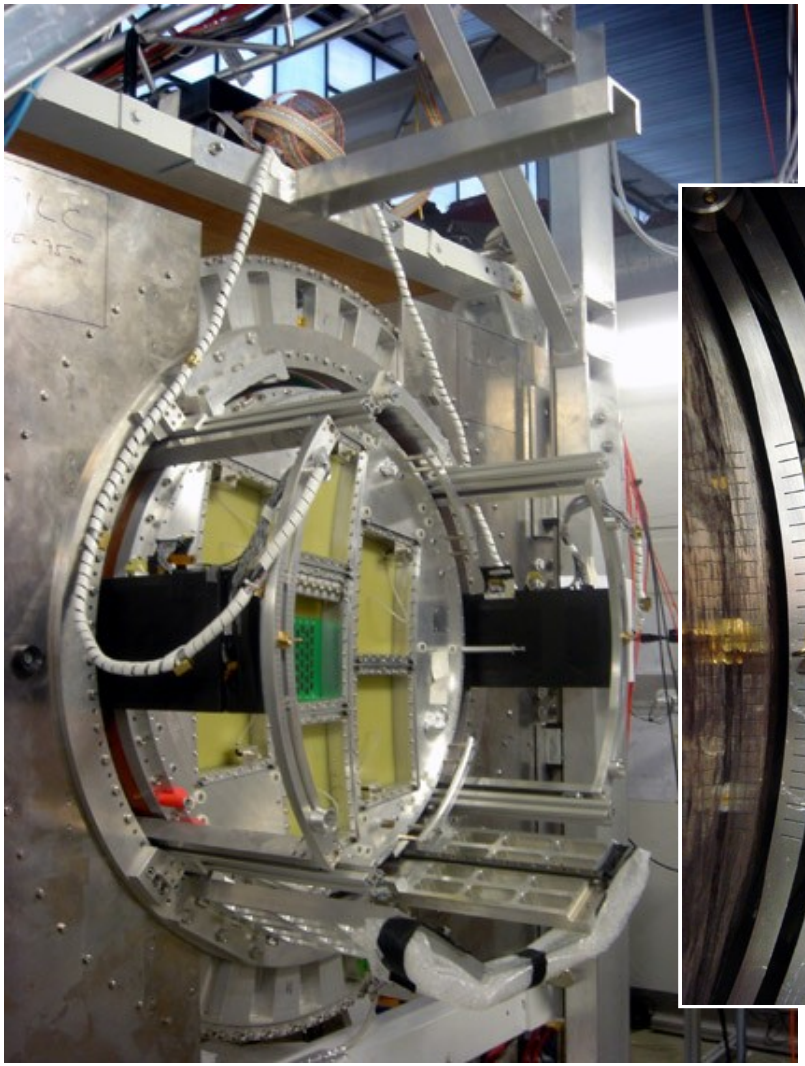




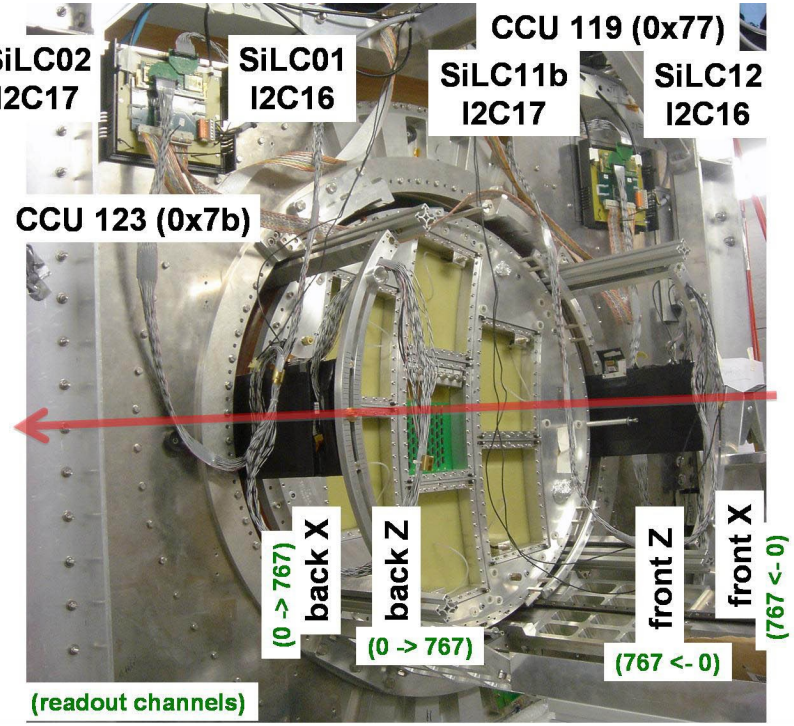


S. Haensel
HEPHY Vienna

Si Envelope



Combined test beam campaign with two Micromegas modules in Nov. 2009



S. Haensel
HEPHY Vienna

Readout Electronics: S-ALTRO

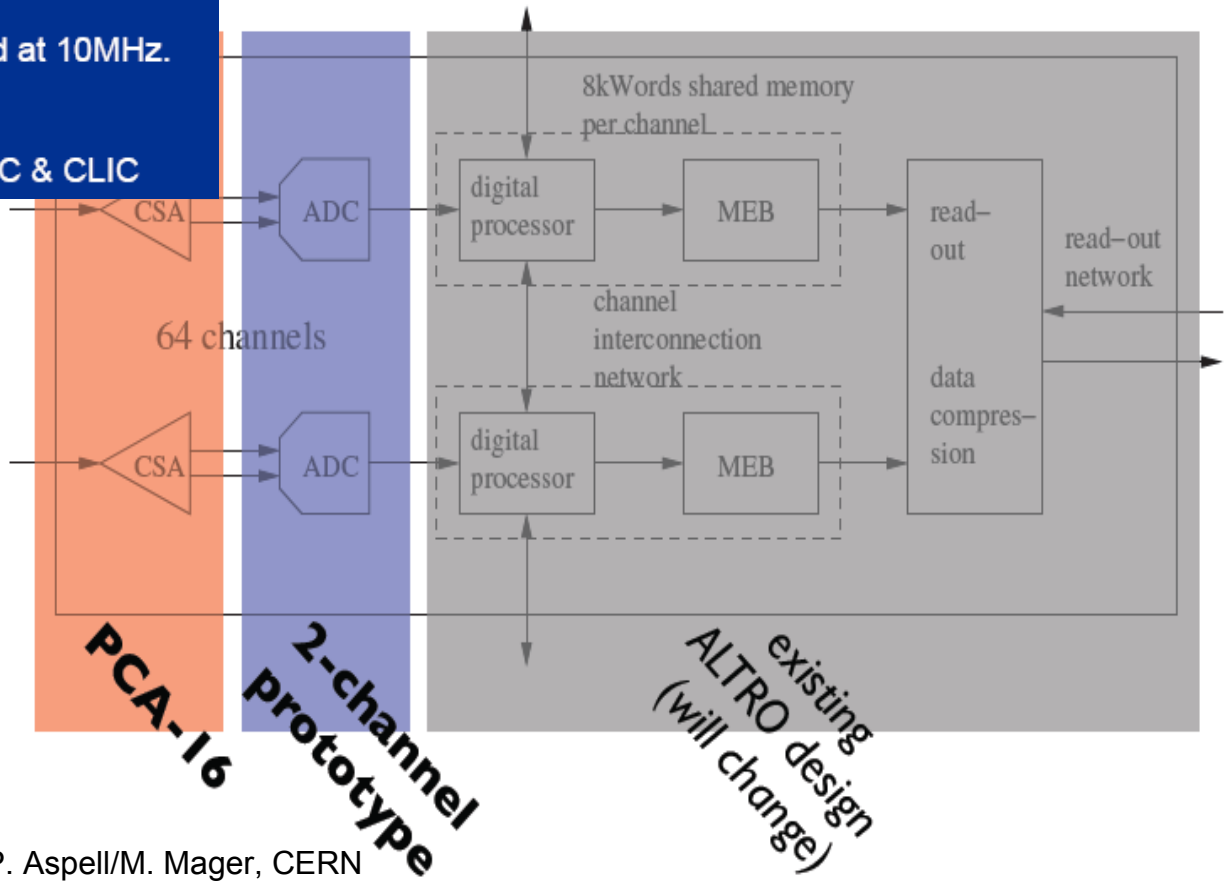
Goal :

To demonstrate integration per channel of an analog front-end, an ADC and digital signal processing in a single chip.

Data processing of 100us of data sampled at 10MHz.

Prepare ideas for TPC readout in the ILC & CLIC

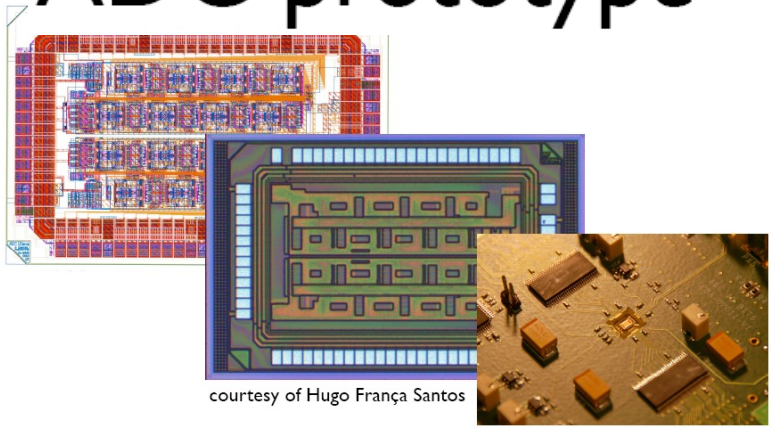
Current Design



P. Aspell/M. Mager, CERN

Readout Electronics: S-ALTRO

ADC prototype

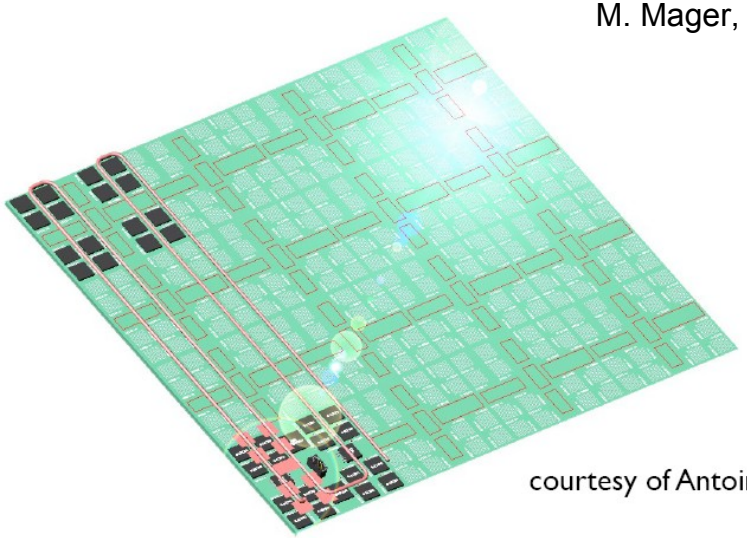


courtesy of Hugo França Santos

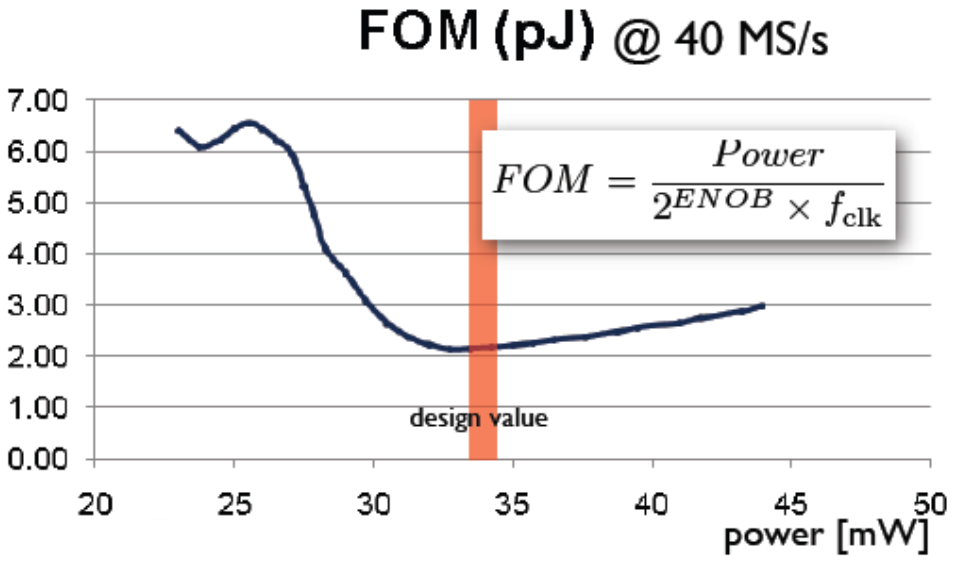
Single ADC area: 1.57 X 0.45 = 0.7 mm²

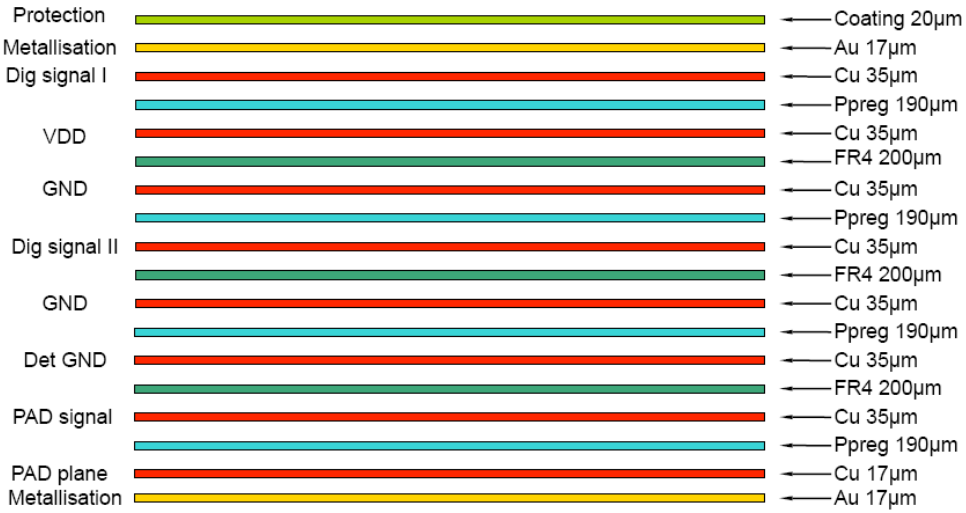
Prototype area: 2.35 X 1.6 = 3.76 mm²

M. Mager, CERN



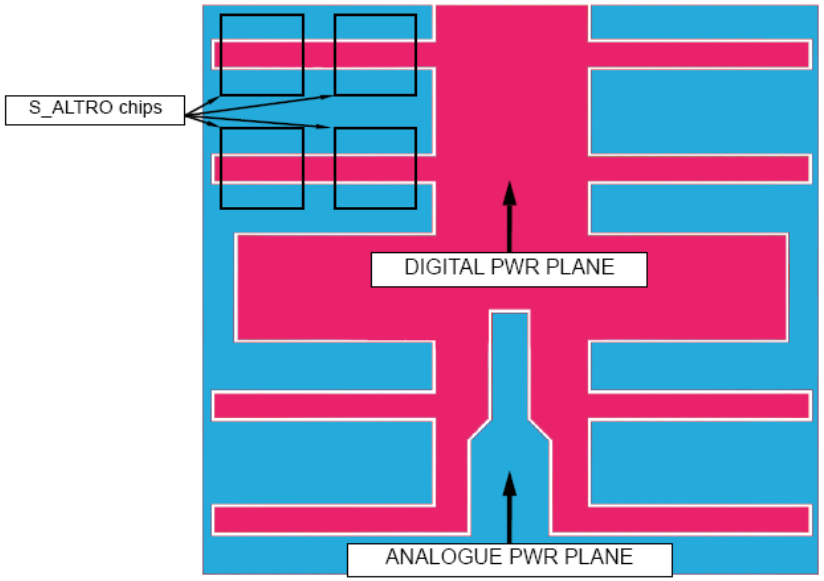
courtesy of Antoine Junique



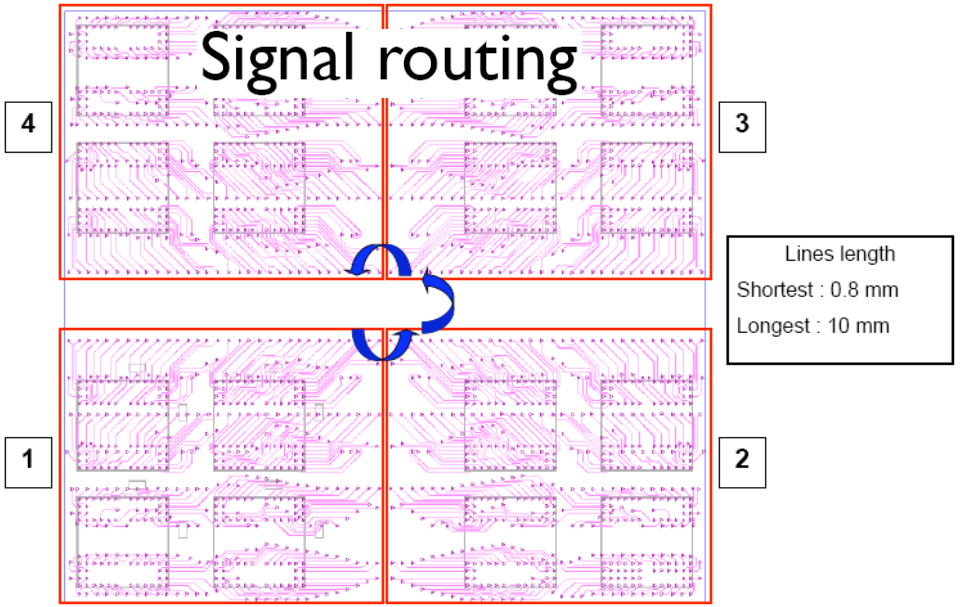


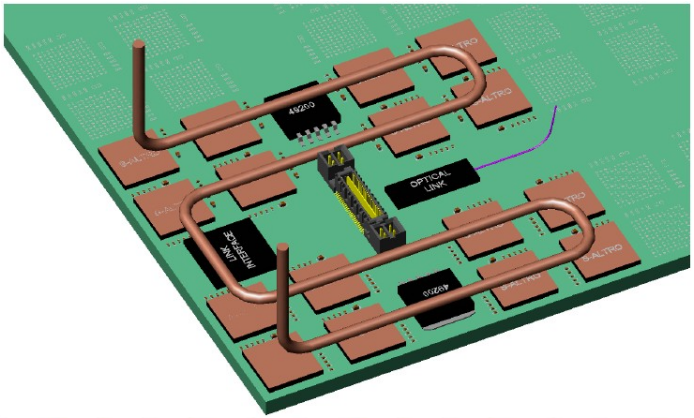
Readout Electronics: S-ALTRO

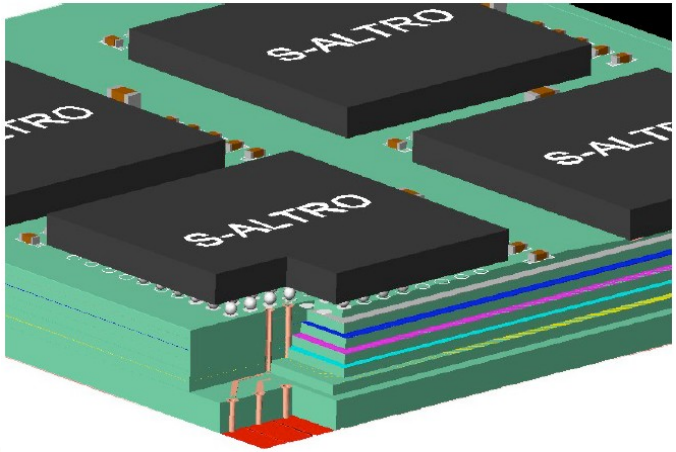
Power distribution



M. Mager, CERN







Readout Electronics: S-ALTRO

Goals for the S-Altro16 electronics prototype:

The prototype pad modules has to fit into the present endplate

The chip size should be compatible with a realistic pad size. The final goal is to get down to 1x4 mm^2 pad size. The present pad size is about 1x5 mm^2 and the prototype should be compatible with similar size.

Power pulsing should be prototyped.

A solution for efficient cooling has to be found.

A realistic noise level should be achieved.

Experience with the S-Altro16 chip should guarantee a safe final step to the S-Altro64 chip.

L. Joensson, Lund Univ.

Readout Electronics: S-ALTRO

The are obvious disadvantages in mounting all the electronics directly onto the pad module.

Instead a system with Multi Chip Modules is proposed.

It is a fairly conservative approach, reducing the risks.
Cheaper to produce
It has several advantages in the prototyping phase.
It provides realistic prototyping for safely taking the final step to the S-Altro64 chip.
It offers better separation between analogue and digital circuitry and it offers great flexibility in terms of how the electronics components are organized.
The size of the MCM for the S-Altro64 chip is compatible with
1x4 mm^2 pads
It can be easily moved from a system with GEM readout to a system with MicroMegas readout.
Its modular structure allows re-design of the readout chain without affecting the pad board

L. Joensson, Lund Univ.

Summary & Outlook

- Gas-/HV-infrastructure
- Infrastructure for LP present and being used
- Infrastructure for SiLC envelope installed
- LP assembled, commissioned and being tested
- LP with three different amplification technologies operated
- First SiLC run performed
- ~22 weeks of test beam with LP operation so far
- >10M events recorded → ~2TB data on GRID
- → more to come

Summary & Outlook

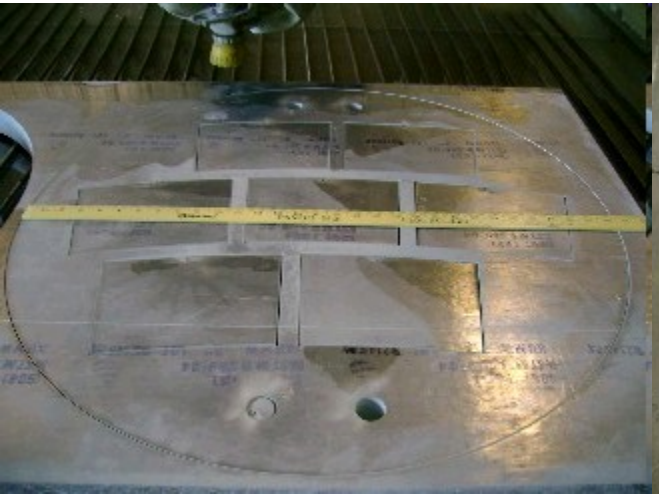
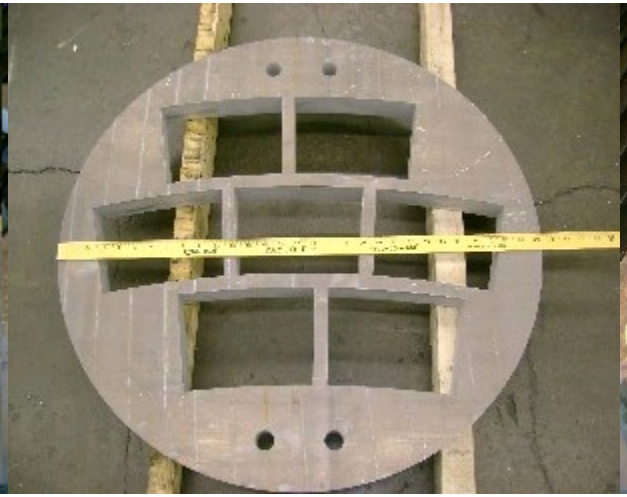
- Items not yet completed:
  - Alignment system for LP within PCMAG to be tested/installed
  - Slow control to be (further) developed
  - Automation of processes
  - DESY GEM module
- Further test beam campaigns for this/next year:
  - Backplane integrated 7,500 channel readout system, based on ALTRO electronics → just completed
  - Seven Micromegas modules with AFTER electronics attached to the modules (in 2011)
  - DESY-GEM module with ALTRO electronics (end 2010?)
- PCMAG modifications in 2011
- S-ALTRO16 to be prototyped

The Goals and their Status

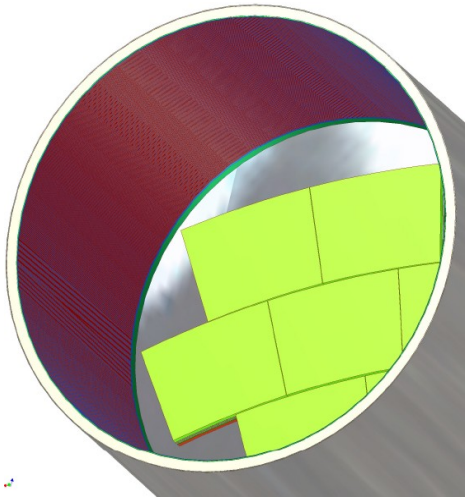
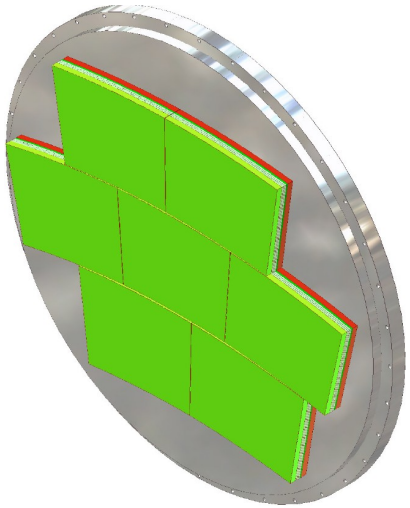
Milestones of JRA2/TPC

Milestones for the TPC development facility		
Milestone	**Expected Date**	**Status**
Preamplifier prototype board ready	2007	Available
Field cage available	2008	Available.
DAQ prototype available	2008	Available
Prototype compact readout system ready	2009	In Progress
Final report	2009/10	To Be Done

End Plate for Readout Modules

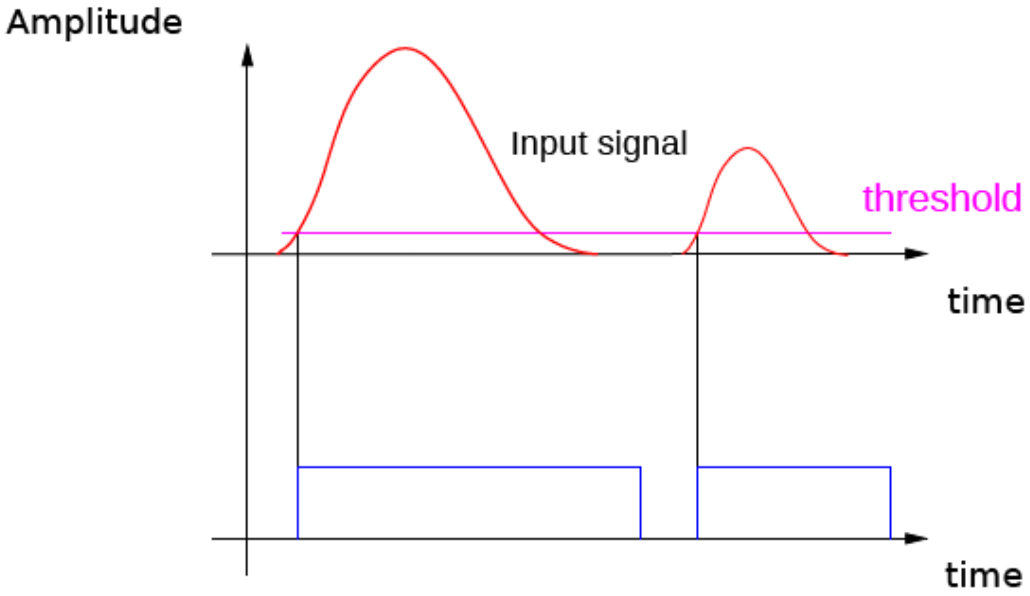





D. Peterson, Cornell

Readout Electronics: TDC



Output digital signal from QTC

Data zero suppression by analogue data processing.

Here example with threshold timing and charge-to-time conversion.

- The time of arrival is derived using the leading edge discriminator.
- The charge of the input signal is encoded into the width of output digital pulse.

A. Kaukher, Univ. Rostock

Readout Electronics: TDC

A. Kaukher, Univ. Rostock

Readout Electronics: TDC

No results with GEM Modules, yet. Higher gas gain is necessary.
Currently, VME crate is not prepared to work in (stray) B-field.

It is planned to use a Micromegas Module. Higher gas gains are possible. Larger area can be covered.

Next step:

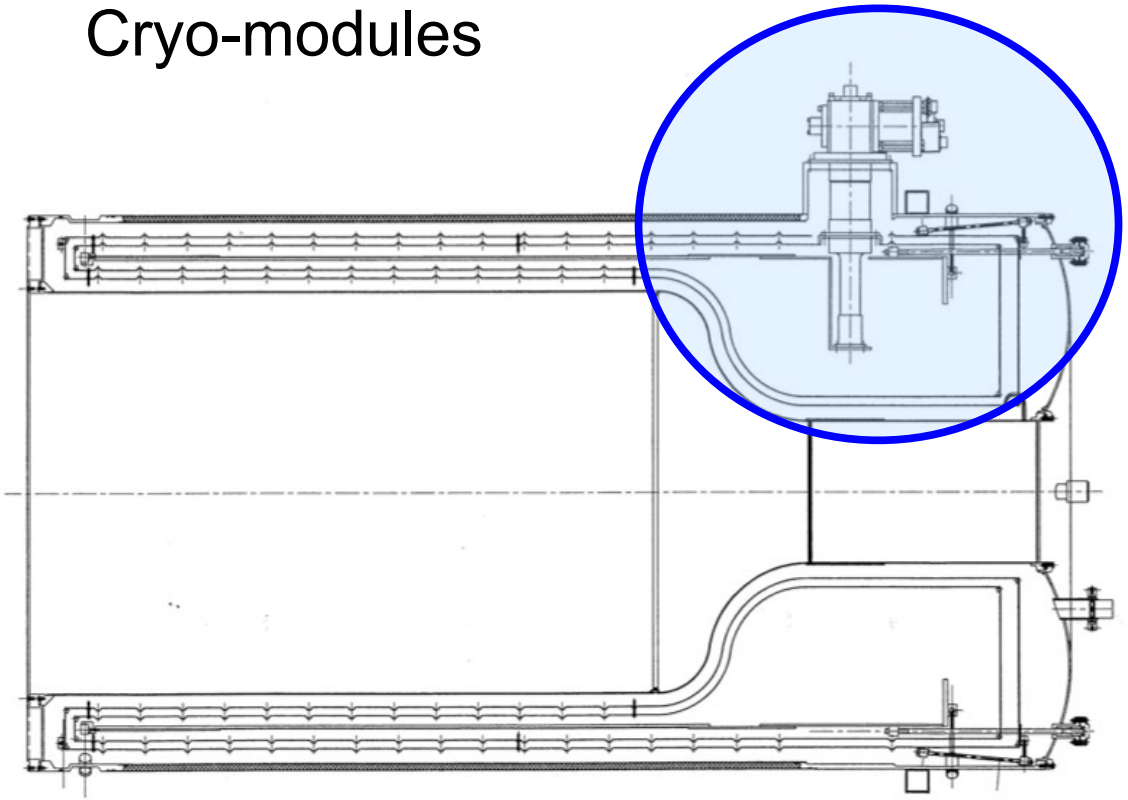
- Threshold / efficiency scan,
- Charge-to-time conversion parameter (QDR) scan,
- Z-scan in LPTPC.

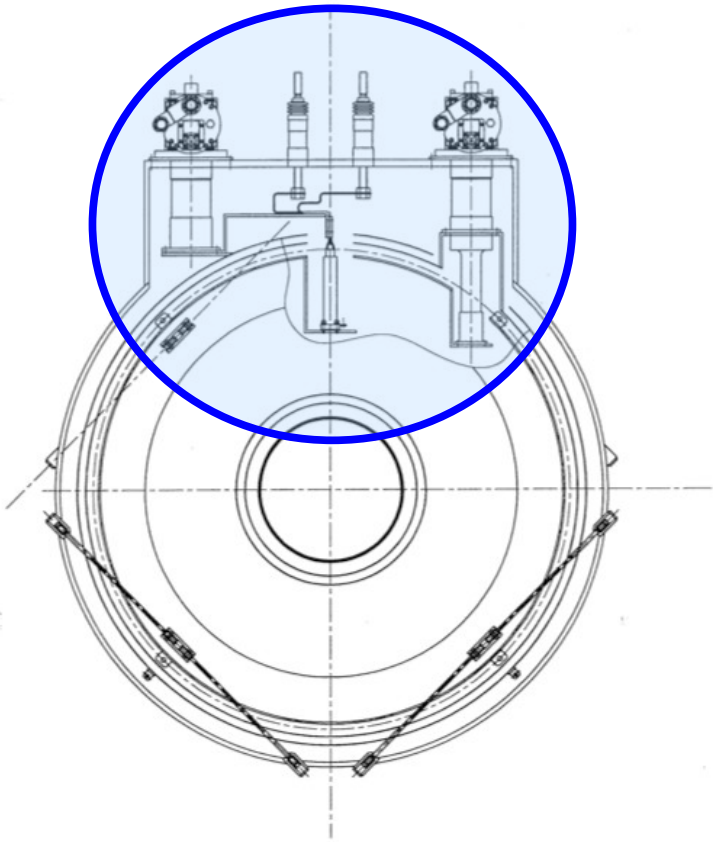
Signal simulation for a GEM detector is being prepared.
Last milestone (31.12.2009) to be reached in time.

A. Kaukher, Univ. Rostock

PCMAG Modification

Cryo-modules





Modification planned for 2011 → ~6 months duration, after “finishing” beam tests