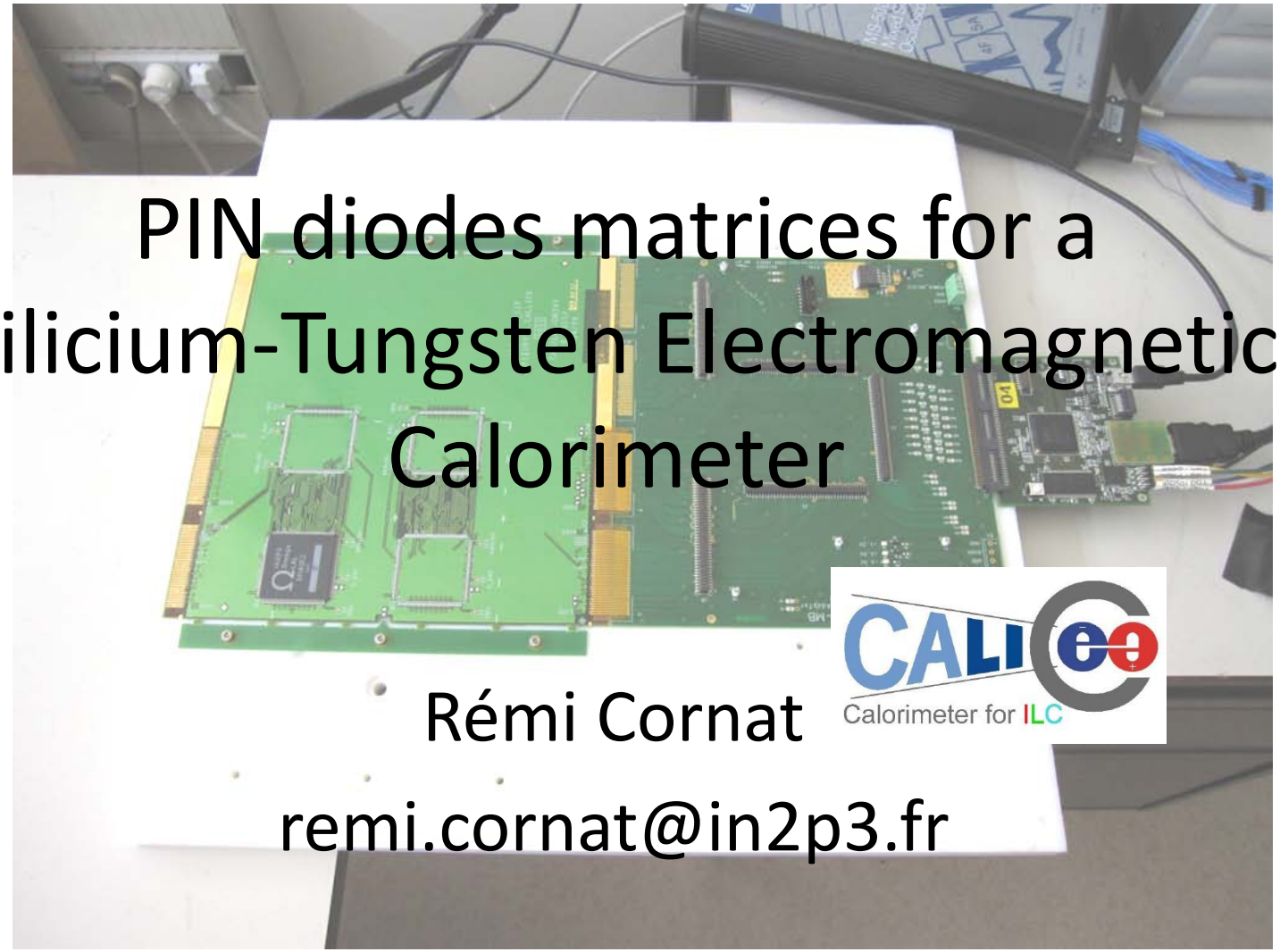
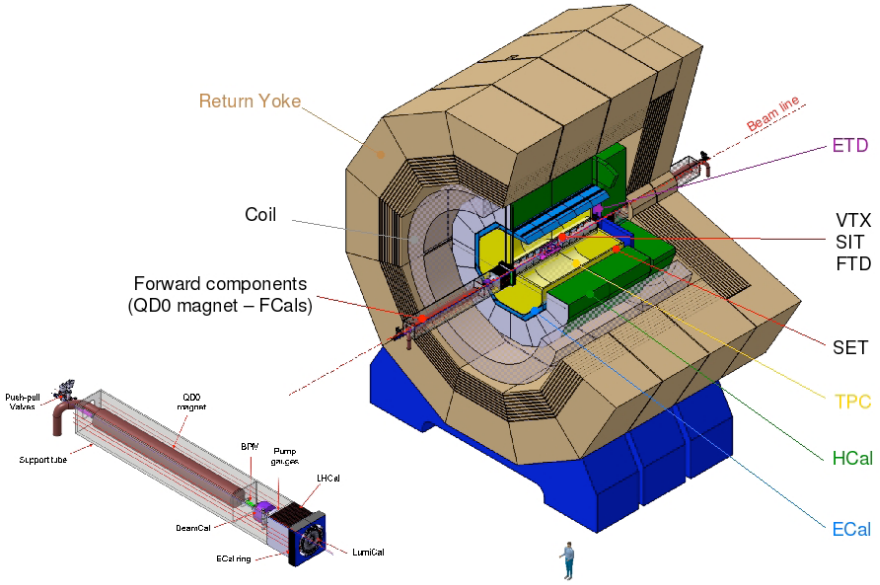


PIN diodes matrices for a Silicium-Tungsten Electromagnetic Calorimeter

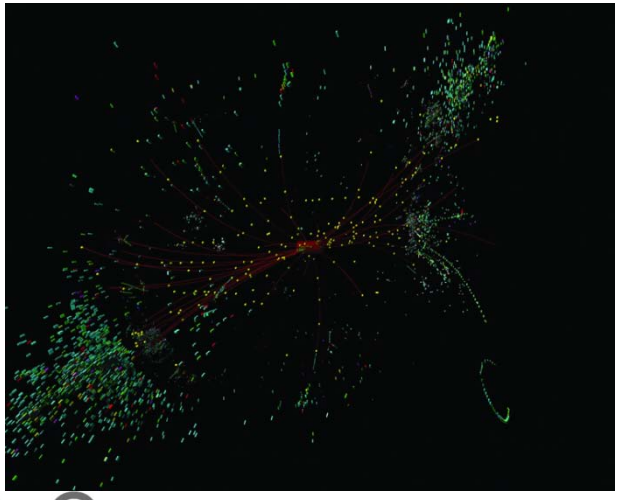
Rémi Cornat

remi.cornat@in2p3.fr

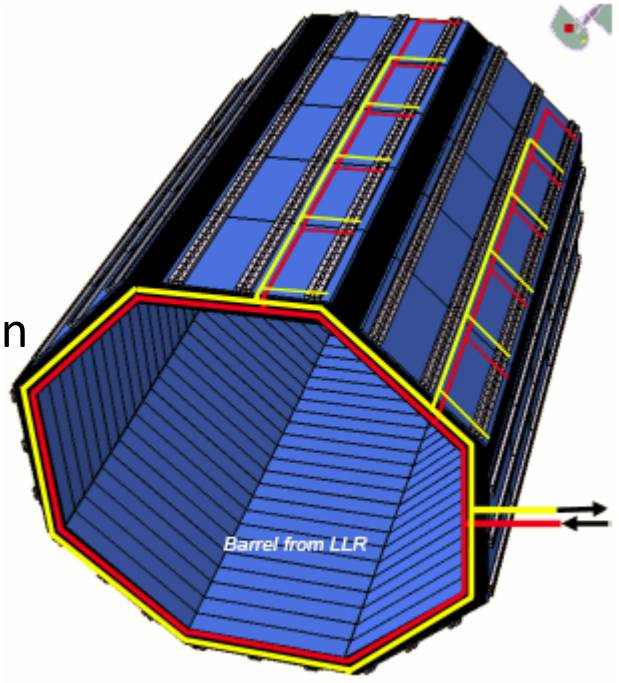
ILD concept detector



Ultragranular detectors
In 4T B field
Very low power dissipation

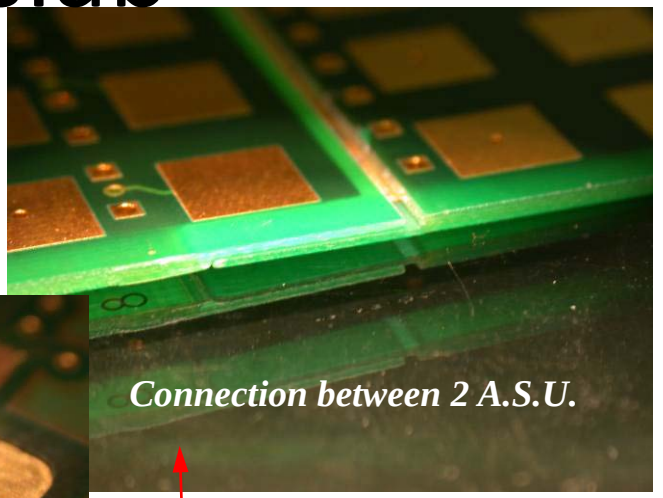


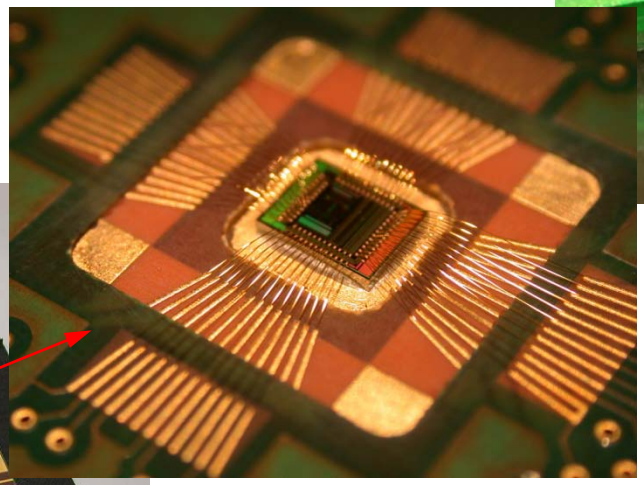
« Imaging calorimetry »
High density of detection cells in 3D
10000 channels / dm^3



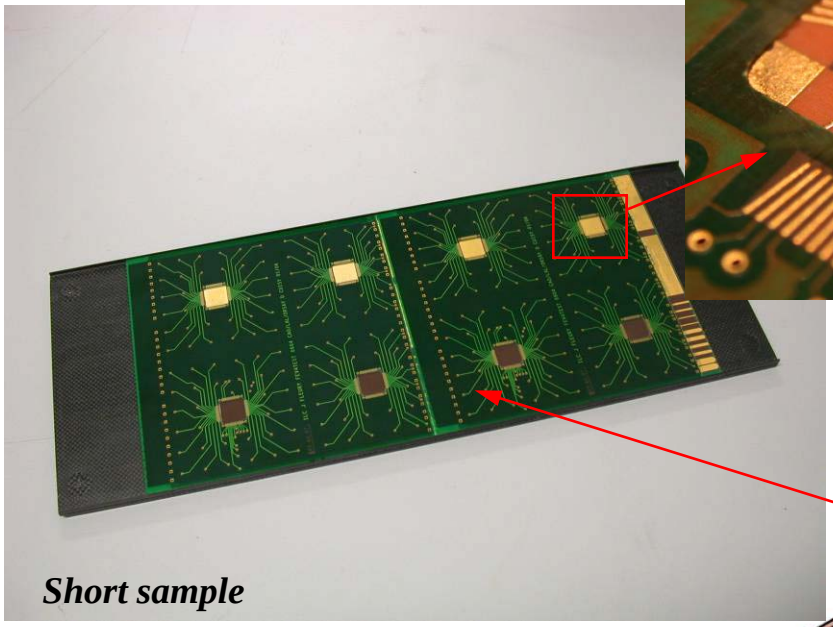
ECAL detector slab

Slightly relaxed mechanical constraints : ILD + 0.4 mm





Chip embedded



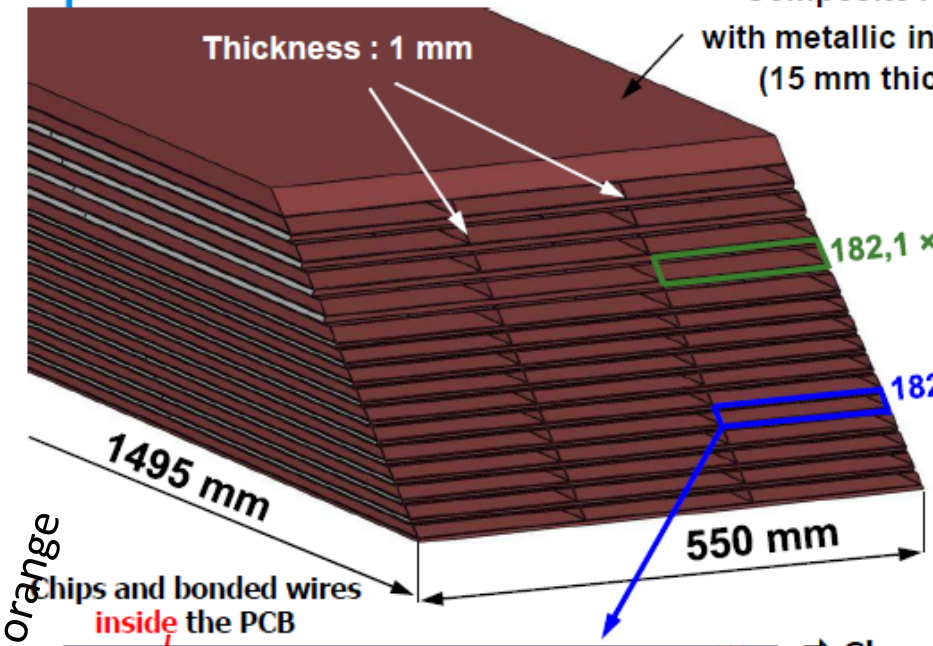
Short sample

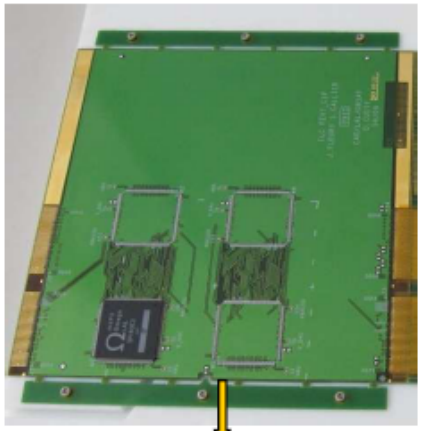
A long SLAB and a tower made up of short SLABs (30 layers)

Detector design

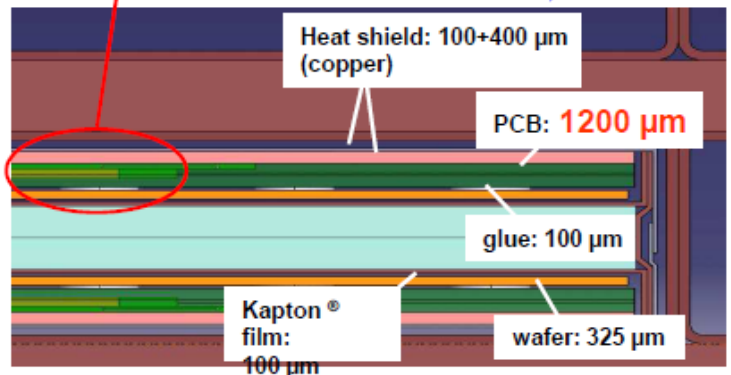
Sandwich made up of tungsten PCB and silicon. Slide into a composite carbon fibre structure

EUDET design





Silicon wafer in orange

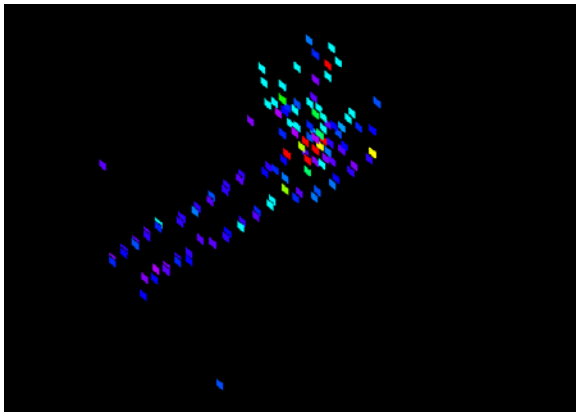


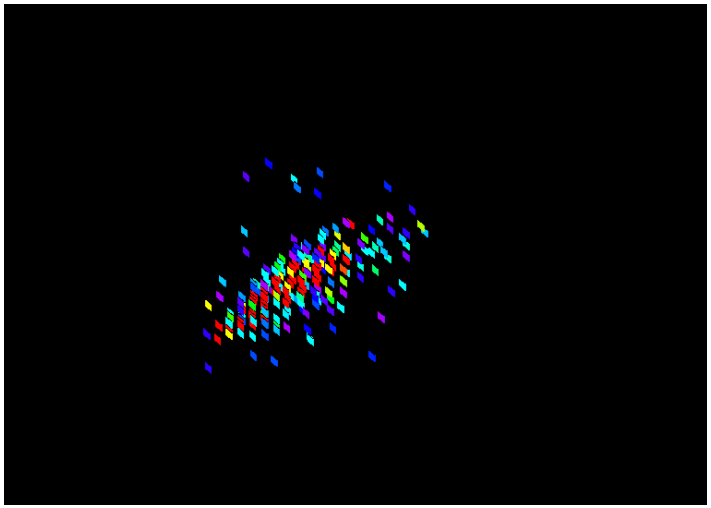
- ⇨ Clearance (slab integration) : 500 µm
- ⇨ Heat shield : 500 µm → Thermal demonstrator
- ⇨ PCB : 1200 µm → but 1100 µm used
- ⇨ Thickness of glue : 100 µm
- ⇨ Thickness of wafer : 325 µm
- ⇨ Kapton® film HV : 100 µm ? → tests
- ⇨ Thickness of W : 2100/4200 µm (± 80 µm)

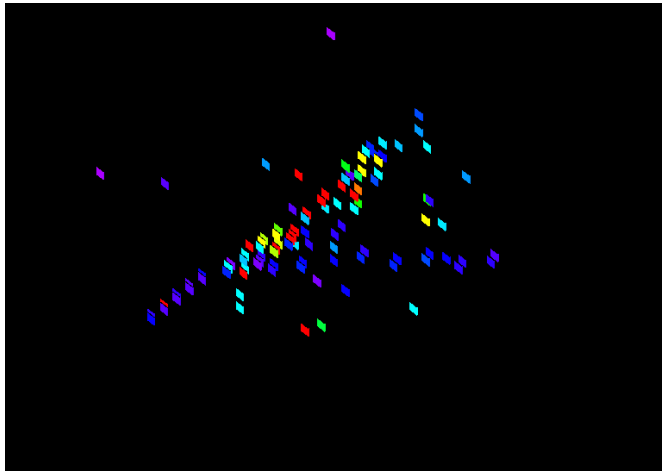
Chip embedded

Experimental data

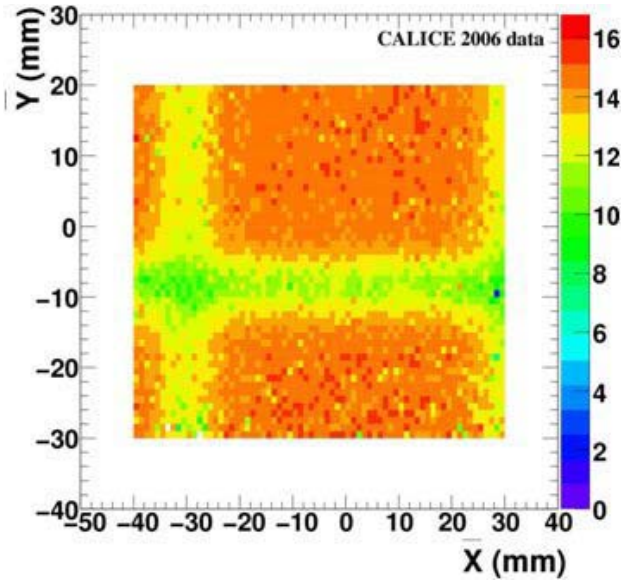
2005 prototype

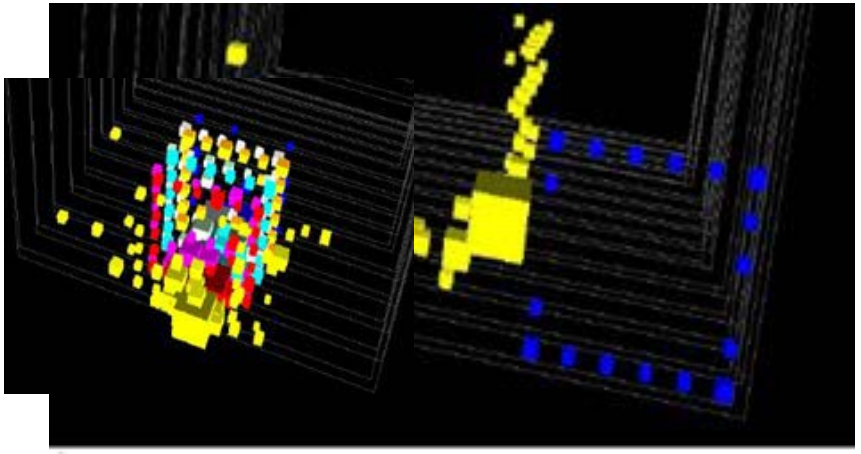






2 effects





Peripheral dead zone : -20% of detection efficiency

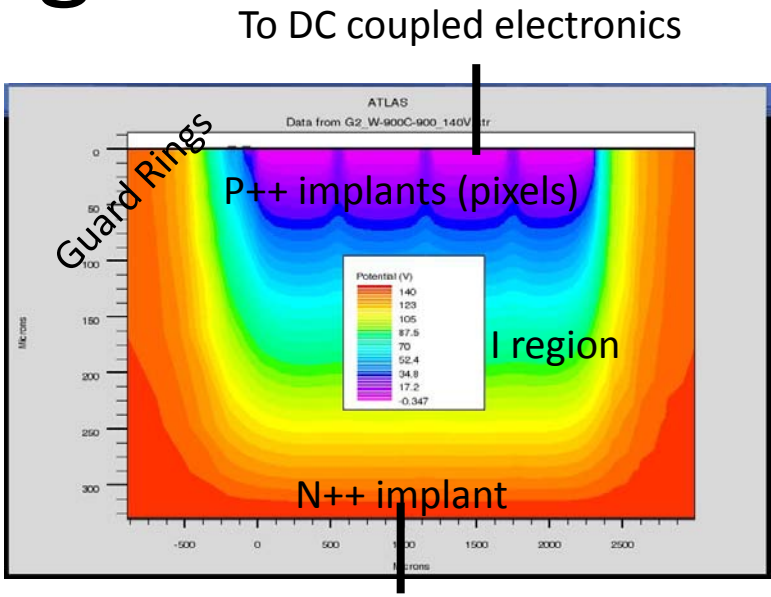
Can be compensated (off line)

« square » events : crosstalk beetween guard rings and peripheral pixels

Should be reduced by a factor 50 to 100

Sensor Design

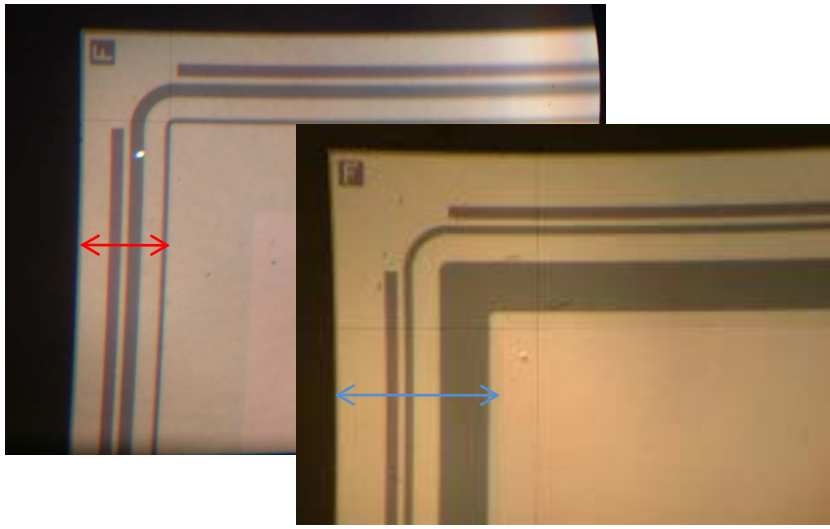
- Glued on PCB
- Guard rings are not biased
- Possibility to wire bond the GR
- Assumption that the simplest design allow to control the cost
  - Few thousands of m² needed for ILD
  - Up to 400 000 matrices
- New versions should optimize
  - Width of the dead zone at the edges
  - Crosstalk level between GR & pixels (Square Events)
- Financial viability would be insured for costs of about 2 € /cm²
  - 70 keur (including NRE) for 40 pcs of this hamamatsu prototype = 22 € / cm2 (14 w/o NRE)



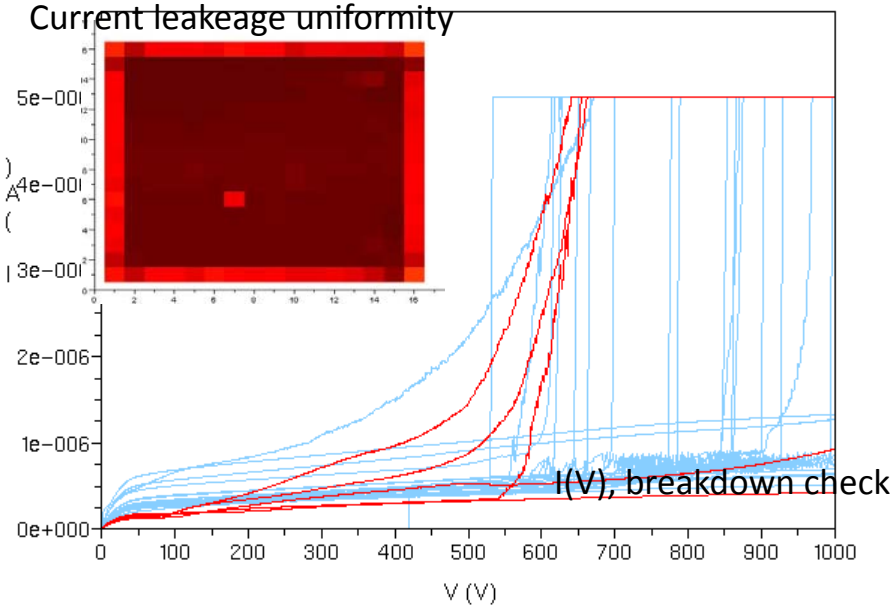
9x9 cm², 324 or 256 pixels

Hamamatsu sensor V2

- Dead area decreased to 750 um (1200 µm previous)
- Leakage current issue seen at Hamamatsu
  - Level: x 5-10 wrt previous sensors ,
  - non uniformity
  - new test setup : better!
- 5 samples + production batch of 35 pcs
- Breakdown ok but seems to be slightly lower
- Have 40 sensors to start EUDET SLAB assembly (160 needed)



I(V)



Alternate designs

- Alternate designs are possible
  - Allowing to reduce overall cost
  - Better integration in the detector
- Changes in dimensions
  - 6x6 cm or smaller but with small dead space at the edges
  - Thinckness up to 1mm (change in electronics gain)
- Relaxed constraints on electrical properties
  - Current leackage up to 10 nA per pixel
  - Vbreakdown =~400 V
  - Accept spread or non uniformity (if random) but with sorting (done at LLR)

Pending questions

- Change in design requests
  - what parameter(s) should we modify to allow cost reduction ? (trends)
  - Level of expected cost reduction ?
- GR bonding (last design)
  - Optimal bias voltage ?
- Lowering the width of the dead zone
  - Change the GR ?
  - Impact on cost ?
  - Impact on crosstalk ? (with or w/o bonding)
- Crosstalk
  - What about CTR ? (feasibility, impact on cost)
  - Split guard rings ?
- PhD student ?

Design (call of offers)

The LEPRINCE-RINGUET laboratory is asking for the manufacturing of P-I-N diodes matrices including 16 x 16 pixels on a 81 cm2 square shaped surface. A minimum of 30 matrices are expected. The mask layout of some given layers will be provided by the LLR or one of its partners. It will be based on the technological characteristics given by the contractor. The sensors must be compatible with a bias voltage comprised between 150 V and 300 V with a leakage current below 5 nA as the mean value per diode.

The silicon substrate is type N silicon with a resistivity greater than 4kΩ.cm. The wafer thickness must be 320±10 µm and must be provided by the contractor. The crystal orientation has no influence.

Tab 1 : Résumé des caractéristiques du substrat
Summary of the substrate characteristics

	Min.	Typ.	Max.
N type silicon	-	-	-
Resistivity (kOhms.cm)	4	5	-
Thickness (µm)	310	320	330
Width (mm)			90

Thickness :
Could be 500 µm up to 1000 µm, if justified by cost reduction

Width could be downsize to 6 cm, if justified by cost reduction

Design (call of offers)

For example, the table 3. gives the expected characteristics:

Tab 3 : Propriétés électriques (conditions typiques)
Typical electrical properties

	Min.	Typ.	Max.
Courant de fuite d'obscurité (nA/pixel) Dark current per pixel	-	2	6
Courant de fuite d'obscurité total (nA) Total dark current	-	650	1000
Tension de déplétion complète (V) Full depletion voltage	-	-	120
Tension dite d'avalanche (« breakdown »)	300	-	-
dC/dV @ V_{nom}, matrice totale (pF/V) dC/dV @ V_{nom}, full matrix	-	1	2

The constraints of the integration of the matrices within the detector prevent any other external connections than the access to the pixels. The guard-ring (GR) or equivalent structure can therefore not be biased. Nevertheless, for test purpose, bounding pads can be placed on the GR (located in the middle of the sides).

The GR width has to be as low as possible (dead zone for the detection). The capacitive coupling between the guard-rings (or equivalent) and the pixels must be minimized.

Dark current @pixel :
Define a distribution ?
0.5-1% out of range pixel are acceptable
Typical value could be increased

Impact of dC/dV constraint ?

Design (call of offers)

The wafers are glued thank to the EPOTEK E4-110 glue. The passivation technique has to be compliant with this glue. The dark current and the full depletion voltage must not vary within a 20% range from the typical values (the bias voltage remains the same).

The pads for gluing should be slightly larger (typ. 4 mm) than the glue dot dimensions (from 3 to 3.5 mm).
The common electrode is glued with a 30 mm glue dot.