

ILD Software Working Group

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Silicon Tracking System

One of the goal of the SiLC collaboration

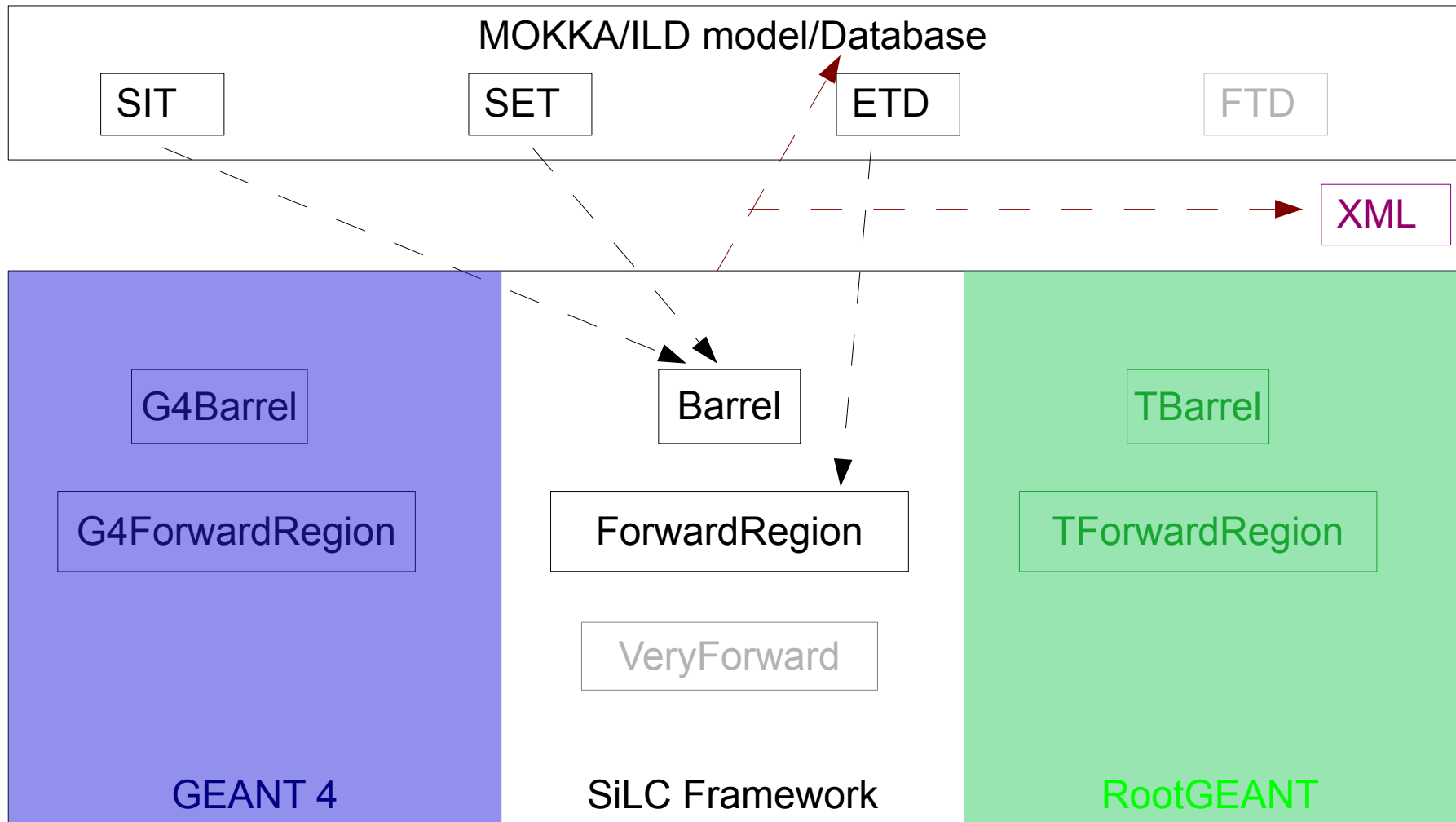
- Resume the optimisation studies of silicon trackers
- develop a tool to facilitate the optimisation studies
- provide drivers for ILD concept (and other experiments CLIC)

Main ideas

- Generate different kind of geometry very easily (number of silicon layers, false/true double-sided, technology ...)
- Possibility to introduce mis-alignment studies according a mechanical structure
- Materiel budget effects induce by the support and the cabling
- Could be used in different framework

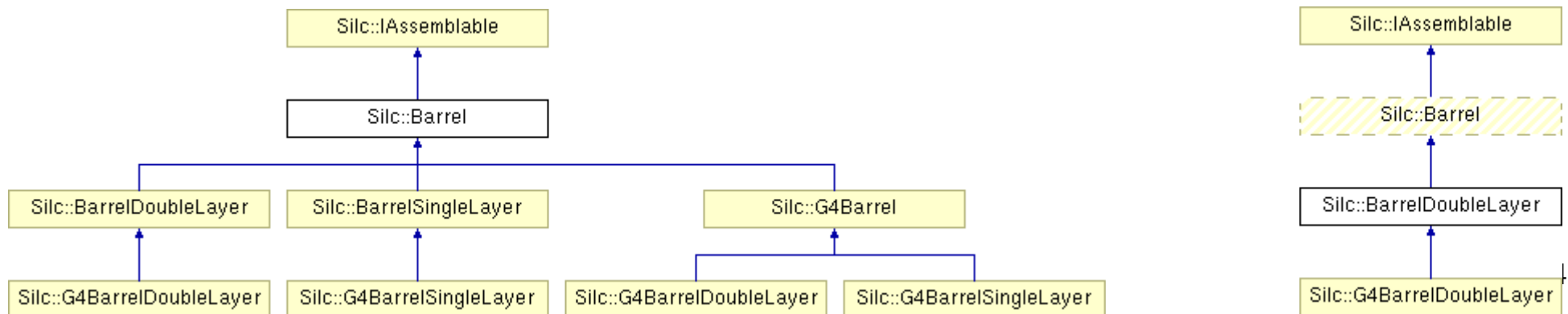
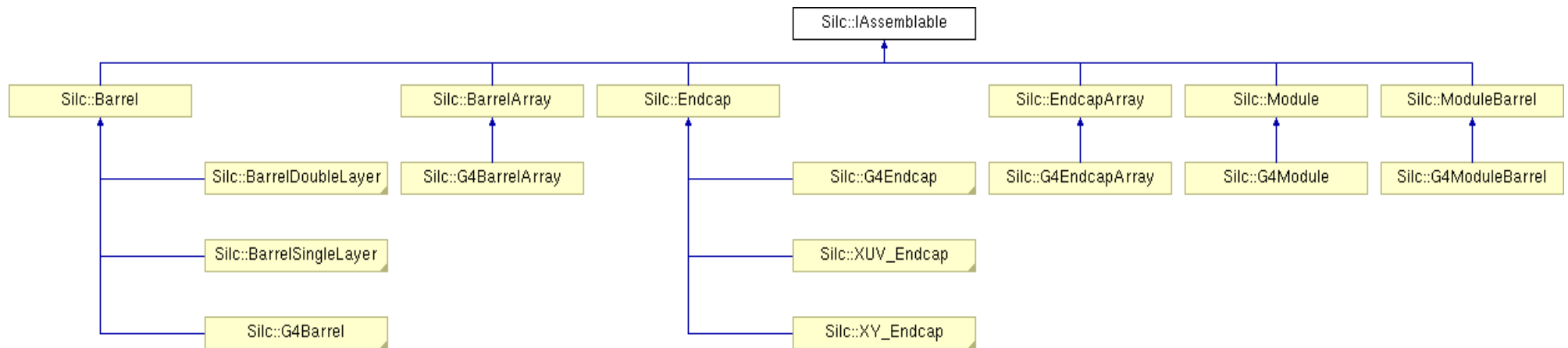
Silicon Tracking System

Code description



Silicon Tracking System Design Pattern

Common class for the Silicon Tracking Detectors



Silicon Tracking System

Silicon Module Detector

- **Baseline**

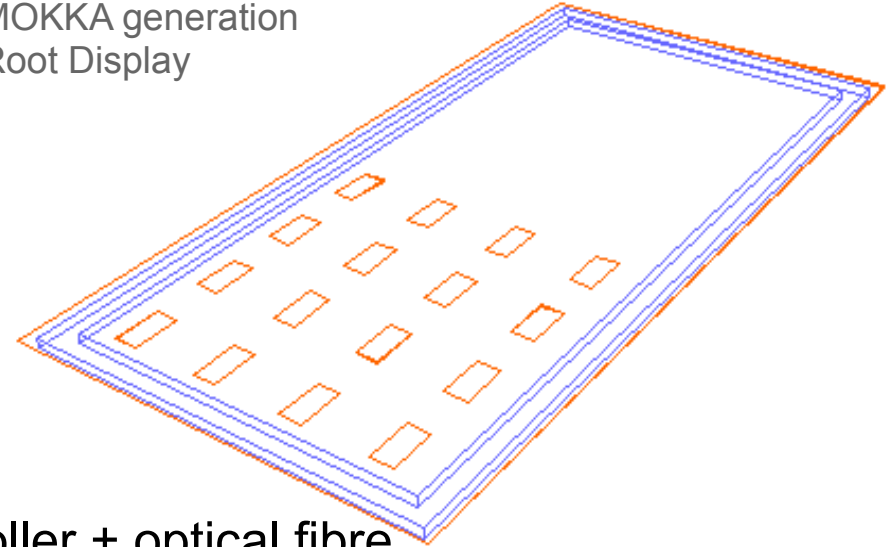
- 100.12*100.12*200 mm²*μm
- Strip technology
- 50μm pitch (~2048 channels)
- Edgeless
- Chips on board: SiTr130-128+ controller + optical fibre

→ A silicon module consists into n chained silicon sensors

- **GEANT 4 description**

- Module size: 1*n sensors+gap
- The module segmentation and the sensors misalignment (rotation+shift) are included in the digitisation process
- Chip+controller included

Silicon module (1*2 sensors)
MOKKA generation
Root Display

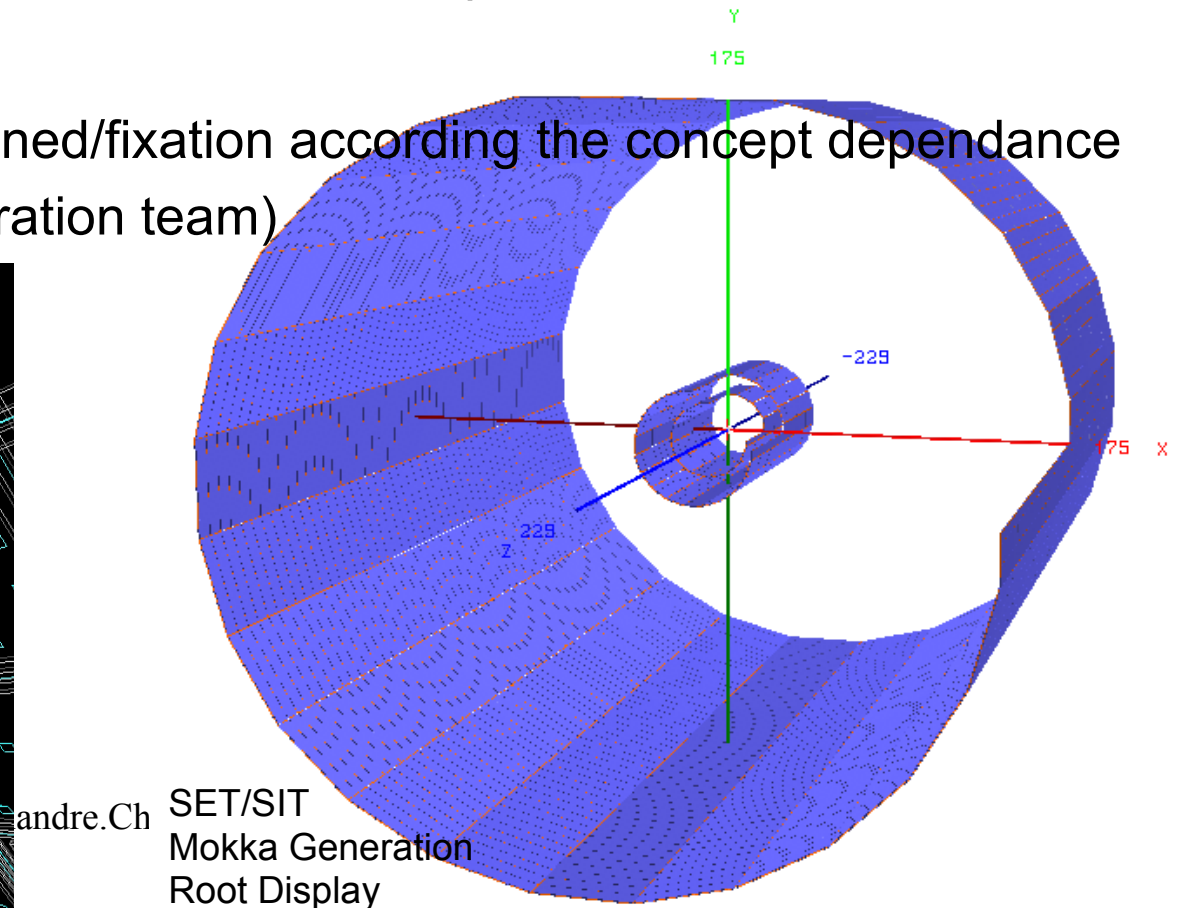
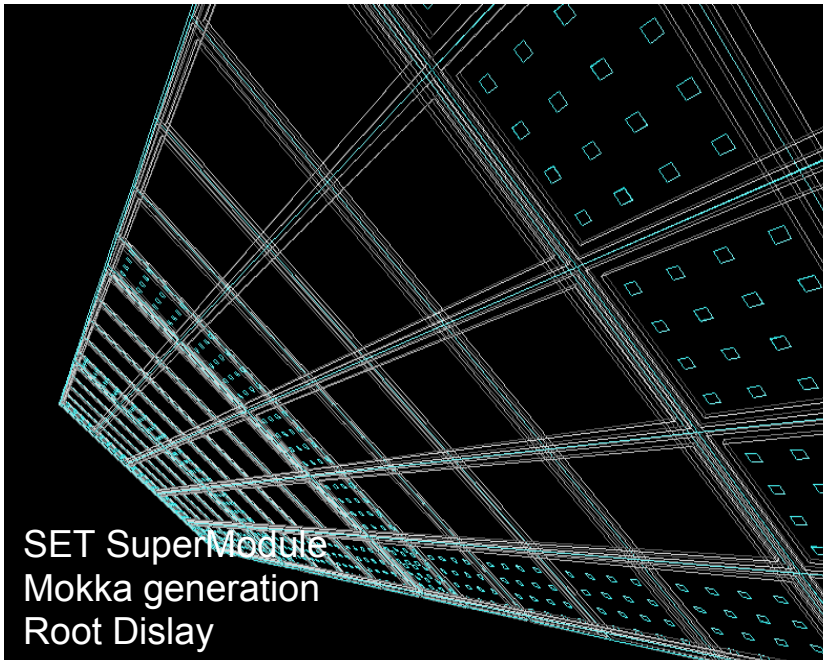


Silicon Tracking System

SIT/SET

- Description:

- Using the edgeless properties
- false double sided strip detectors
- Gaps: 50 micron gap between modules, Super Module, Detection Element
- Support:
 - SET → partially defined/fixation according the concept dependance
 - SIT → waiting integration team)

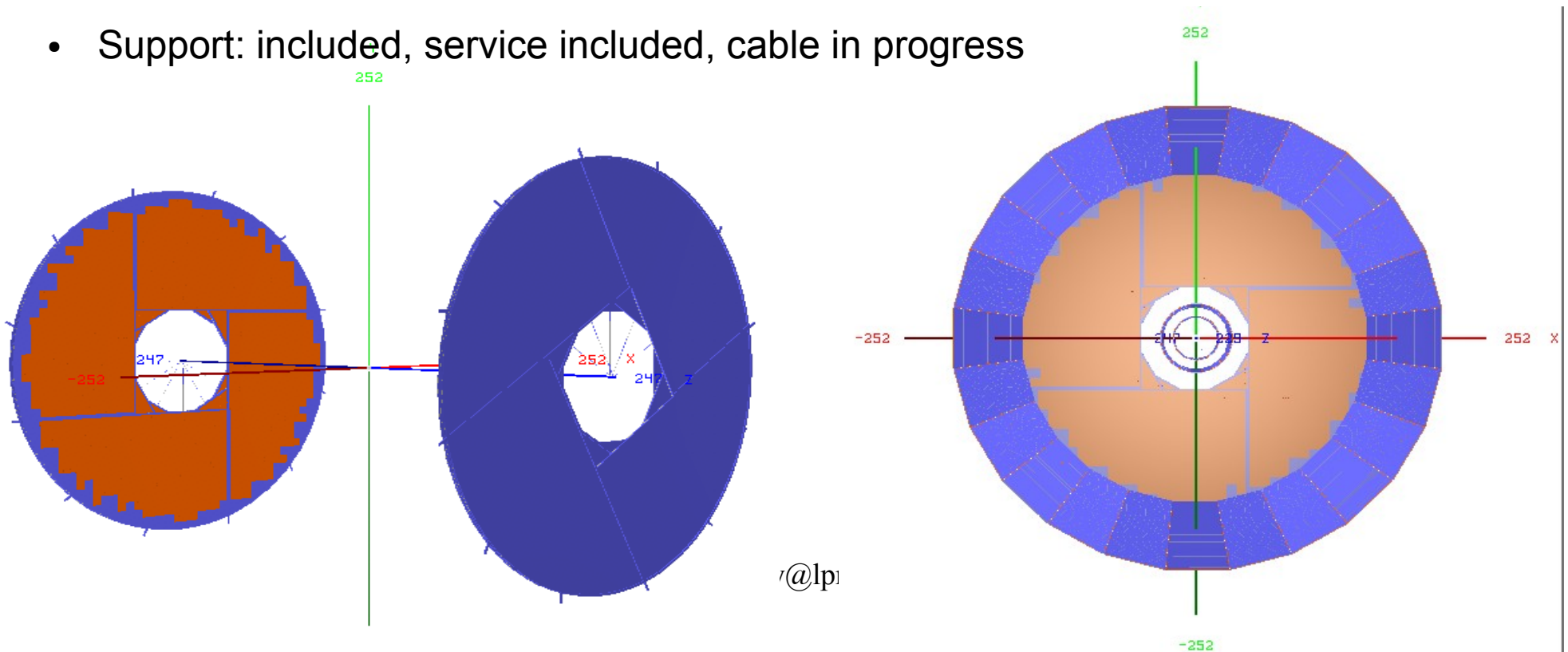


Silicon Tracking System

ETD

- Description:

- Using the edgeless properties
- XUV solution: pixels at small angle have to be implemented (XY alternative solution is available)
- Gaps: 50 micron gap between modules, super module, Gap between detection Element
- Support: included, service included, cable in progress



Silicon Tracking System

Overlapping

Overlapping in the Silicon tracking components:

- checked through Root within 100 μm
- according the status of the development

→ SIT : ok

→ SET : ok

→ ETD : detected during the support assembly – identify and patch in progress

Overlapping with other detectors:

- SET/TPC → need to be discussed when the support structure will be validated (possible re-scaling)
- SIT/FTD → need to discuss with Paulo and Jordi

Time Table and Manpower

What is done:

- The design pattern is frozen
- The module distribution is done → gap and basic support included

Tasks priority:

- complete the integration in Mokka and the ILD concept → sub-detectors dependancy (end of today)
- write the GEAR part according the interface provide by A. Munich and depending the reconstruction request (S. Aplin)
- Test TRKSISD00 class
- test the overlapping
- complete support and cabling description of the SIT/SET
- Complete the cabling for the XUV
- Complete the XY configuration
- write the documentation (to compete the doxygen one)

Manpower:

Alexandre Charpy (do what I can)
(Konstantin Androsov PhD ?)

Who is interested ?

Thanks for you attention ...