GRPC SDHCAL REVIEW: ASIC + DIF

IPNL Lyon, LAPP Annecy, OMEGA/LAL Orsay

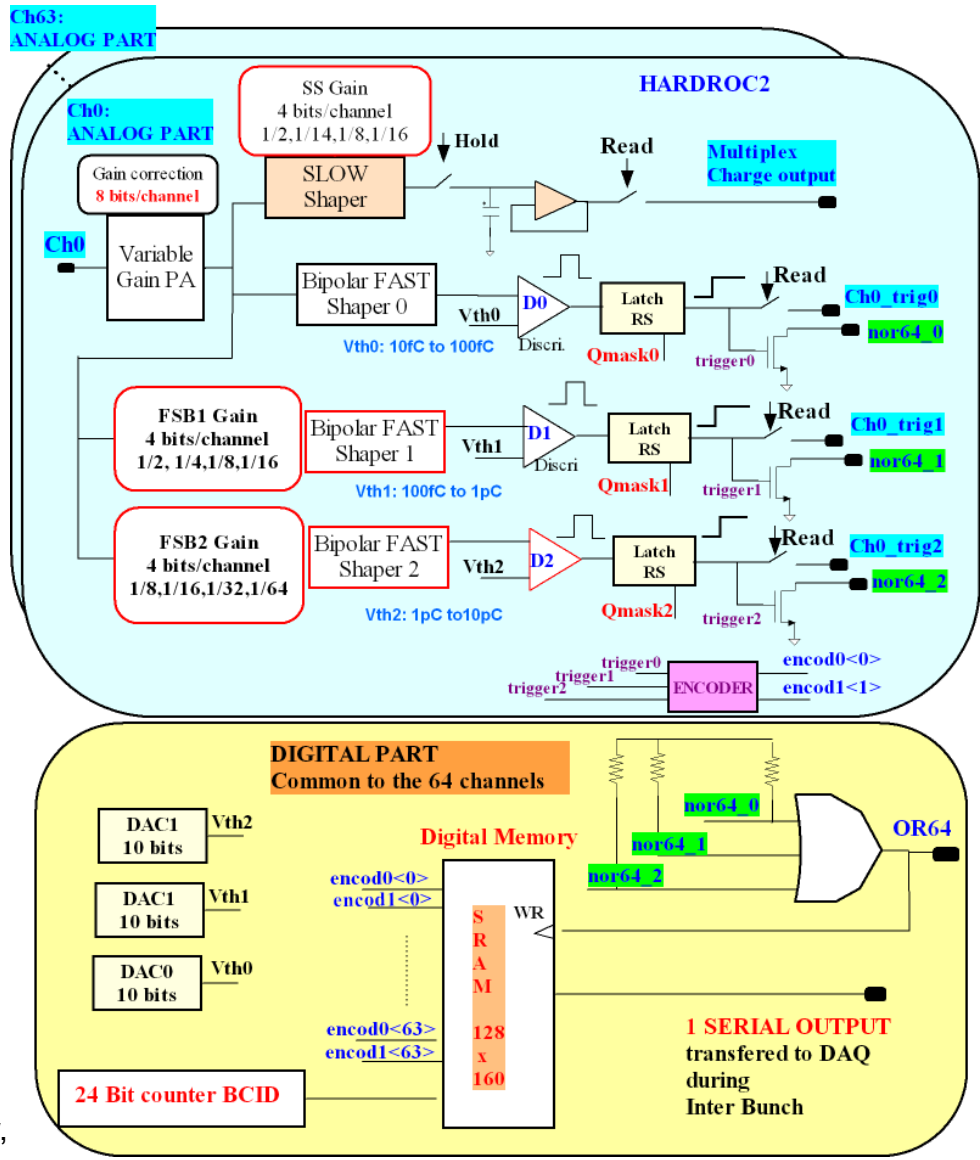
OUTLINE

- Very Front End ASIC
- PRODUCTION TESTS
- Detector InterFace board (DIF)

HARDROC2

http://omega.in2p3.fr/

- **64 inputs**
- Current preamp with **8 bits** gain correct: G=0 to 255 (analog G=0 to 2)
- **3 shapers**, variable Rf,Cf and gains:
  - Fsb1, G= ½,**1/4**,1/8,1/16
  - Fsb2, G= 1/8,**1/16**,1/32,1/64
- **3 discriminators**
  - 3 10 bit-DACs to set the thresholds (100fC, 1pC, 10pC)
  - Encoded in 2 bits
- **Auto-trigger down to 10fC up to10pC**
- Store all channels and BCID for every hit in a **127 bit deep digital memory**
  - Data format : 127 (depth)*[2bit*64ch+24bit(BCID)
  - +8bit(Header)] = 20 320 bits
- **872 SC registers**, default config
  - Mask of bad channels
- **Full power pulsing: < 10µW/ch**

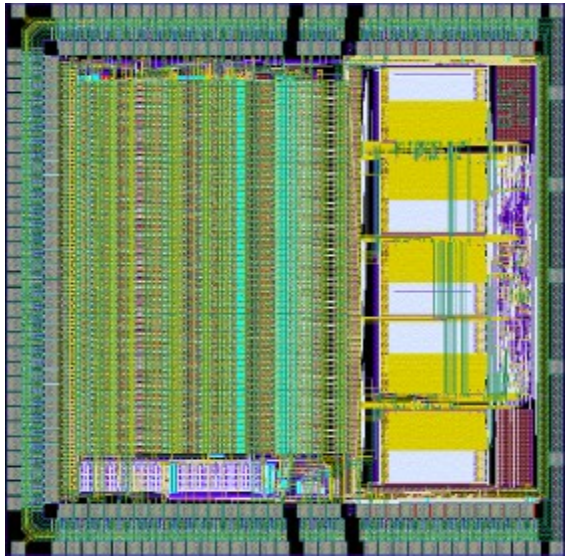


ASIC : HARDROC versions

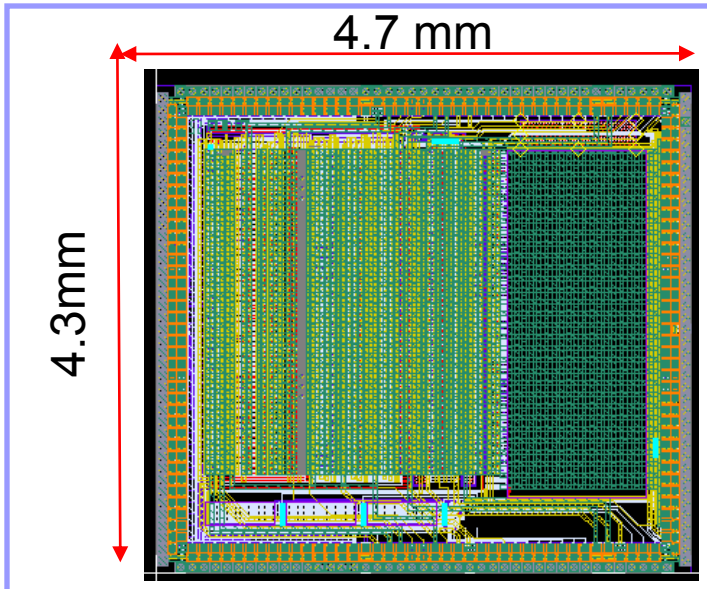
- **AMS 0.35µm SiGe**

- **HARDROC1** (Sept 2006):
  - **1 FSB and 2 discriminators**
  - **240 staggered pads, QFP240 package 3.4 mm thickness**

- **HARDROC2 (June 2008) and 2B (June 2009):**
  - **Versions 2 and 2B very similar, 3 FSB, 3 discris**
  - **160 aligned pads, Thin package TQFP160 = 28 mm x 28 mm x 1.4 mm**



HARDROC1,
240 staggered pads

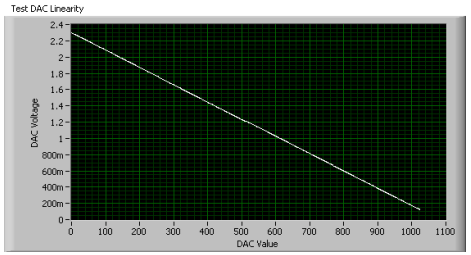


HARDROC2 and 2B
160 pads

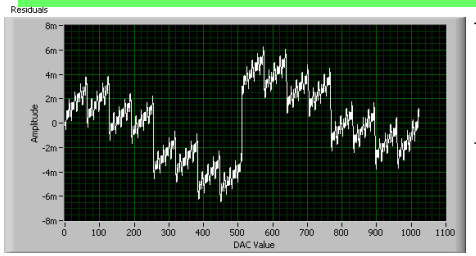
HR2 Trigger path : fast shaper, DAC, Xtk

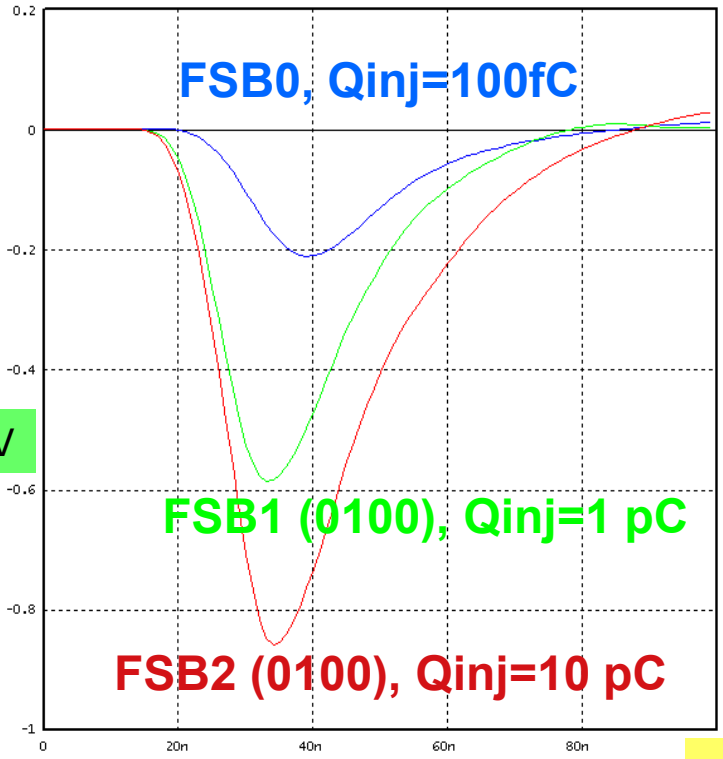
- Fsb0: **Typically 2mV/fC** (variable by a factor 10)
- 3 integrated DACs to deliver threshold voltages
  - Residuals within ±5 mV / 2.2V dynamic range. INL= 0.2% (2LSB)
- **2.1 mV/DAC Unit ie 1 fC/DAC Unit (fsb0)**

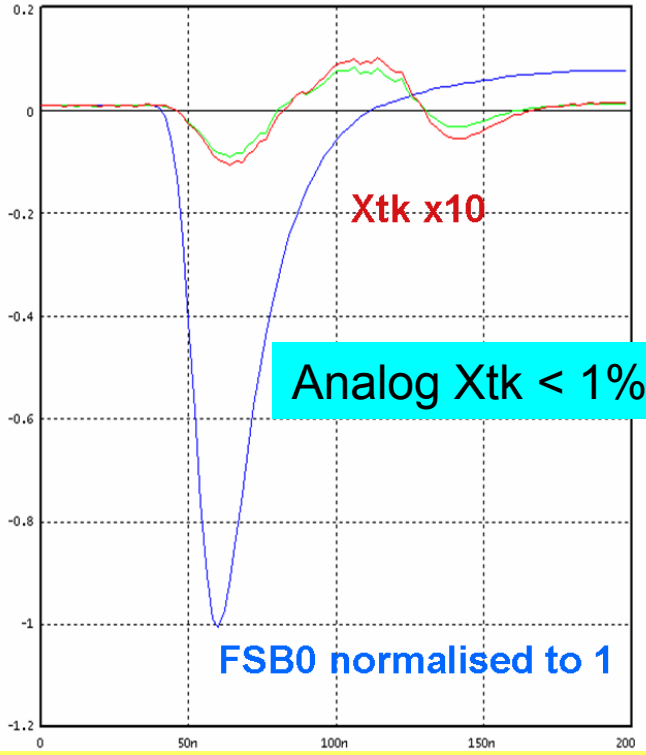
2.1mV/DAC Unit



Residuals within ±5 mV



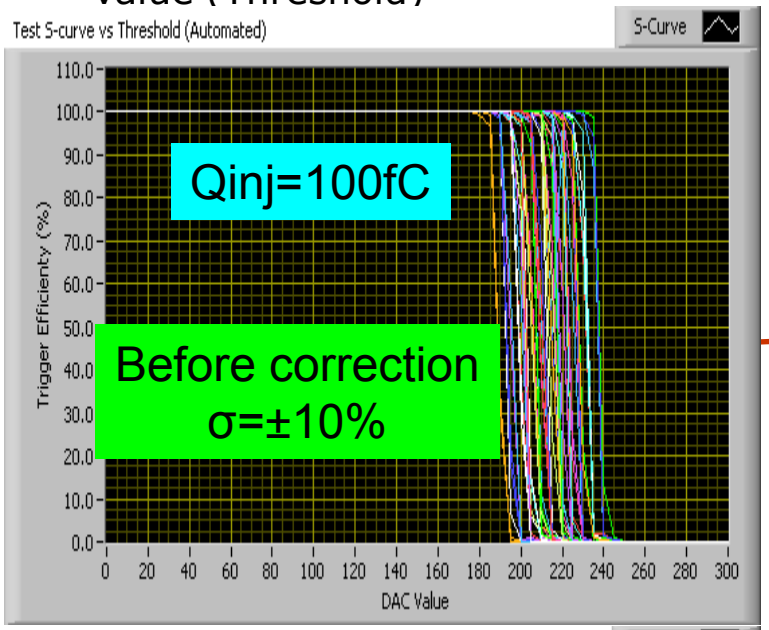


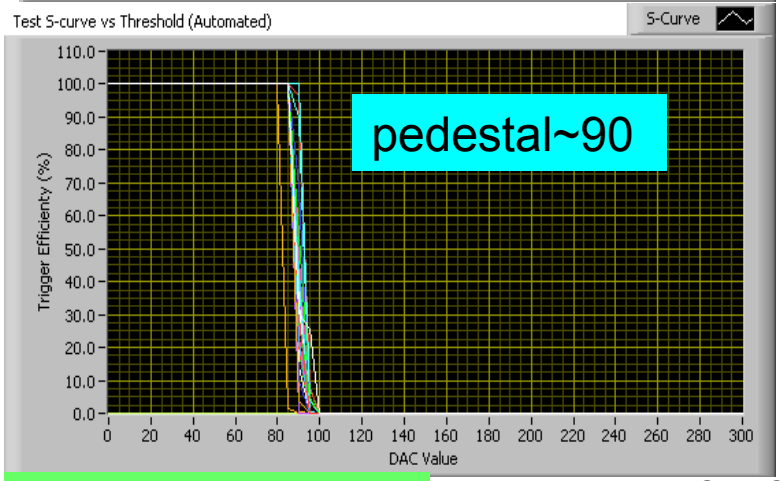


Testboard wo any decoupling cap.

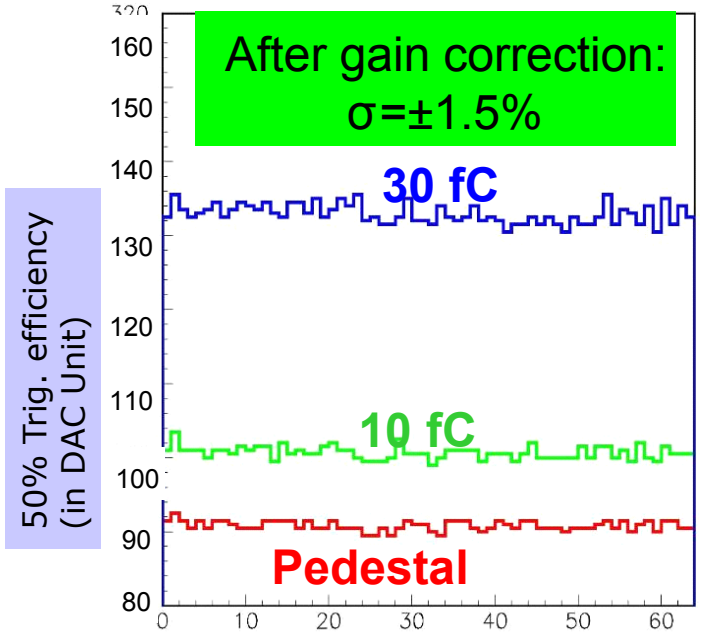
Trigger efficiency measurements

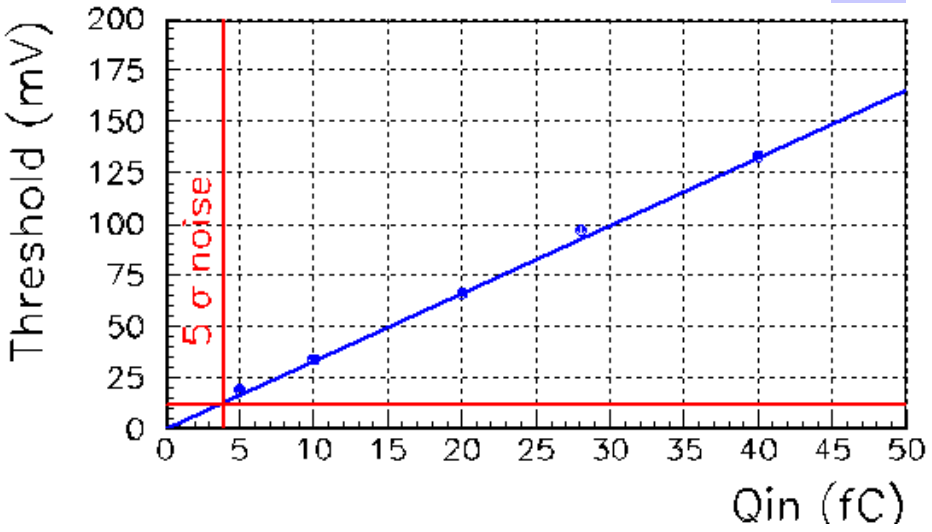
- Scurves performed on FSB0 by varying the DAC value (Threshold)



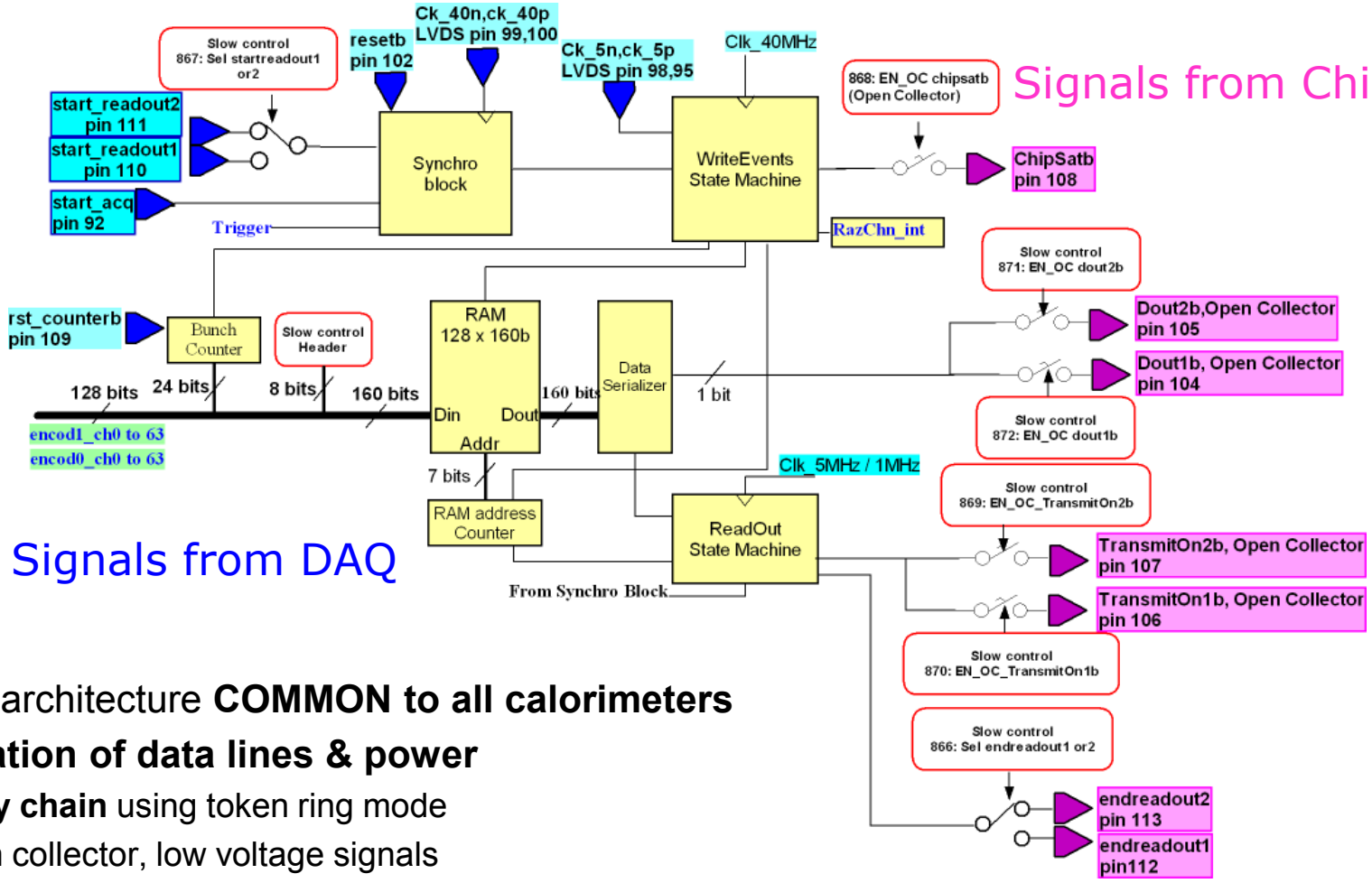


FSB0, 100K, 100fF, G=144





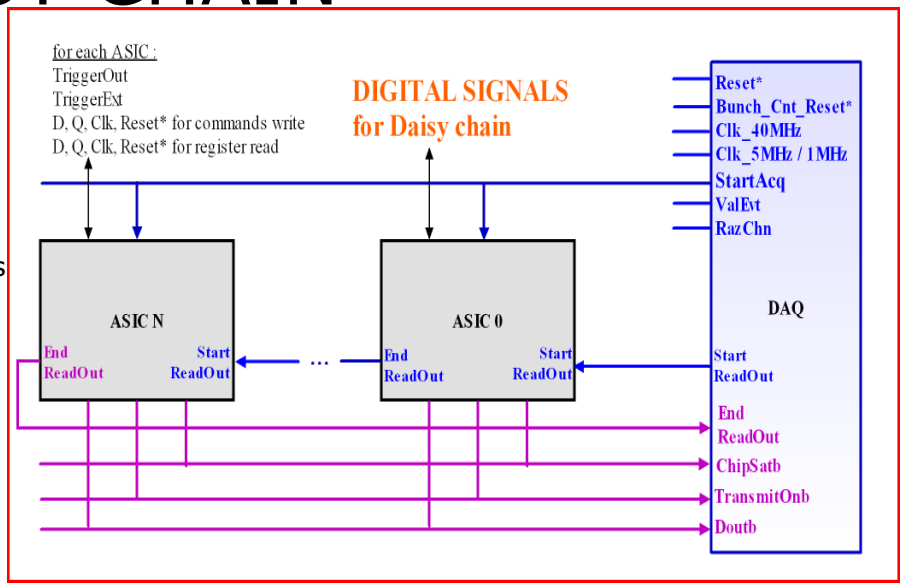
Digital part for DAISY CHAIN readout

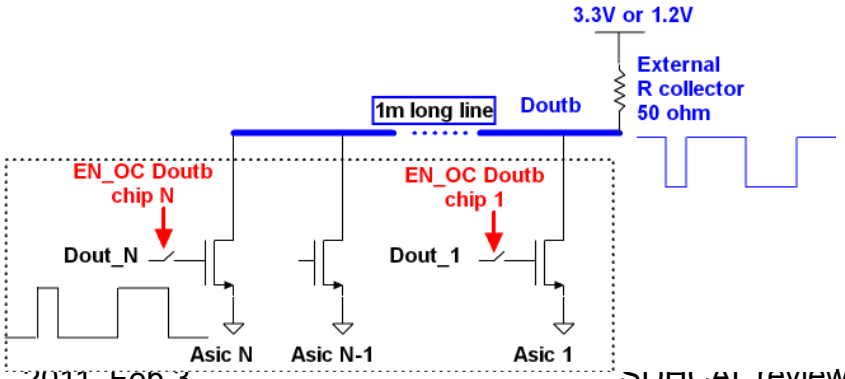


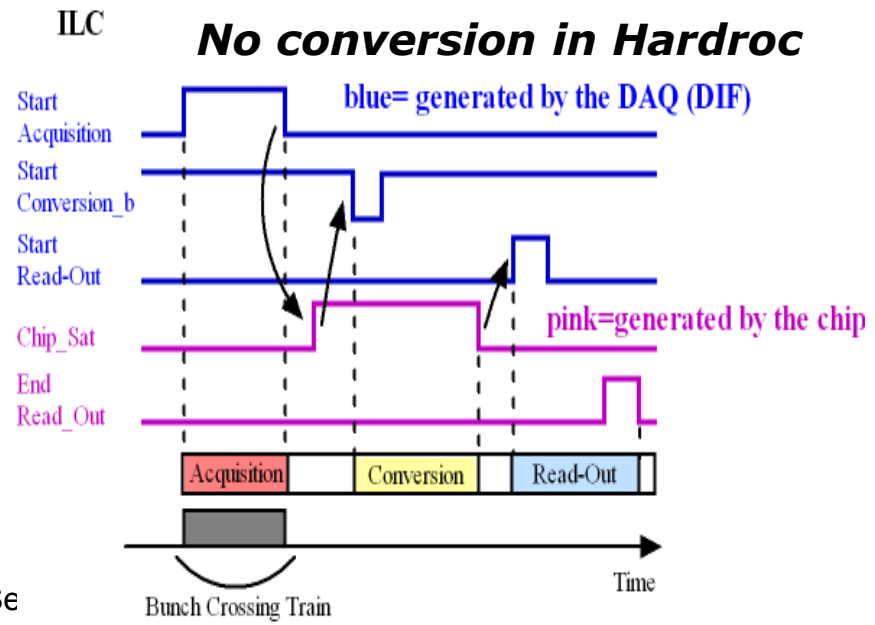
- Readout architecture **COMMON to all calorimeters**
- **Minimization of data lines & power**
  - **Daisy chain** using token ring mode
  - Open collector, low voltage signals
  - Low capacitance lines

Main signals of the DAISY CHAIN

- **COMMON to all the ROC chips**
  - **StartAcq**
    - Start acquisition, generated by DAQ
  - **ChipSat** (**O**pen **C**ollector signal):
    - Generated by chip, « 1 »: digital memory is full or acq is finished
  - **StartReadout:**
    - Generated by DAQ, start of the readout
  - **EndReadout**
    - Generated by chip, End of the readout
  - **Dout:** data out (OC signal)
  - **TransmitOn** (OC signal)
    - Generated by chip, Data out are transmitted
- Buffers integrated for OC signals

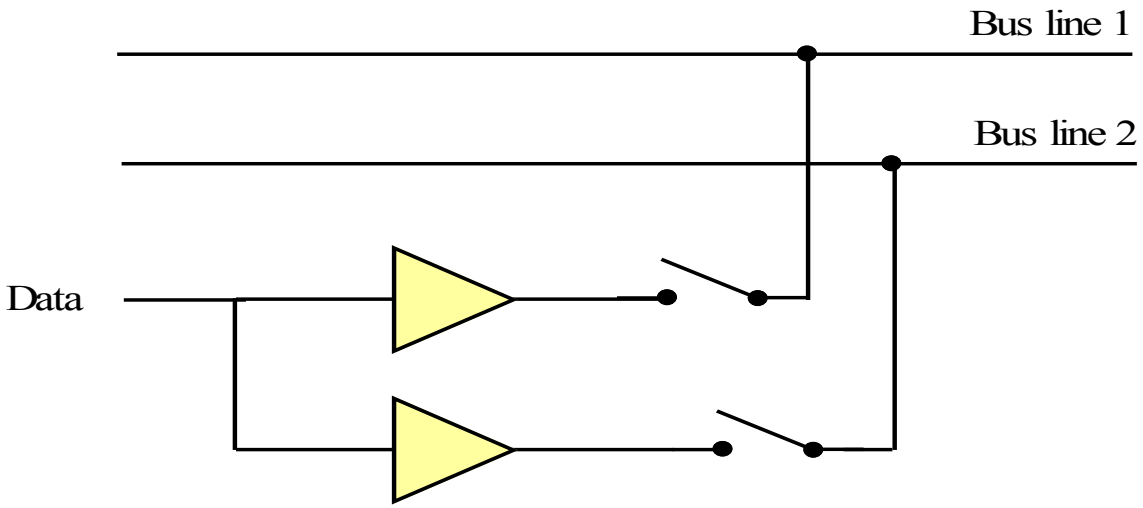






Redundancy and bypass of the OC lines: Doutb and TransmitON

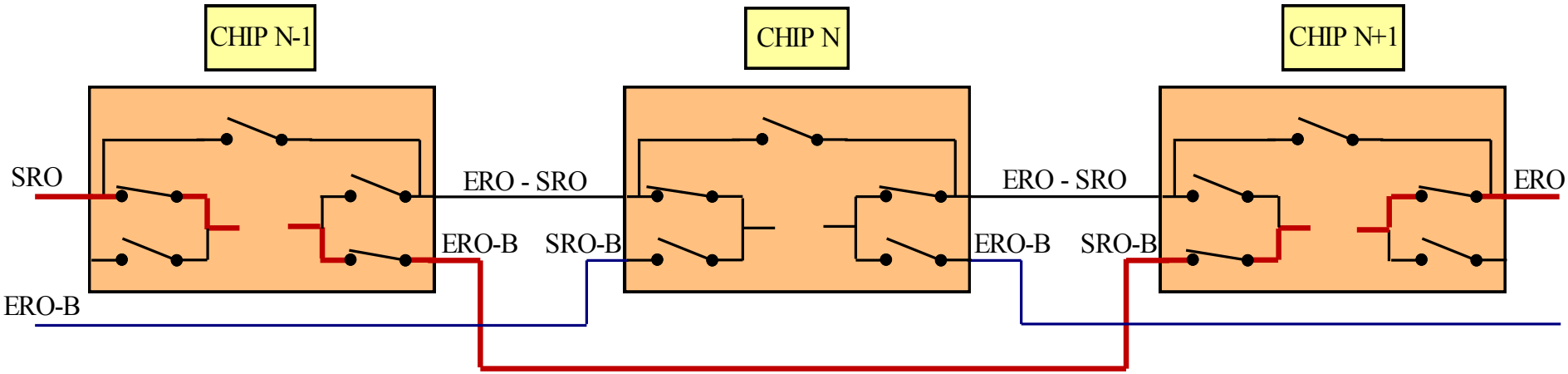
- 2 data line/chip (Dout1b and Dout2b), chosen via SC
- 2 TransmitOn lines /chip
- Each one is removable from bus line by SC



- Allow to remove buffers which stick the bus line

Redundancy and bypass: StartReadOut and EndReadOut

- Bypass : SRO, ERO ➔ SRO-B, ERO-B

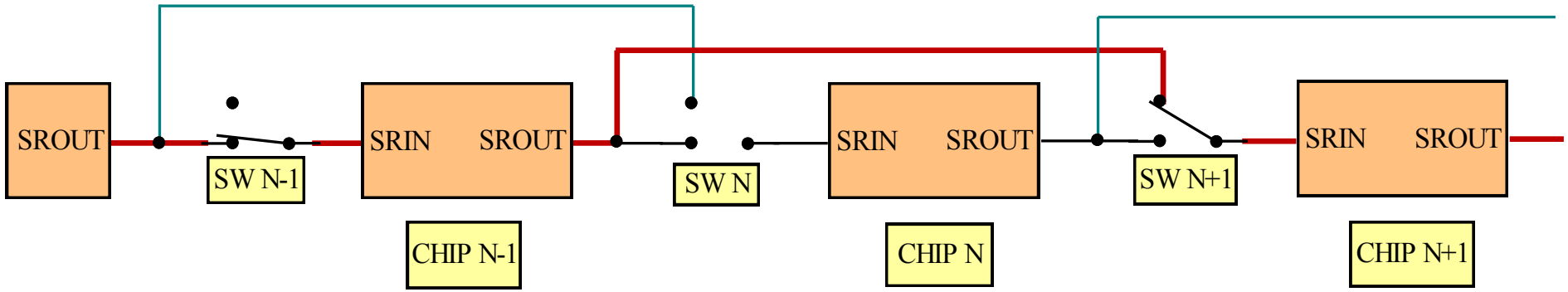


In red, StartReadOut and EndReadOut flow if chip "N" fails

- Chip N can be bypassed using SC parameters
- Chip "N-1" and chip "N+1" can bypass chip "N" by SC
- If Chip N fails :
  - Chip N-1 sends EndReadOut signal on EndReadOutBypass
  - Chip N+1 reads StartReadOut signal on StartReadOutBypass

Slow Control: bypass

- Bypass jumpers on PCB

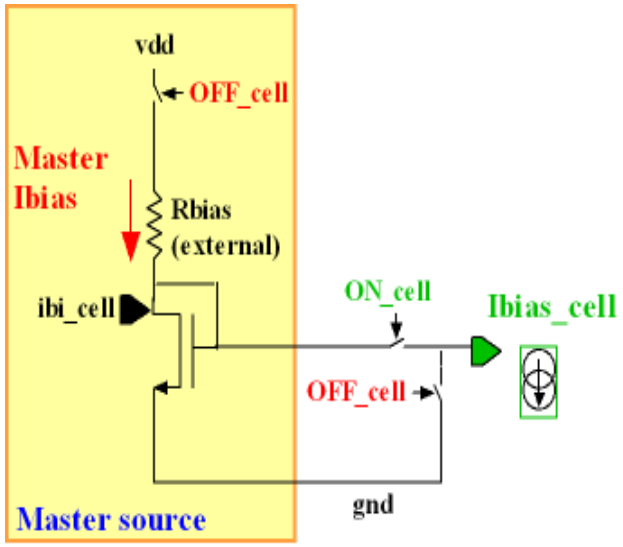


In red, SC flow if chip "N" fails

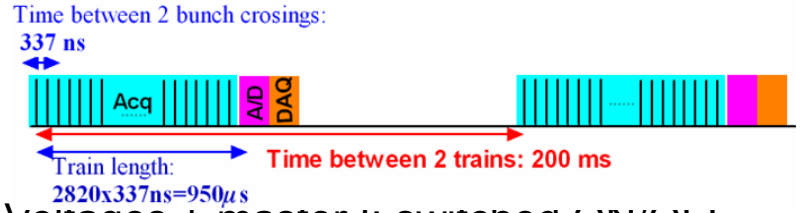
- Default position is chip "N" reads chip "N-1"
- If Chip N fails :
  - Switch N removed
  - Switch N+1 ➔ in position to read chip "N-1"

- 3rd generation of ROC chips: I2C link

POWER PULSING



- **Requirement:**
  - **10 µW/ch with 0.5% duty cycle**
  - **200 µA for the entire chip**



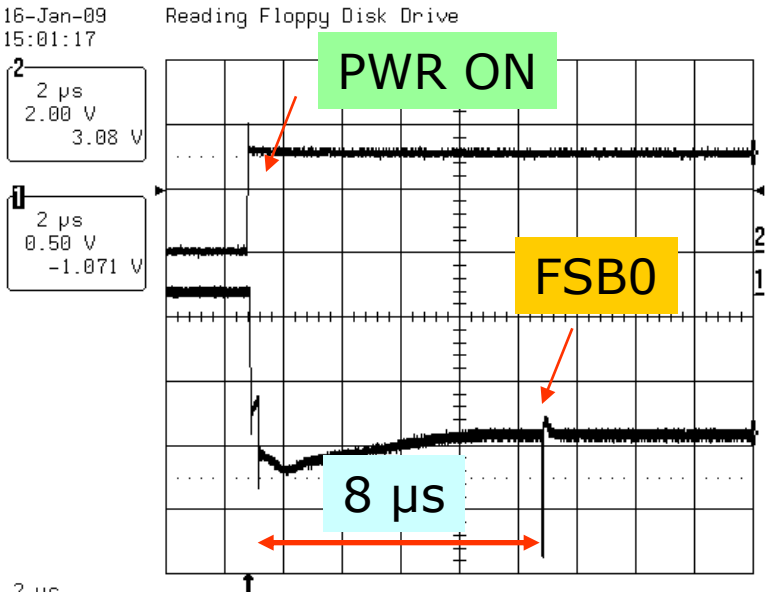
- **Power pulsing:**
  - Bandgap + ref voltages + master I: switched ON/OFF
  - **Shut down bias currents with vdd always ON**

- **HR2 power consumption measurement:**
  - 29 mA x 3.3V ≈ 100 mW => **1.5 mW/ch**
  - **7.5 µW/ch with 0.5% duty cycle**

Preamp	5.46 mA	DAC	0.84 mA
3 FSB	12.3 mA	BG	1.2 mA
3 Discris	7.3 mA	vddd 2	0.4 mA (=0 if 40MHz OFF)
TOTAL	29 mA		

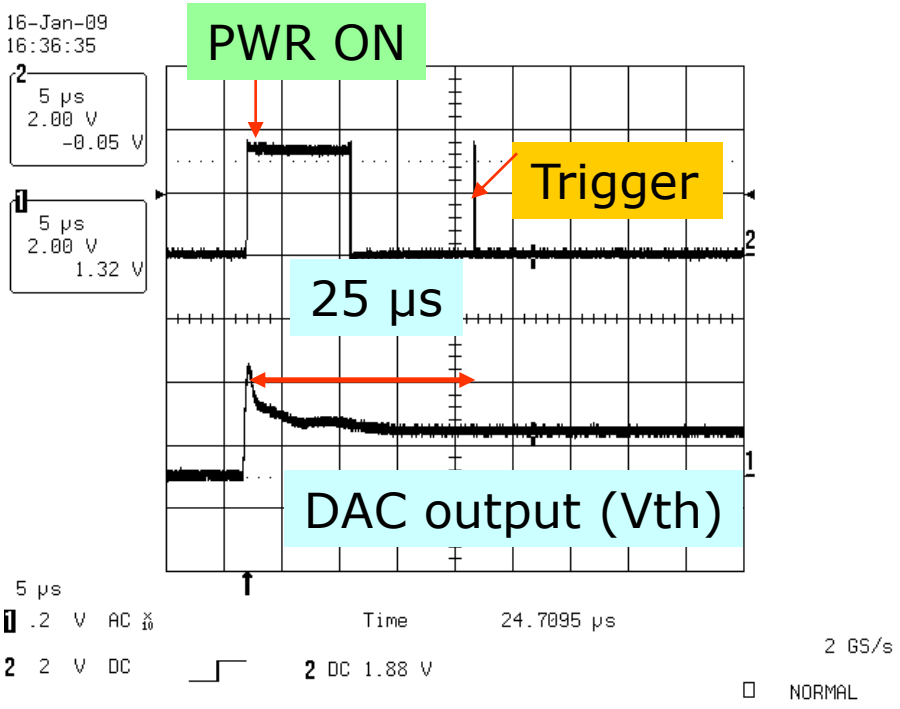
- **4 Power pulsing lines** : analog, (conversion), dac, digital
- Each chip can be forced **on/off by slow control**

POWER PULSING: « Awake » time



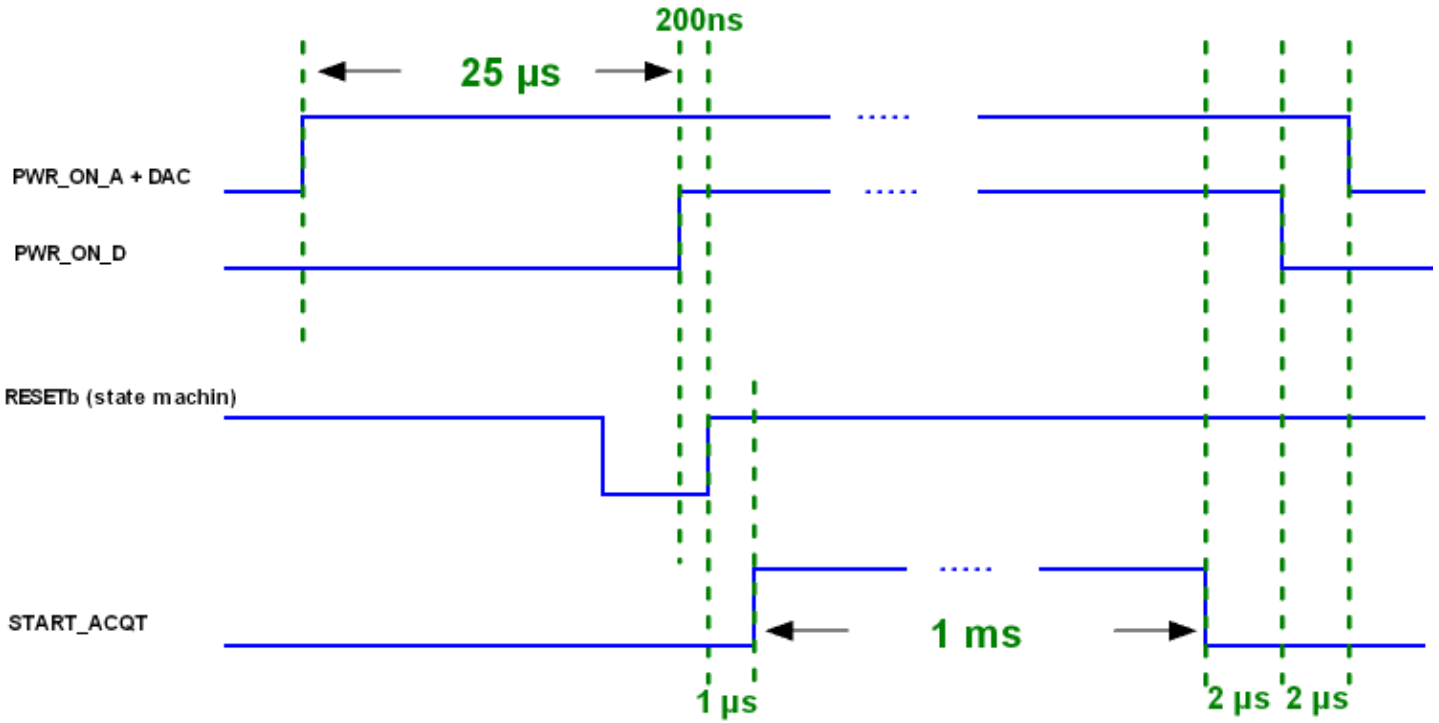
- All decoupling capacitors removed
- PWR ON: ILC like (1ms,199ms)
- PP of the analog part:
  - Input signal synchronised on PWR ON
  - Awake time= 8 µs

- **Power pulsing of the DAC:**
  - **25 µs (slew rate limited)**

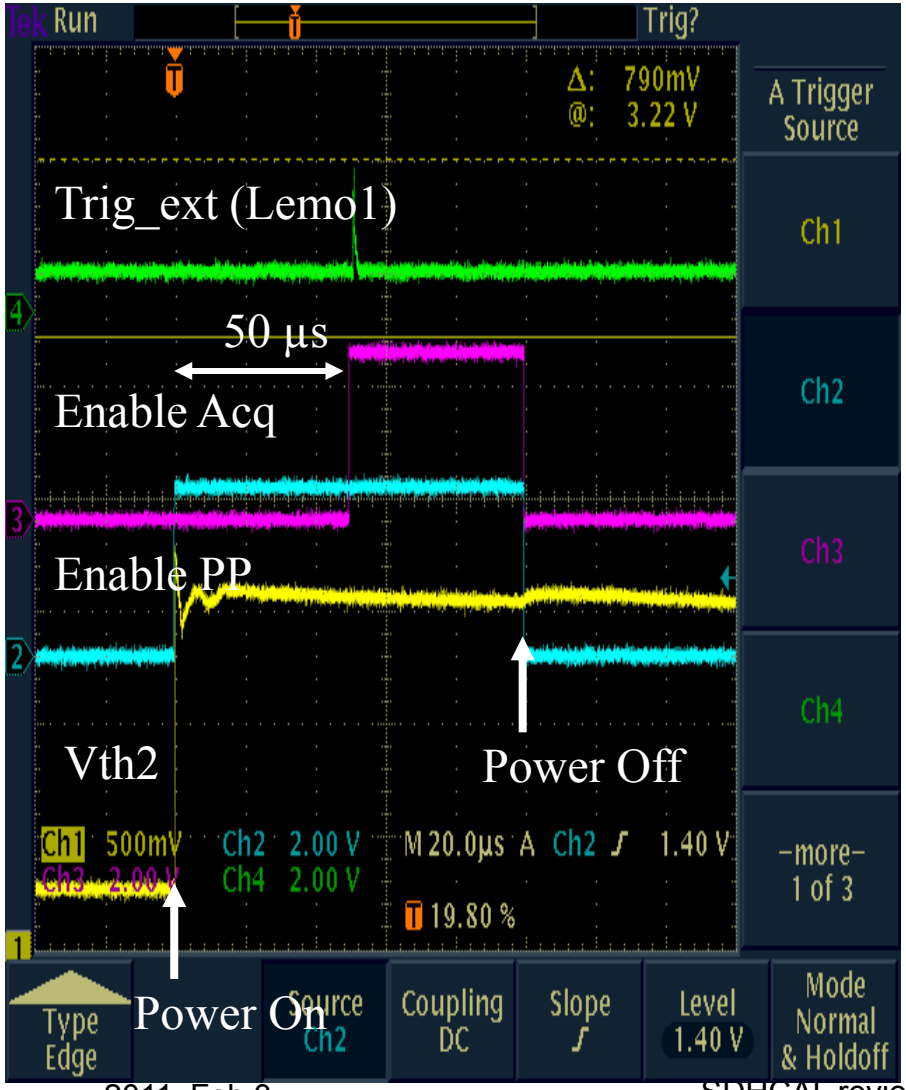


Power pulsing sequence

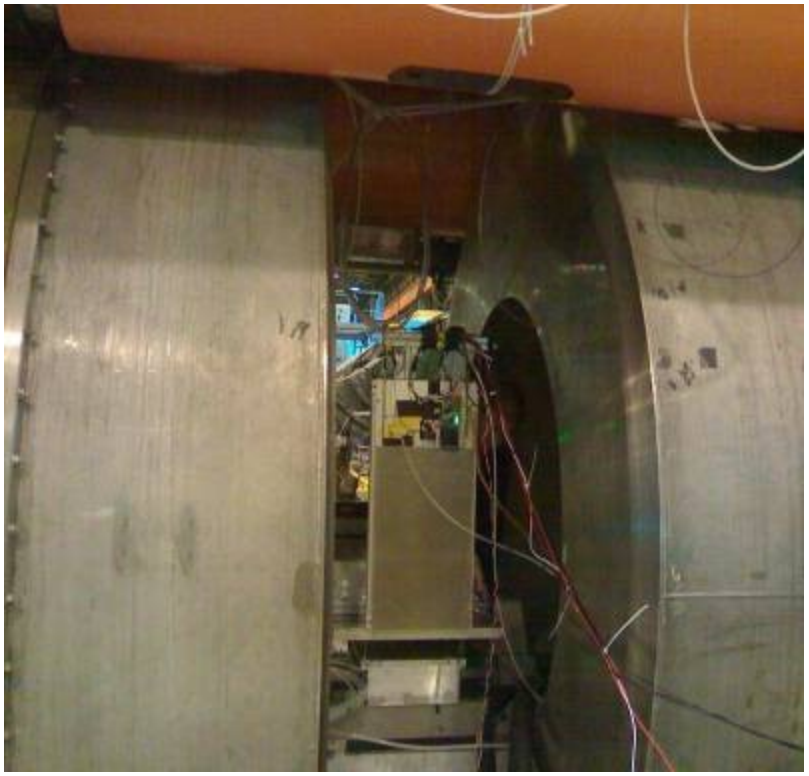
- 4 Power pulsing lines : analog, conversion, dac, digital
- Each chip can be forced on/off by slow control
- Timings detailed in Eudet-Memo-2010-05, Frédéric Dulucq, http://www.eudet.org/e26/e28/



Readout Electronics in TESTBEAM: Power-Pulsing

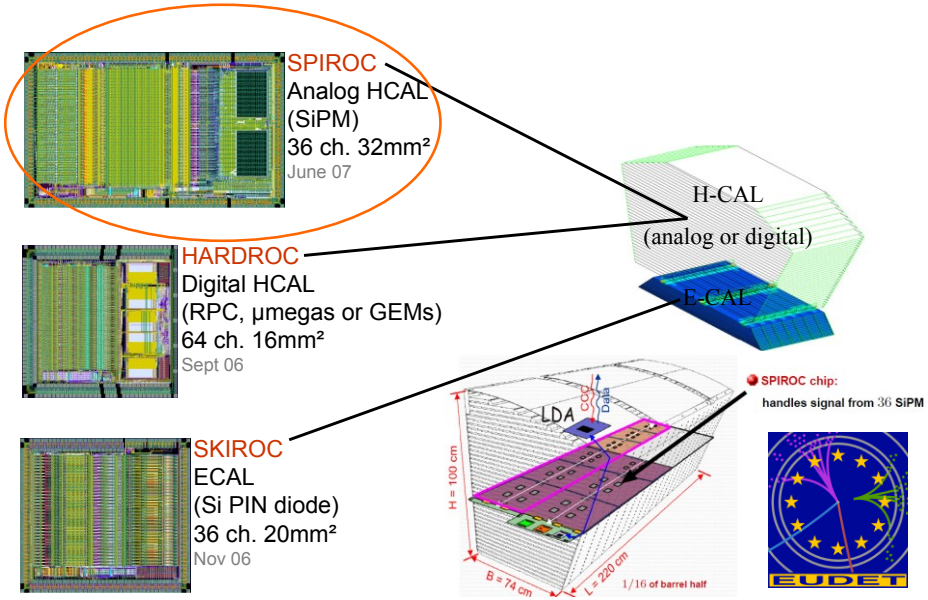


Power pulsing was successfully tested on a 24-ASIC electronic board. The board associated to a GRPC was also successfully tested in a 3-Tesla B field in June (SPS-H2)



Production run

- **Production run launched in March 10**
- **Reticle size : 18x25 mm²**
  - 50-55 reticles/Wafer
  - 25 wafers needed
- **Final arrangement:**
  - **« Calice » chips produced:**
    - **7 Hardroc 2b** => ~9000 chips
    - **1 Spiroc 2a** => ~1200 chips
    - **1 Spiroc 2b** => ~1200 chips
    - **1 Skiroc 2** => ~1200 chips
  - **Additionnal chips produced:**
    - 1 Spaciroc : JEM EUSO experiement
    - 1 Maroc 3 : for PMT readout
    - 3 Spiroc 0 (SPIROC « light » version)
    - => **cost reduction** for CALICE



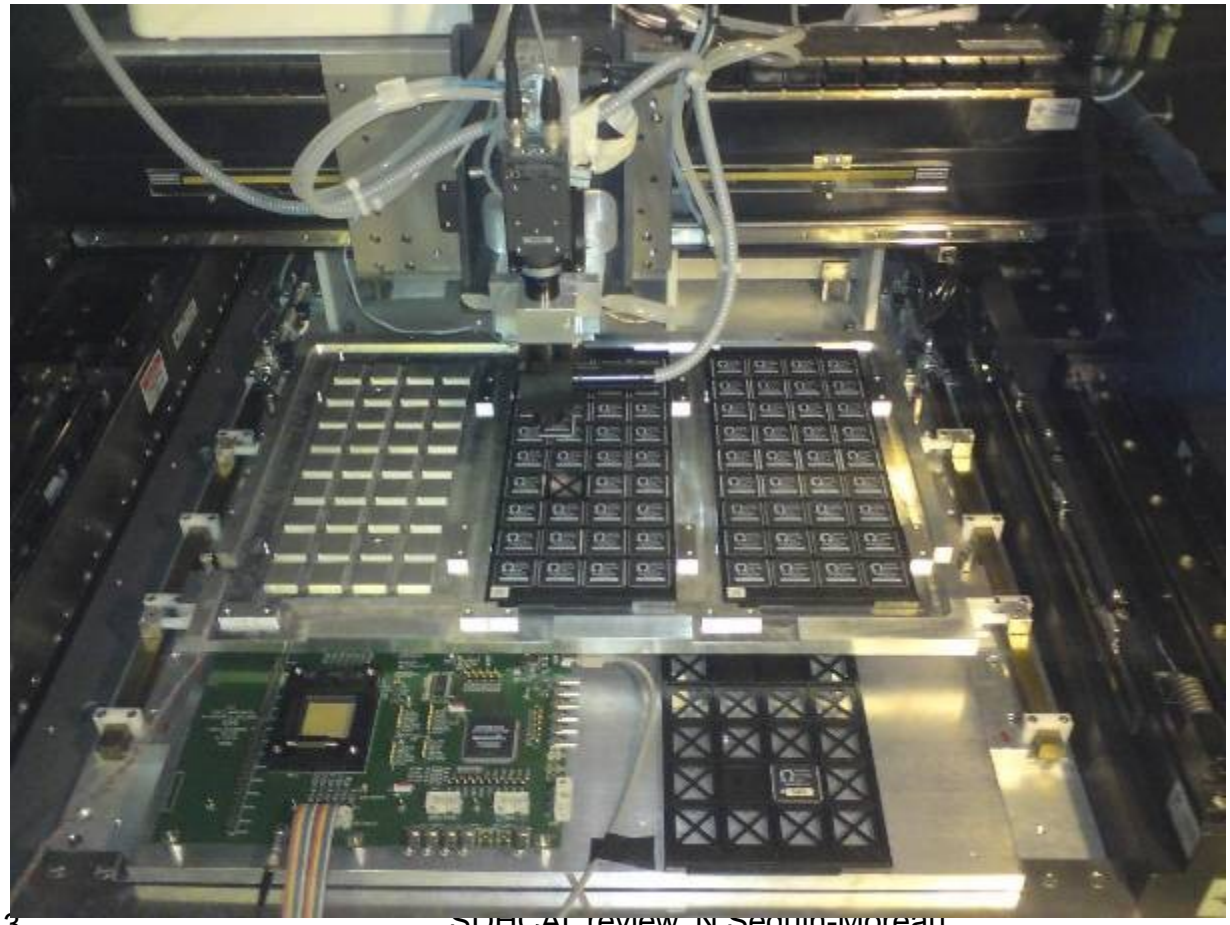
Packaging

- Wafers received from AMS at the end of June and sent directly to I2A Technology (Fremont, USA) for packaging
- Thinning of the wafers down to 250µm
- Dicing

- Packaged chips and bare dies received at the end of August
  - **HR2b: 10 510 packaged in TQFP160 + ~ 1 000 bare dies**
  - SPIROC2A: **973** in TQFP 208, **661** bare dies
  - SPIROC2B: **195** in TQFP208, **1 469** bare dies
  - SKIROC2: **1 671** bare dies

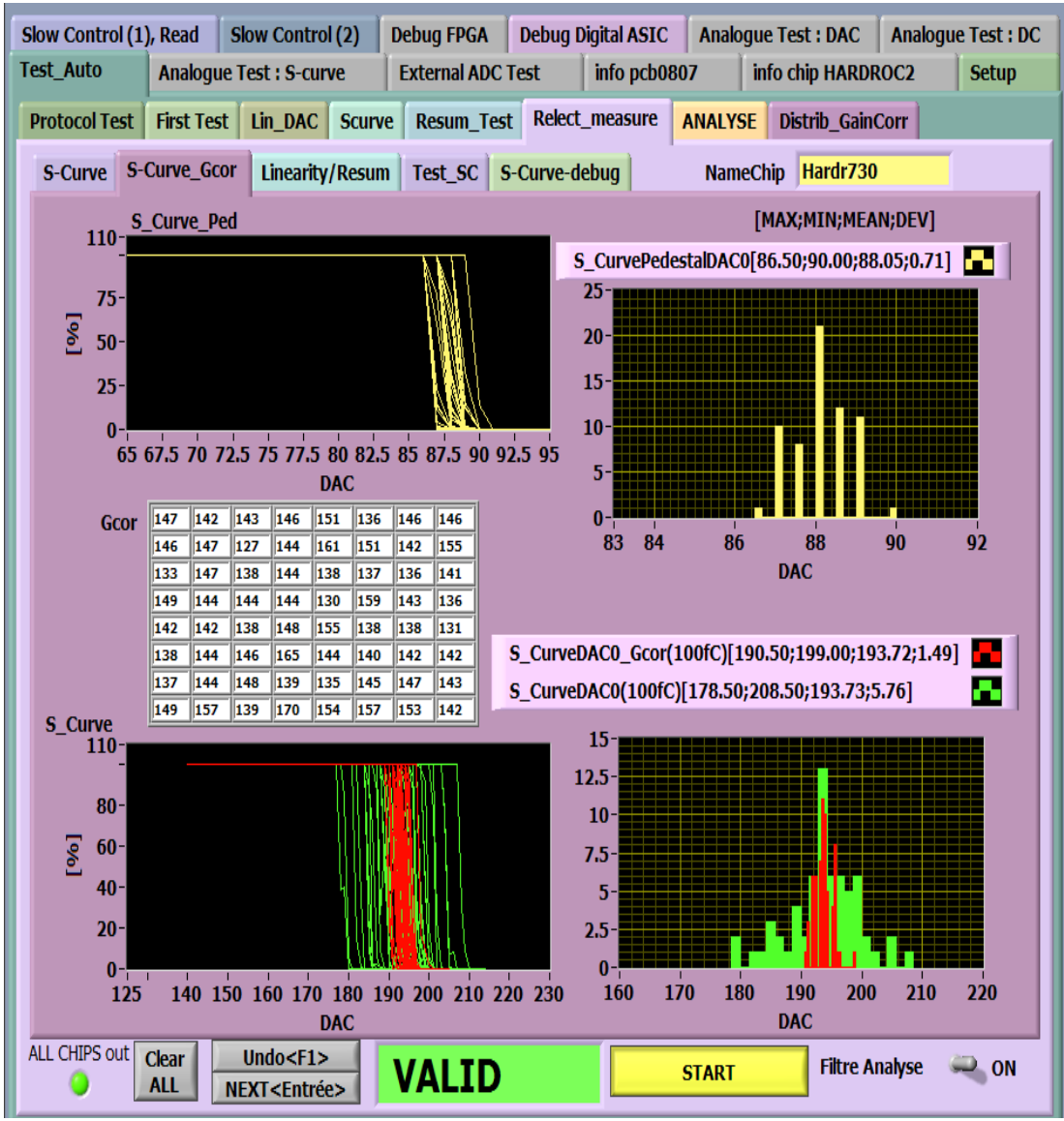
PRODUCTION TESTS

- ~10 000 chips to be tested with a dedicated testbench in IPNL Lyon
- Dedicated Labview program, USB interface, testboard, programmable generator (GPIB), precise multimeter (Keithley)



PRODUCTION TESTS

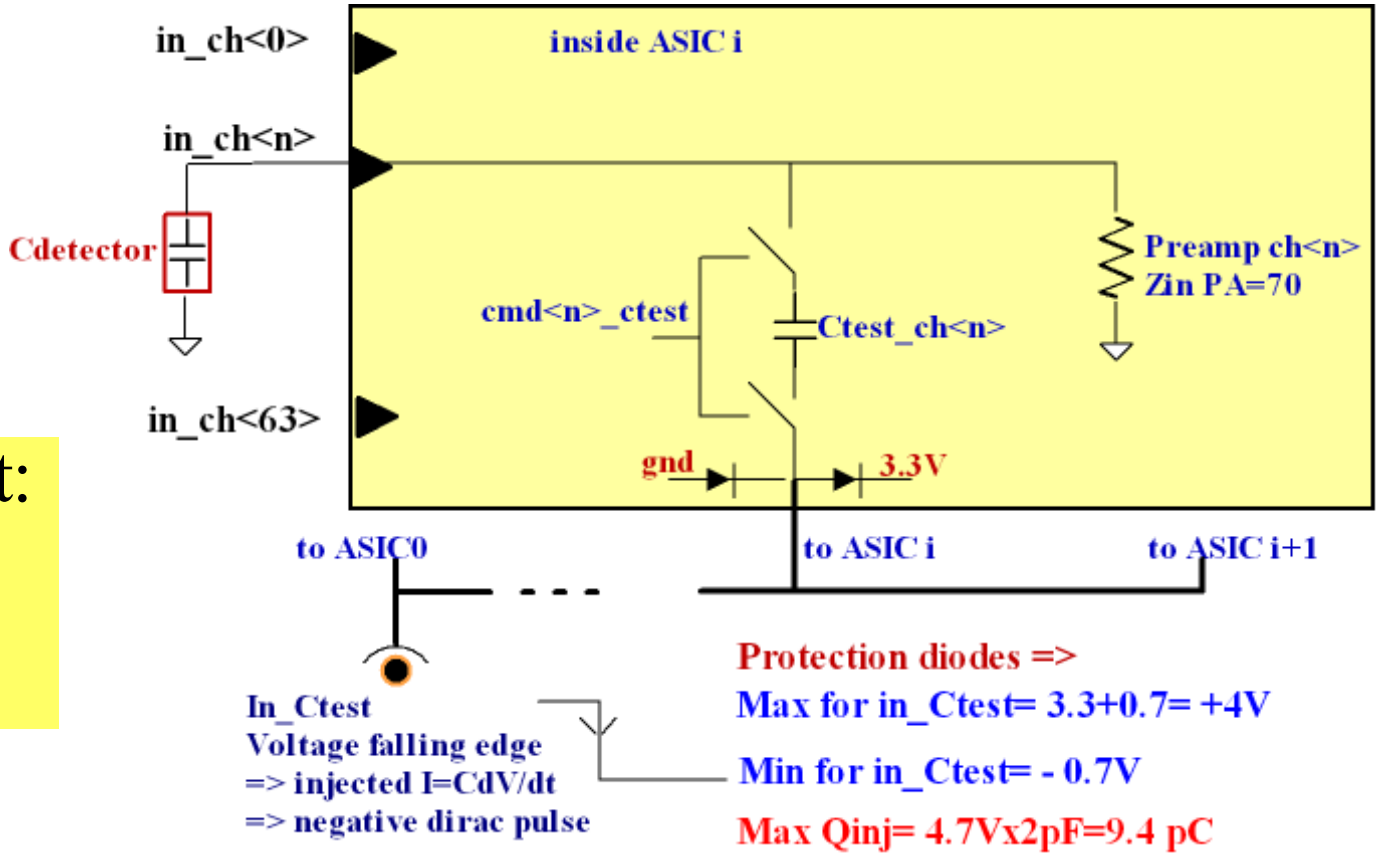
- Measurement of the DC levels and power consumption
- Test of the Slow Control loading
- Memory test
- DACs linearity
- Trigger efficiency measurement
  - Pedestal for the 3 shapers
  - 100 fC trigger efficiency measurement for fsb0 + gain correction for each channel
  - 1 pC trigger efficiency measurement for fsb1 and fsb2



CALIBRATION

- **RPC signal: dirac current**
  - Fsb0: for input charges from 10fC up 100fC
  - Fsb1: for Qinj from 100fC to 1pC
  - Fsb2: for Qinj from 1pC up to 10pC

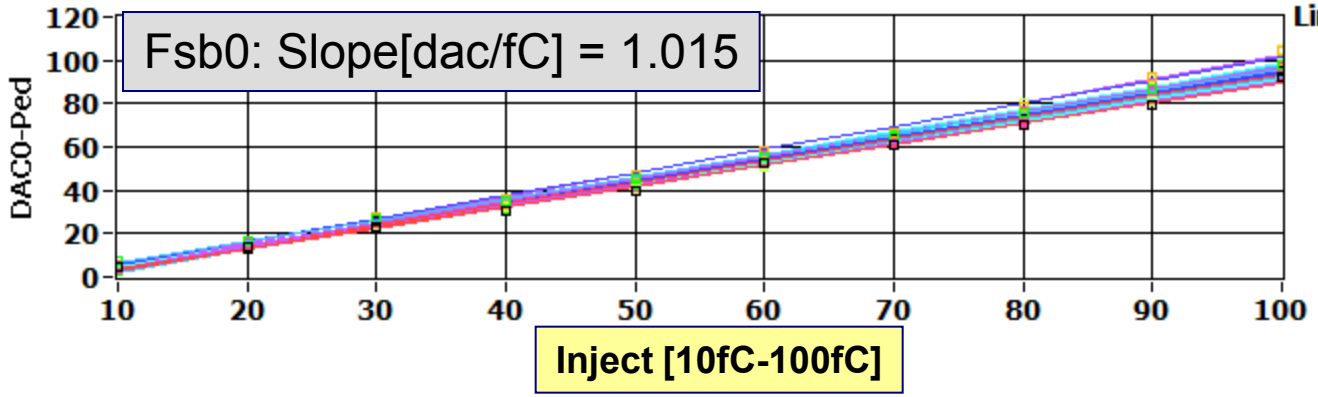
MAXIMUM Qinj through Ctest: about 9pC (protection diodes)



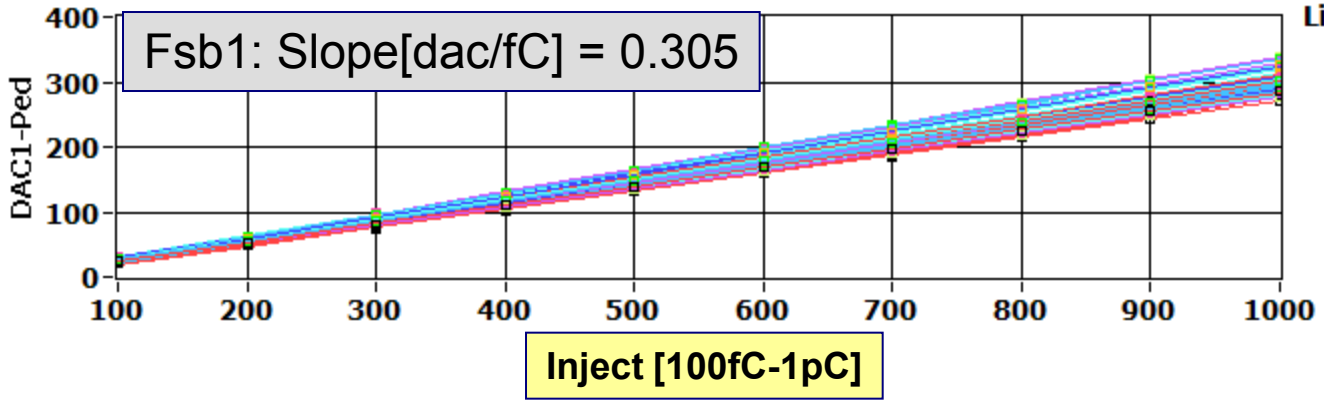
Dirac current:

$$i = C_{test}\frac{dV}{dt}$$

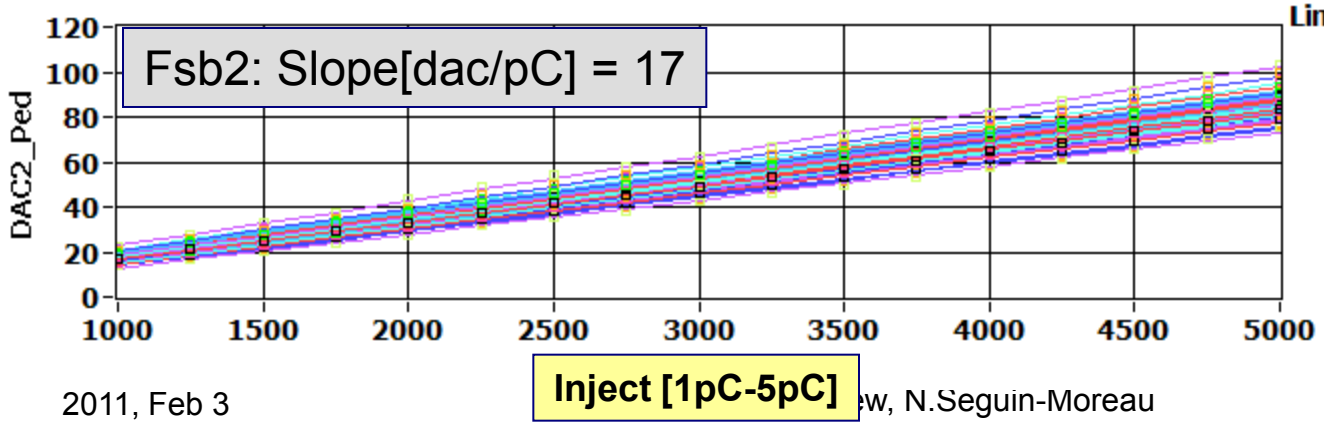
Fast Shaper Linearity: 64 channels



PARAM:
SS Gain : 1111
Sw_50k0:Off
Sw_100k0:On
Sw_100f0:On
Sw_50f0:Off
Measures 64 channels:
Dev : 0.022 [dac/fC]
Max: 1.082 [dac/fC]
Min : 0.961 [dac/fC]



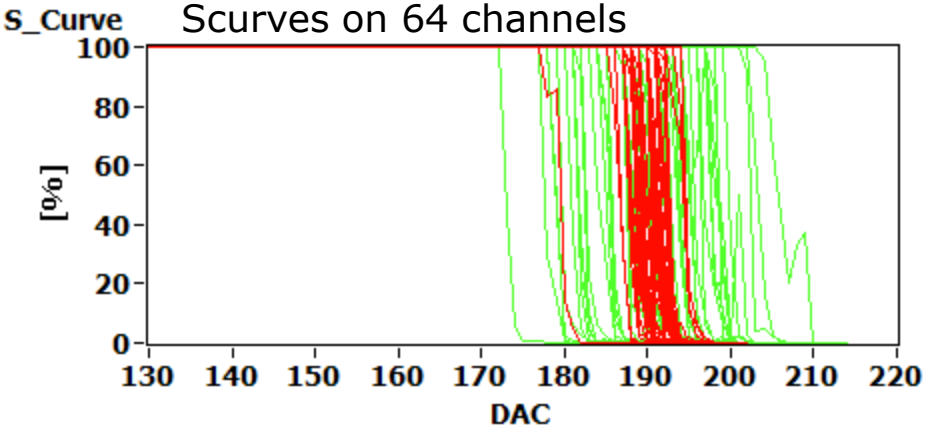
PARAM:
FSB1 Gain : 1000
Sw_50k1:On
Sw_100k1:On
Sw_100f1:On
Sw_50f1:On
Measures 64 channels:
Dev : 0.016 [dac/fC]
Max: 0.346 [dac/fC]
Min : 0.277 [dac/fC]

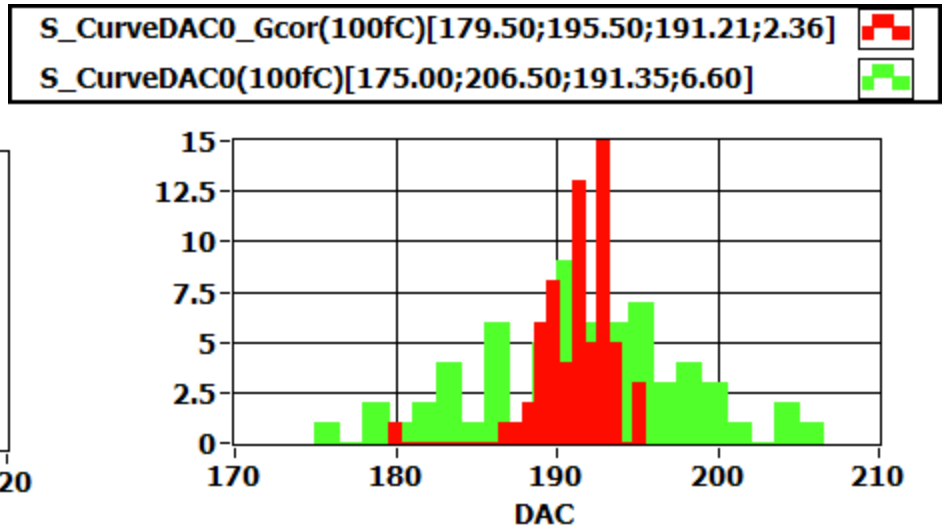


PARAM:
FSB2 Gain : 0010
Sw_50k1:On
Sw_100k1:On
Sw_100f1:On
Sw_50f1:On
Measures 64 channels:
Dev : 0.001 [dac/fC]
Max: 0.0198 [dac/fC]
Min : 0.0151 [dac/fC]

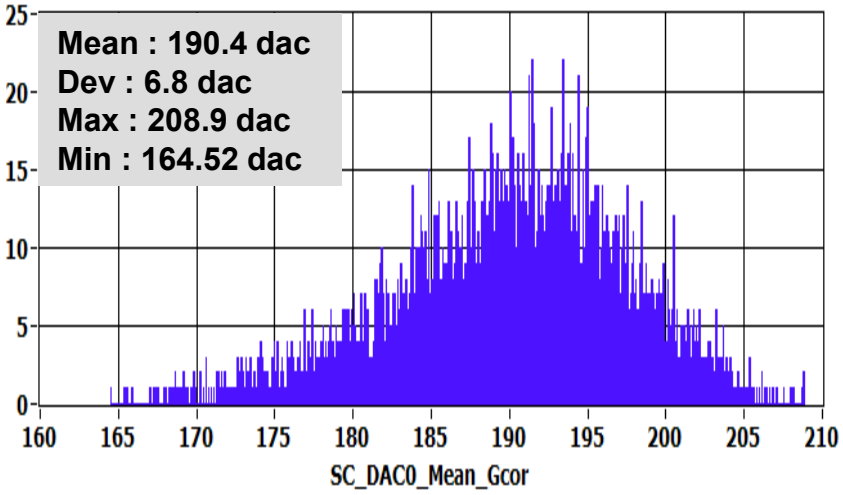
EXAMPLE FOR CHIP B10X3Y7

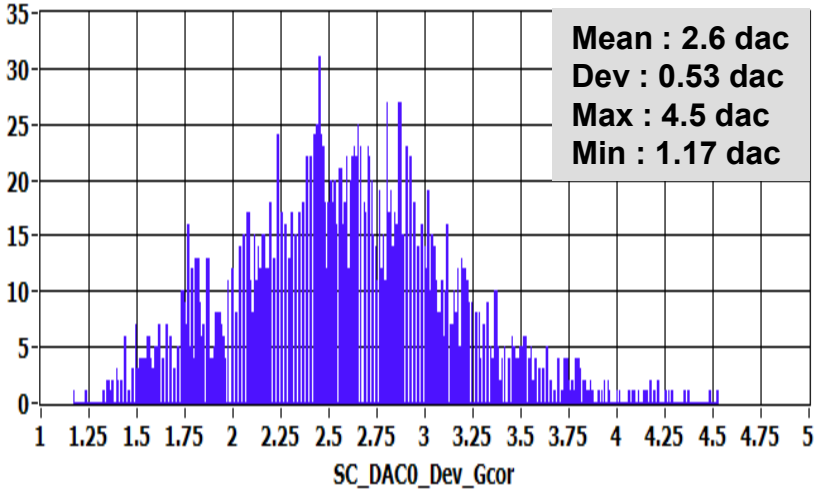
Fsb0, Qinj=100 fC
Scurves on 64 channels



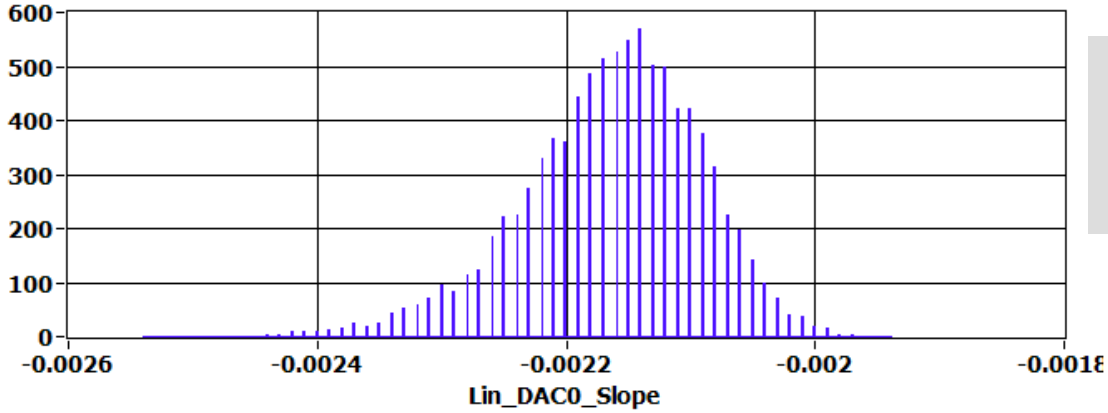


Statistics: 9500 H2B, 50% trigger efficiency point after gain correction

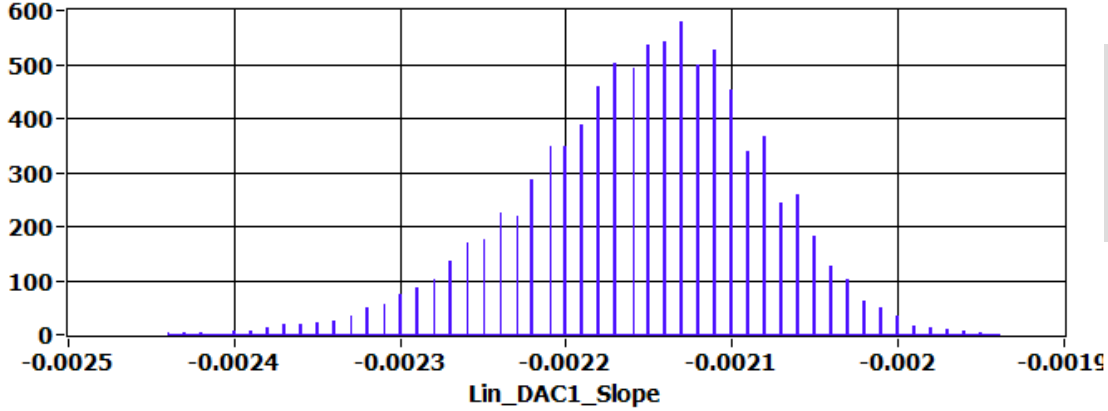




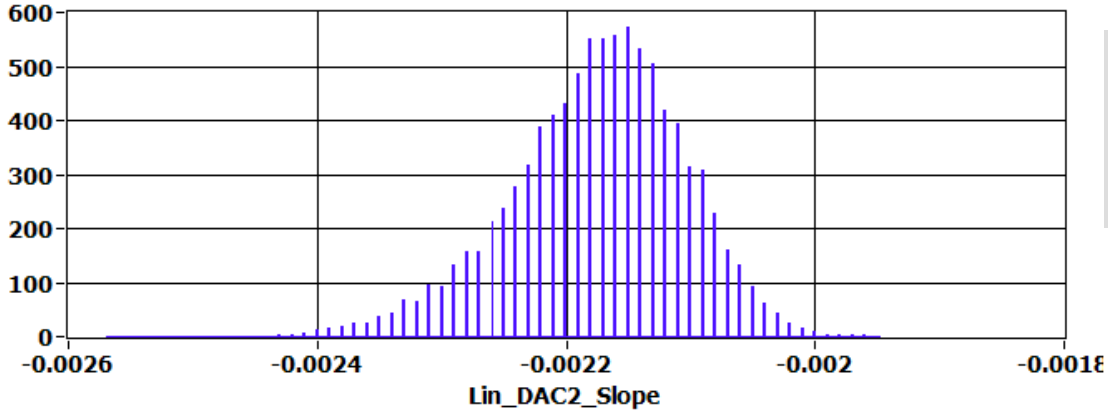
Statistics: 9500 chips, DAC Slope



Mean : -2.16 mV/DAC Unit
Dev : 0.7 mV
Max: -1.94 mV
Min : -2.54 mV



Mean : -2.15 mV/DAC Unit
Dev : 0.7 mV
Max: -1.94 mV
Min : -2.44 mV



Mean : -2.17 mV/ DAC Unit
Dev : 0.7 mV
Max: -1.95 mV
Min : -2.457 mV

TEST PROTOCOL

SEQUENCE OF TESTS	VALUE(Mean) : 9500 H2B	DEV
Conso Power ON (Vcc)	220 mA	2
Conso Init System (Vcc)	209.8 mA	1.1
Conso Power SC (Vcc)	228.8 mA	0.7
Conso before load SC	18.7 mA	0.2
Conso after load SC	37.9 mA	0.4
V_BG	2.486 V	0.02
DC_FSB0(Chan20)	2.141 V	0.02
DC_FSB1(Chan20)	2.148 V	0.02
DC_FSB2(Chan20)	2.148 V	0.02
Memory(DAC0:300):Inj Ctest All Chan	ALL Chan Trig0	
Memory(DAC1:200):Inj Ctest All Chan	ALL Chan Trig1	
Memory(DAC2:200):Inj Ctest All Chan	ALL Chan Trig2	
Linearity_DAC0 (1, 2, 4, 8, 16, 32, 64, 128, 256, 512)	Slope = -2.16 mV/dac	0.072
Linearity_DAC1 (1, 2, 4, 8, 16, 32, 64, 128, 256, 512)	Slope = -2.15 mV/dac	0.070
Linearity_DAC2 (1, 2, 4, 8, 16, 32, 64, 128, 256, 512)	Slope = -2.17 mV/dac	0.068
SCurve_PedestalDAC0(Step=1)	98.9 dac	1.8
SCurve_PedestalDAC1(Step=5)	96.3 dac	1.2
SCurve_PedestalDAC2(Step=5)	96.8 dac	1.2
SCurveDAC0(100 fC):(Step=1)	191.3 dac	6.5
SCurveDAC0_Gcorr(100 fC):(Step=1)	191.2 dac	2.6
SCurveDAC1(1 pC):(Step=10)	354.5 dac	15.7
SCurveDAC2(1 pC):(Step=10)	238.3 dac	10.6
Load SlowControl(Num=100): 872 param(1010101…..)	100%	

Production speed : 160 Chips/24h

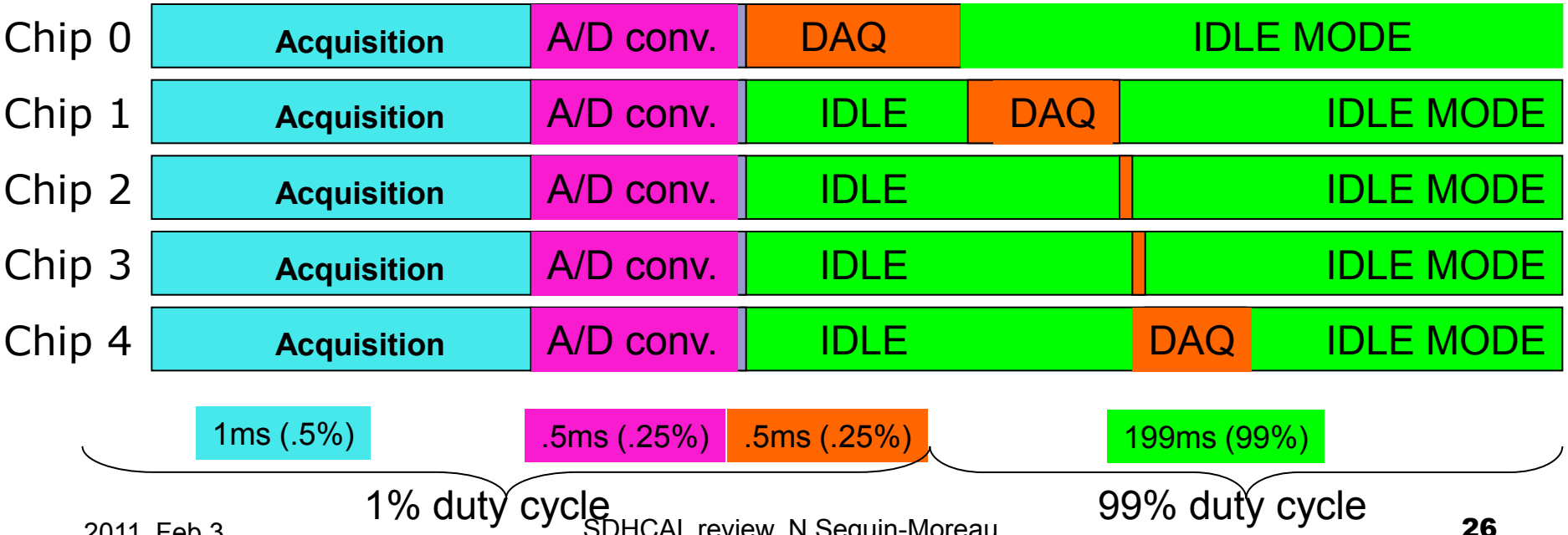
ALL: VALID[8155+1382=9537(92.59%) FAULTY[763(7.41%)]

YIELD : 92.59 %(9537)

DIF
Digital InterFace

Readout Electronics : DIF

- The DIF (Detector InterFace) = interface between the ASICs and the DAQ system.
- **Standardized interface for all detectors, to manage the daisy chain using the token ring readout**

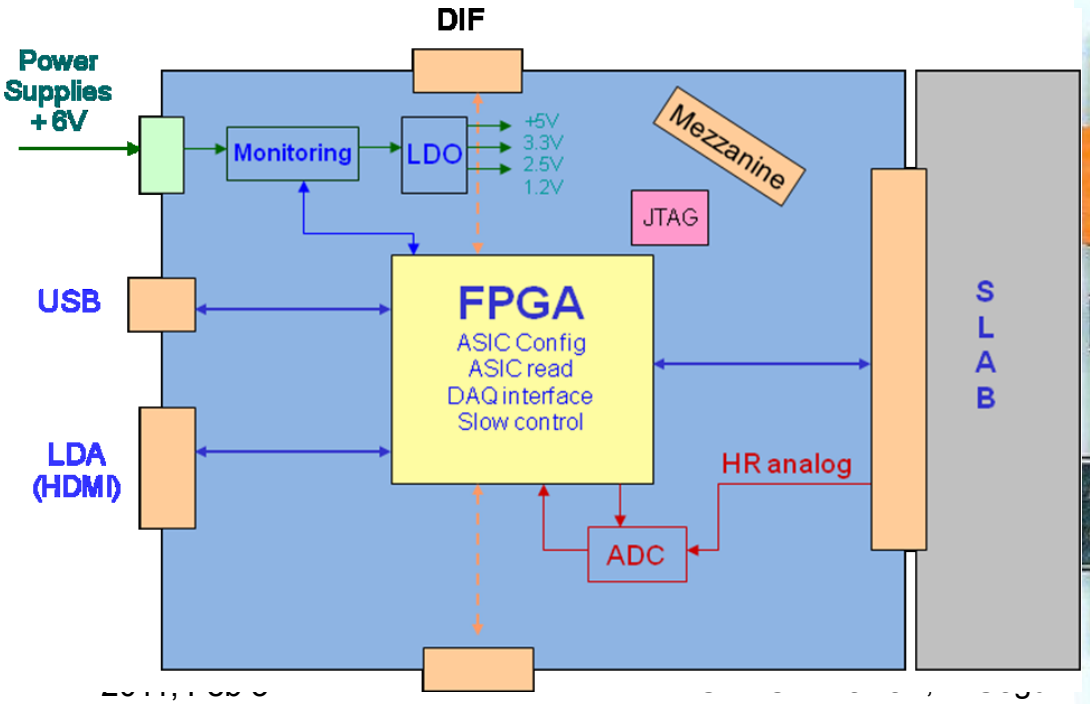


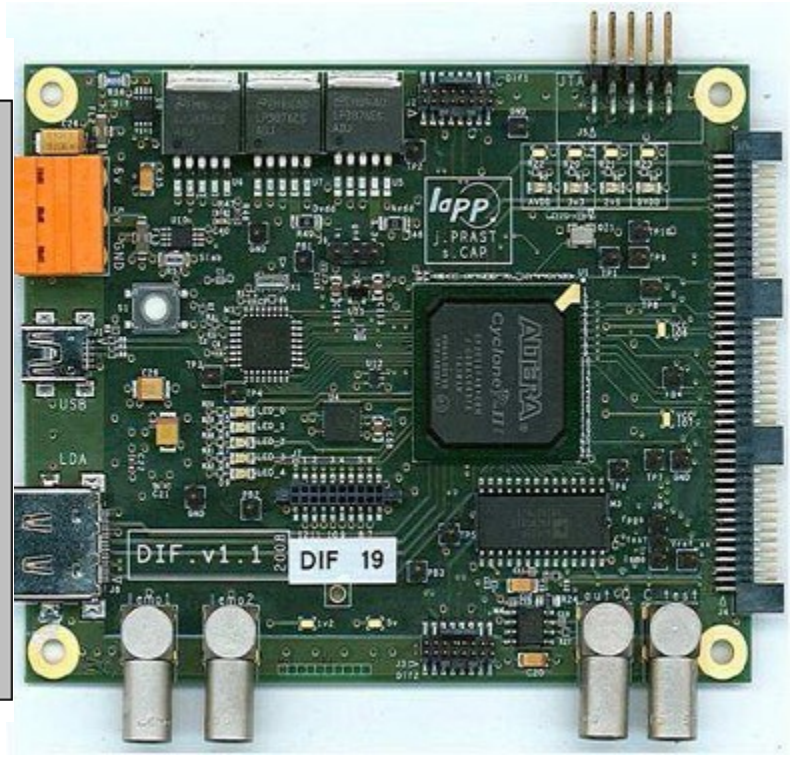
MAIN FEATURES OF THE DIF

- Slow Control parameters: Received from a PC and transmitted to the ASICs
- Launch of the acquisition, performs analog/digital readout and transmission of the data received from ASICs to a PC.
- Communication with other DIFs
- Communication with DAQ either by USB or by HDMI
- The DIF should be able to handle more than 100 ASICs theoretically. The max which has been tested is 48

DIF Architecture

- **Cyclone 3** Altera FPGA (EP3C6F484)
- **Samtec Connector** for SC parameters and analog/digital readout.
- 2 different ways to be connected to the DAQ:
  - **USB connector** (used for standalone tests, debugs and first beam tests)
  - **HDMI connector** (to be used with the prototype DAQ).
- Connector to communicate with another DIF
- **Monitoring** of the temperature of the DIF and of the current consumption of the digital and analog part of the ASICs.





DIF production and controls

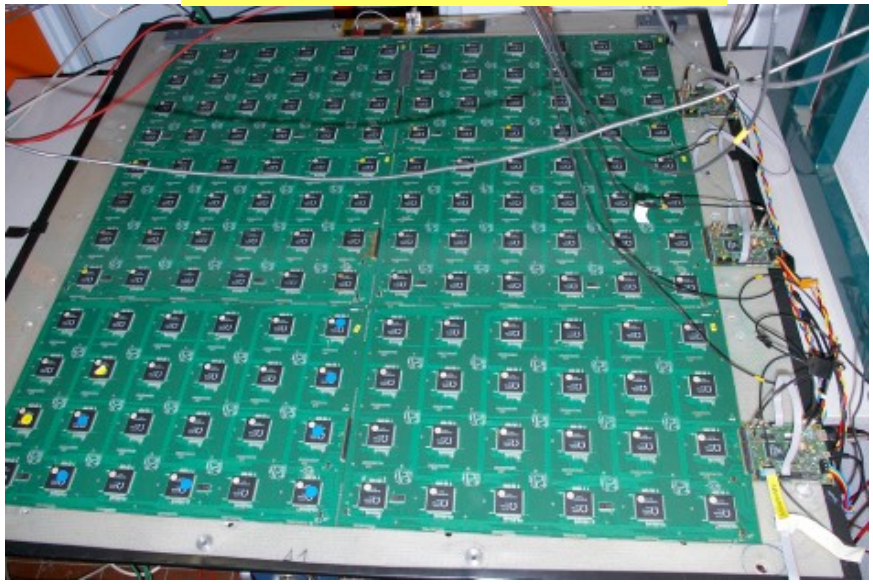
- 190 DIFs already produced and tested using a specific test bench.
- Only 7 were rejected (soldering pb for 5 of them)
- 183 DIFs are ready to be used
- 3 DIFs/1 m^2

CONCLUSION

- 10 300 HR2b tested
  - Test: Yield 93%=> 9537 HR2B available to equip 66 cassettes

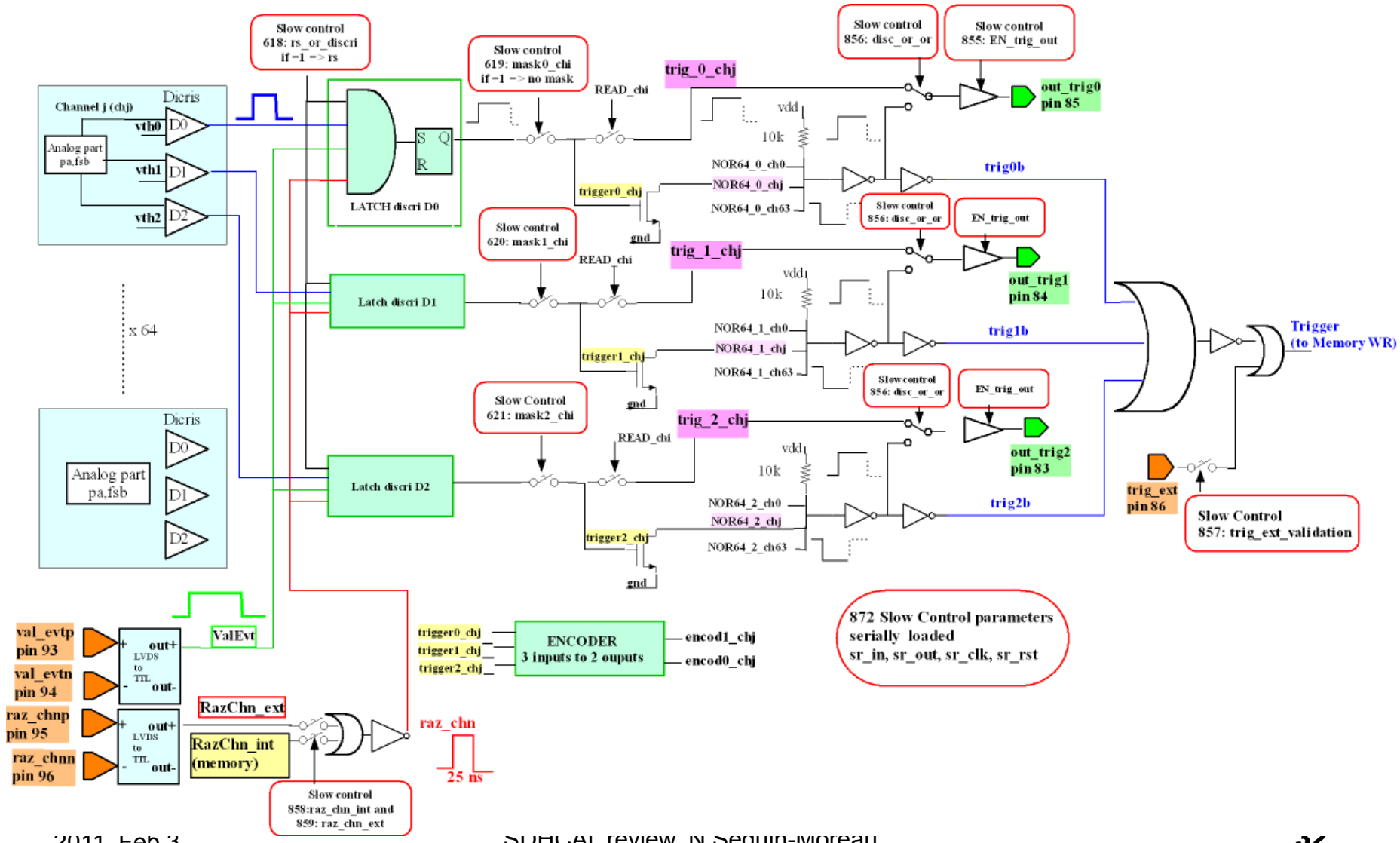
- Validation of a $1m^2$ in test beam
  - Asics and DIF
    - Power pulsing (no external components)
    - Daisy chain

144 chips/$1m^2$ board

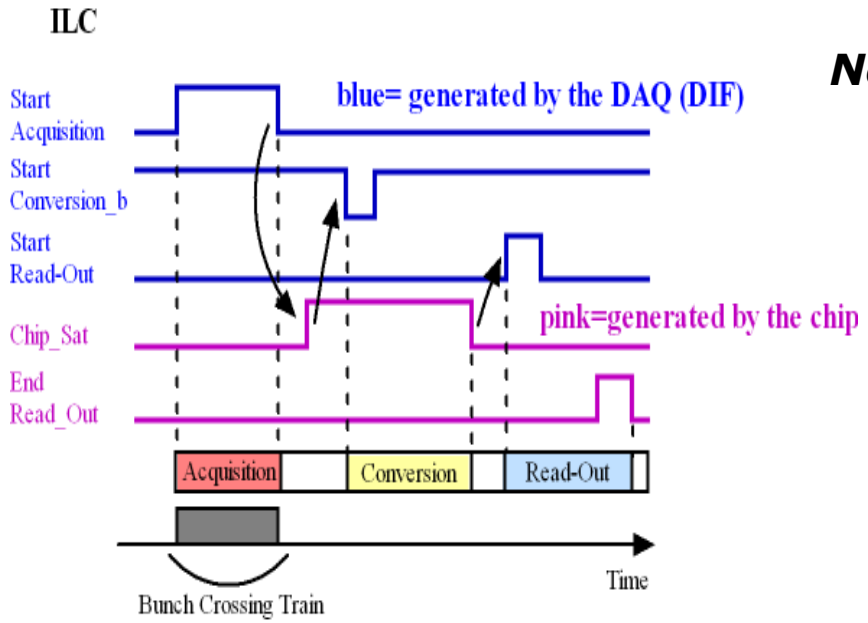


READOUT ELECTRONICS BACK UP SLIDES

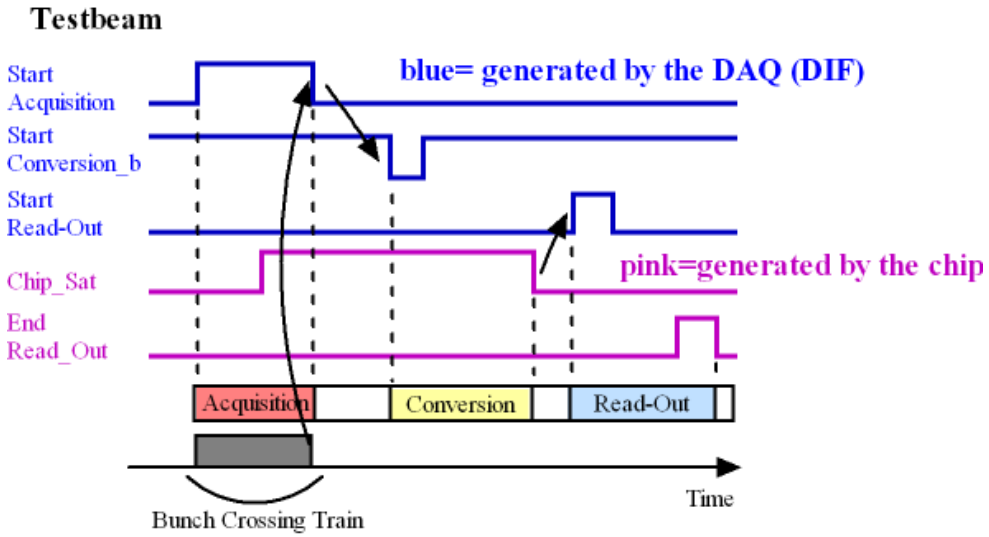
Analog to Digital schematics



TIMINGS: ILC/TESTBEAM

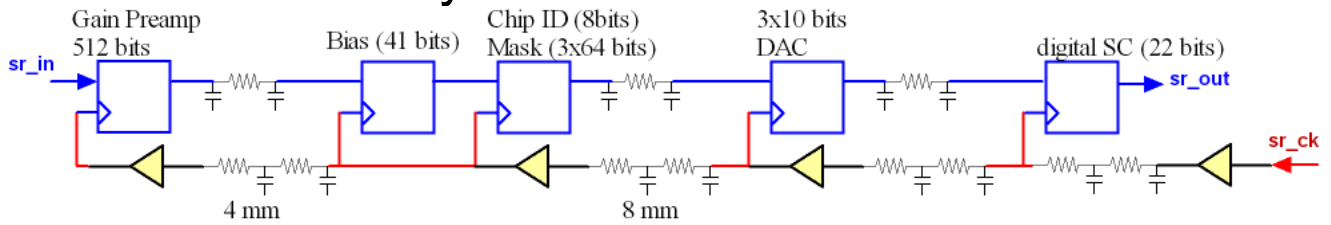


No conversion in Hardroc

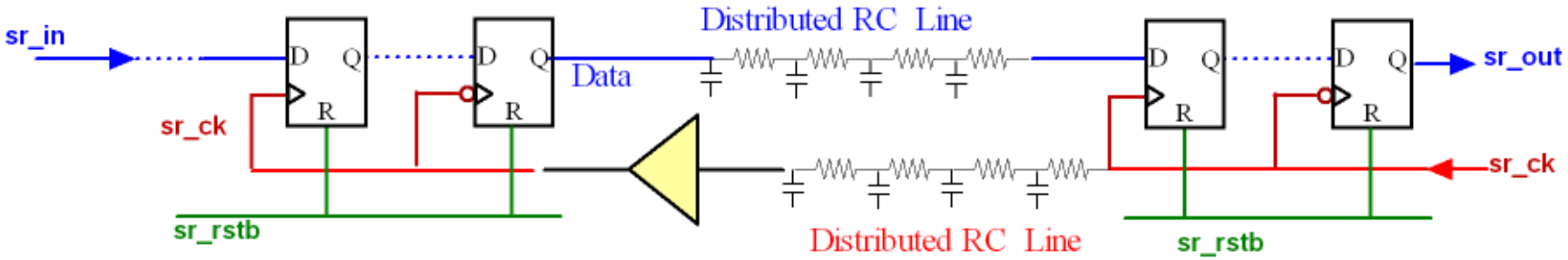


SC pb solved in HARDROC2b:

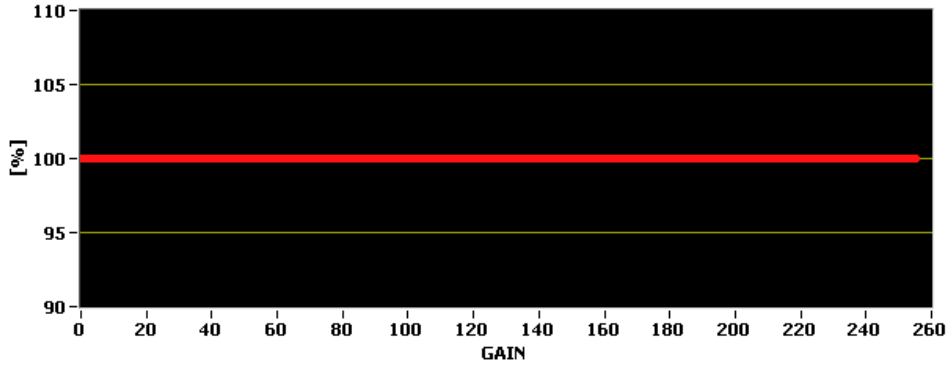
- Buffers added on the Clk only



64 x 8 bits= 512 SC parameters for Gain correction



100% success for the SC @ Vdd=2.6V, temperature increased

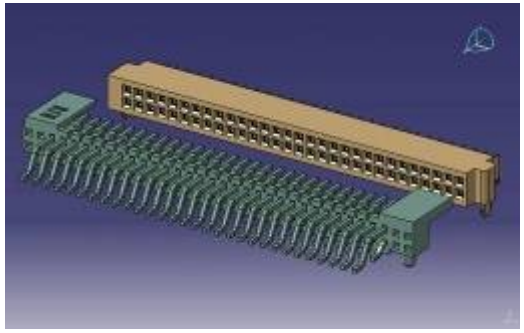


- 36 HR2b measured in Lyon: 100% success when sending the difficult SC config=10101…10, 100 times

DIF: SAMTEC pinout

- 90 pins **common** connector (DIF task force)
- Reliability:
  - Data, TransmitOn, StartReadout and EndReadout signals: doubled for redundancy, bypass using SC

	N pins
Analog	3
User Single Ended	22
Controls Single Ended	5
Digital Readout	12
Power pulsing controls	5
LVDS signals	16
Slow controls signals	8
POWER pins	6
GND	13
TOTAL	**90**

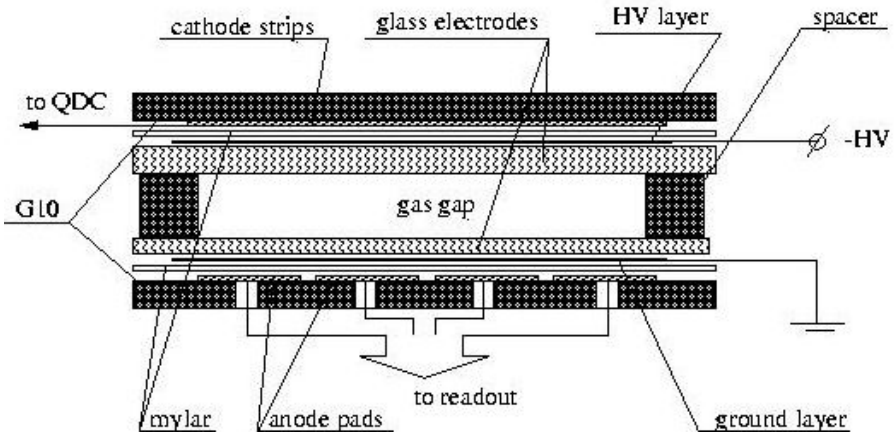


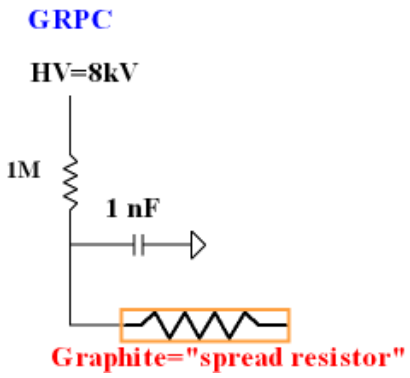
Samtec FSH/ SFMH ?

GND	1	2	GND
MUX3_CSn	3	4	Analog_0
MUX2_CSn	5	6	GND
MUX1_CSn	7	8	Analog_1
spare1	9	10	GND
MUX_ENN	11	12	C_test
MUX_WRN	13	14	GND
spare2	15	16	MUX_A4
en_otaq	17	18	MUX_A3
GND	19	20	MUX_A2
SR_reset	21	22	MUX_A1
hold	23	24	MUX_A0
spare3	25	26	Ramfullext
SR_IN	27	28	Reset_BCID
spare4	29	30	GND
SR_OUT	31	32	Resetn
spare5	33	34	Start_Conv_daqb
SR_clk	35	36	End_Readout
GND	37	38	Start_acq
TransmitOn_3	39	40	RamFull
Pwr_analog	41	42	Dout_3
TransmitOn_2	43	44	GND
Pwr_dac	45	46	Dout_2
Pwr_ss/Pwr_sca	47	48	Start_Readout
GND	49	50	Trig_ext
TransmitOn_1	51	52	Start_Readout_Bypass
Pwr_digital	53	54	Dout_1
TransmitOn_0	55	56	GND
Pwr_adc	57	58	Dout_0
SC_SROUT	59	60	SC_SRIN_BYPASS
SC_SROUT_BYPASS	61	62	SC_SRIN
SC_select	63	64	SC_reset
SC_clk	65	66	SC_load
User_LVDS_P	67	68	User_LVDS_N
Trig_Ext_P	69	70	Trig_Ext_N
DVDD	71	72	AVDD
Clk_5MHz_0_P	73	74	Clk_5MHz_0_N
Clk_5MHz_1_P	75	76	Clk_5MHz_1_N
GND	77	78	GND
Clk_40MHz_0_P	79	80	Clk_40MHz_0_N
Clk_40MHz_1_P	81	82	Clk_40MHz_1_N
DVDD	83	84	AVDD
Raz_Chn_P	85	86	Raz_Chn_N
Val_Evt_P	87	88	Val_Evt_N
AVDD	89	90	AVDD

HV sparks (ESD)

- **GRPC:** HV=8 kV, PADs= a few pF
- ASIC inputs:
  - protection PADs (AMS library): robustness up to 2kV HBM (100pF)
  - High spread resistor= isolates FE inputs

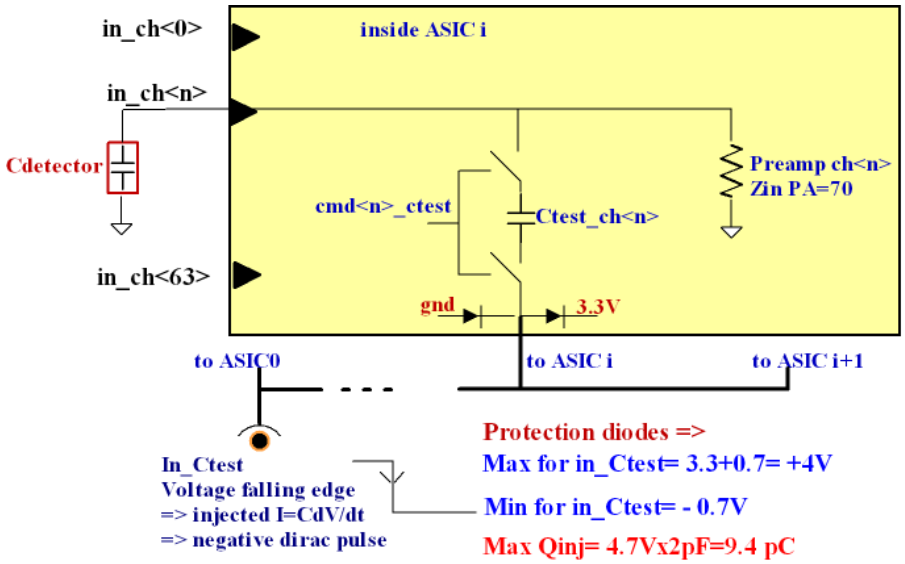


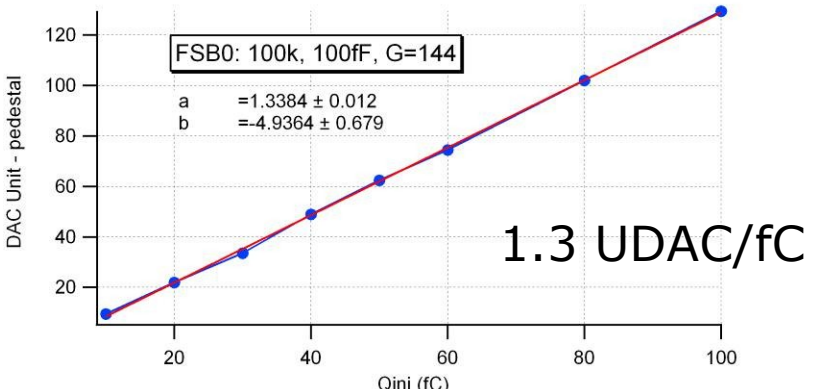


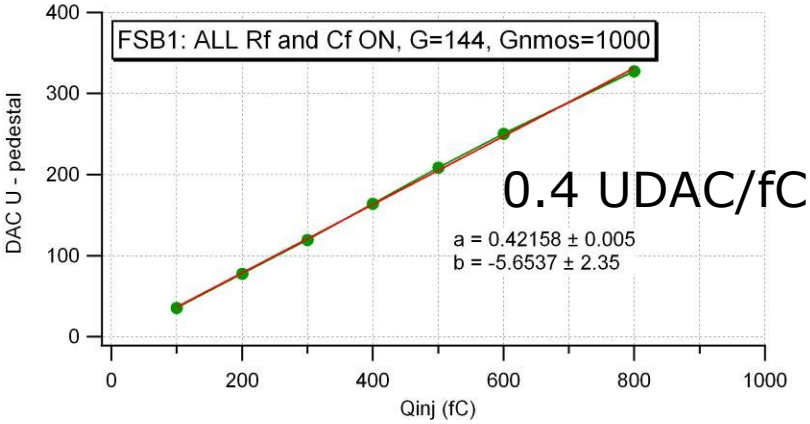
CALIBRATION

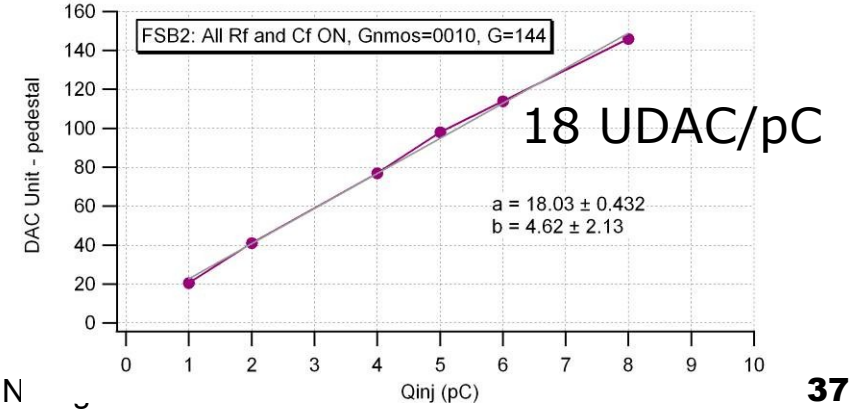
TEST BENCH measurements:

- RPC signal: dirac current
  - Fsb0: for input charges from 10fC up 100fC
  - Fsb1: for Qinj from 100fC to 1pC
  - Fsb2: for Qinj from 1pC up to 10pC





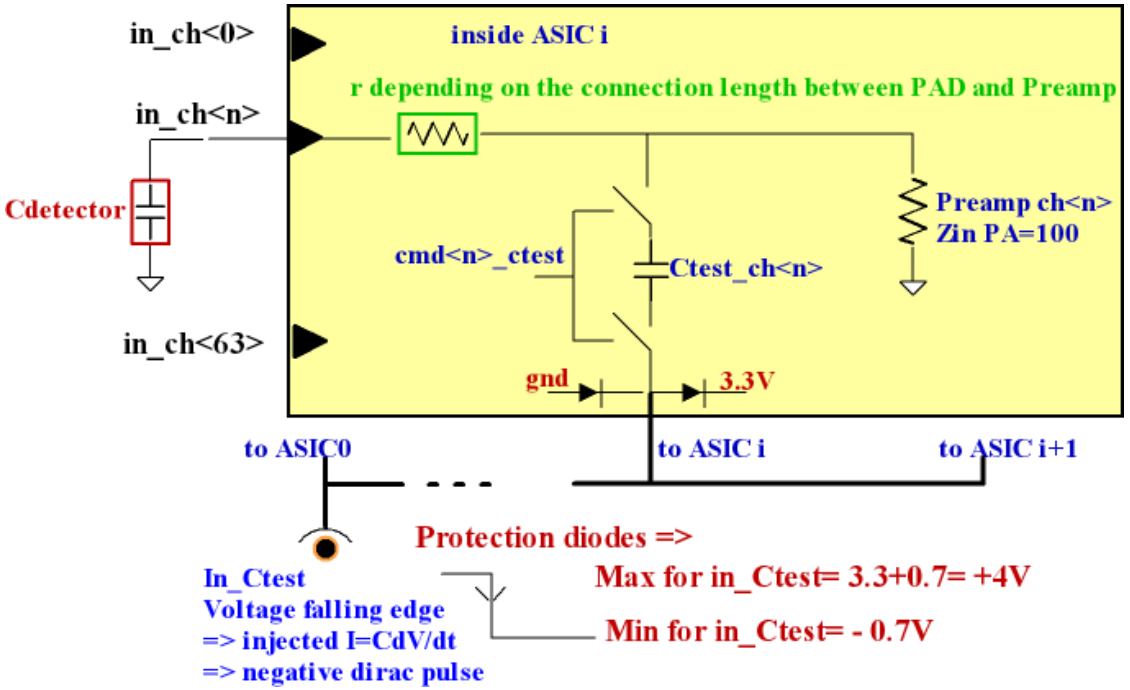




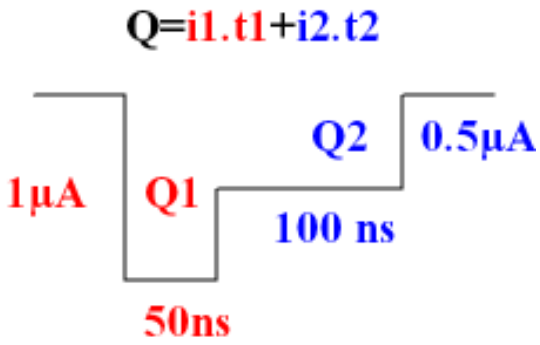
MAXIMUM Qinj through Ctest:
about 9pC (protection diodes)

CALIBRATION

- RPC signal:
  - dirac current

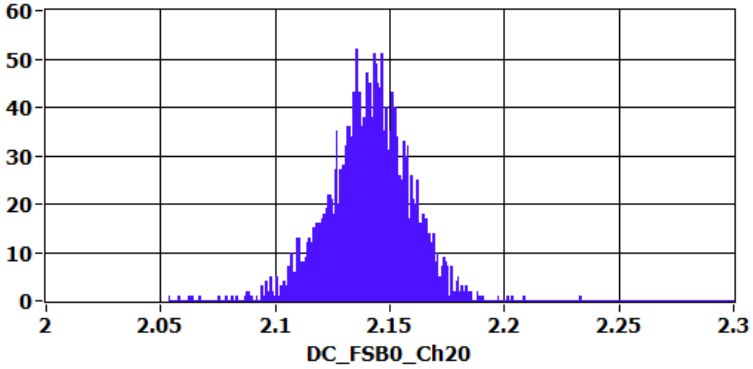


- Micromegas signal:

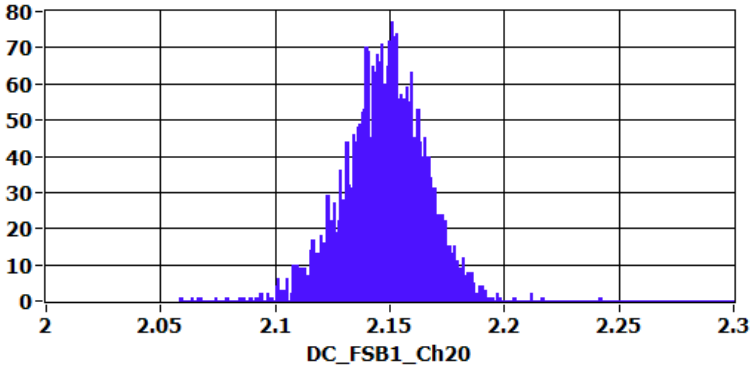


=> HARDROC FSB is too fast compared to the megas signal

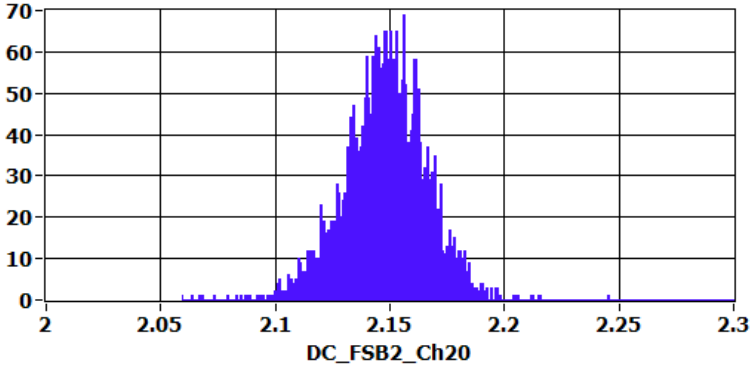
Statistics: 9500 HR2b, DC Level Fast Shaper 0, 1 and 2, Channel 20



Fsb0:
Mean : 2.141 V
Dev : 0.02 V
Max: 2.3 mV
Min : 2.053 mV



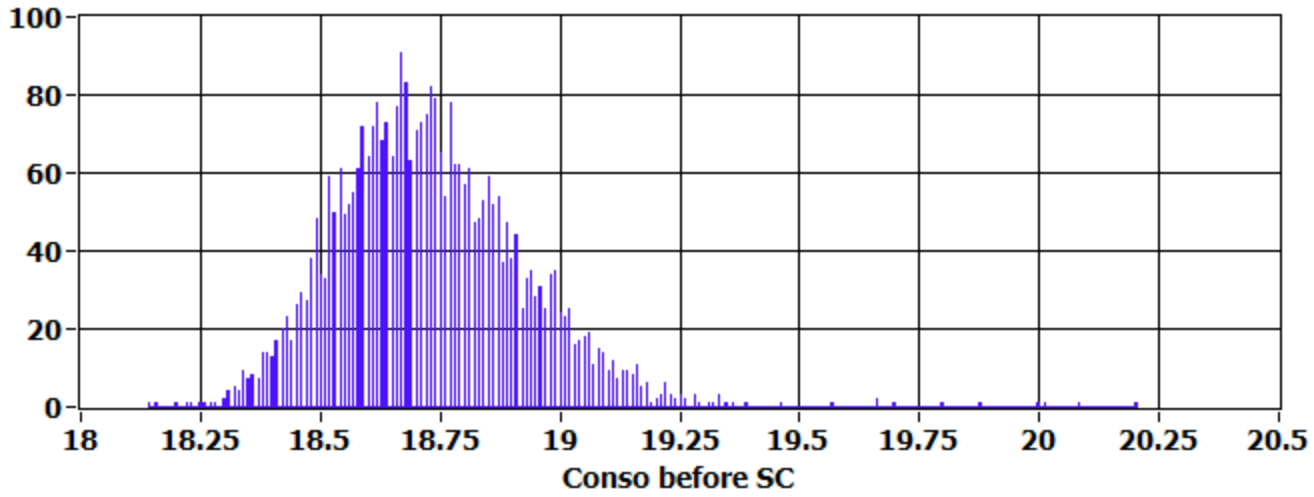
Fsb1:
Mean : 2.148 V
Dev : 0.02 V
Max: 2.3 mV
Min : 2.058 mV



Fsb2
Mean : 2.148 V
Dev : 0.02 V
Max: 2.3 mV
Min : 2.059 mV

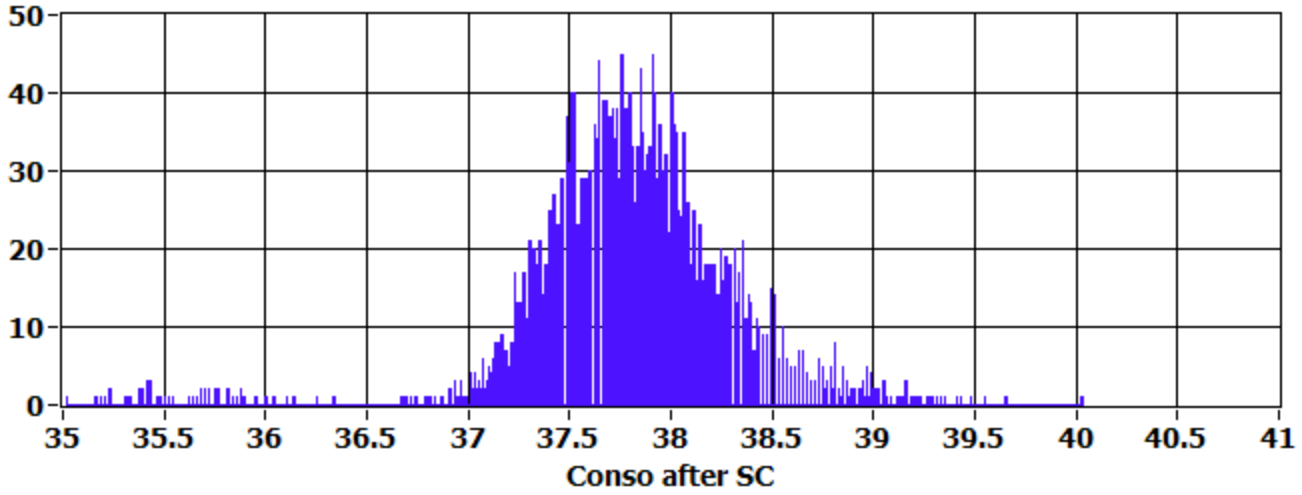
STATISTIC (9500 H2B) CONSUMPTION

Consumption before loading Slow Control



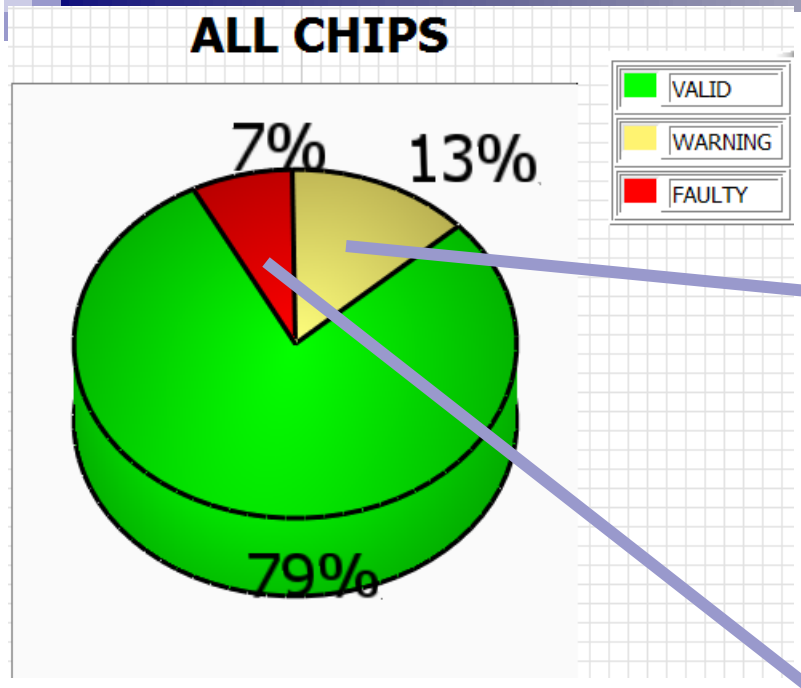
Mean : 18.7 mV
Dev : 0.2 mV
Max: 20.2 mV
Min : 18.1 mV

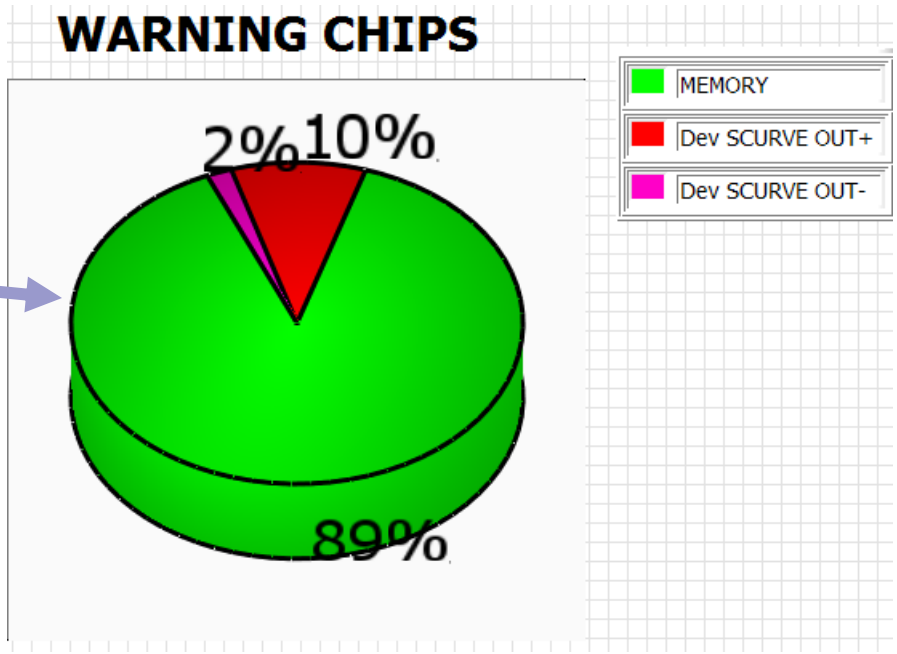
Consumption after loading Slow Control



Mean : 37.8 mV
Dev : 0.5 mV
Max: 40.0 mV
Min : 35.0 mV

STATUS 06/01/2011 : 10300 Chips(H2B) : Tested

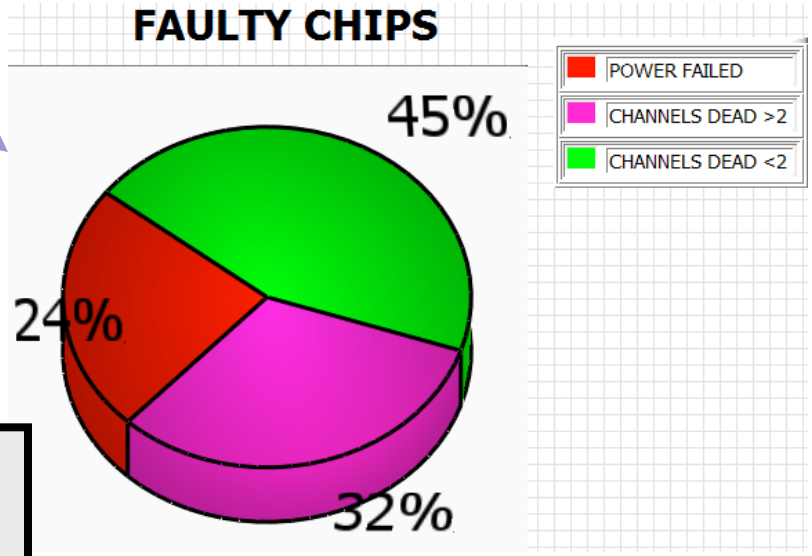




Test_Prod_h2b_Bi_B(i+26) = 27*36=972 Chips

VALID[Nvalid+Nwarning(%)] FAULTY(Nfaulty(%)]

Test_Prod_h2b_B1_B27.xls	VALID[791+130=921(94.75%)]	FAULTY[51(5.25%)]
Test_Prod_h2b_B28_B54.xls	VALID[771+132=903(92.90%)]	FAULTY[69(7.10%)]
Test_Prod_h2b_B55_B81.xls	VALID[774+135=909(93.52%)]	FAULTY[63(6.48%)]
Test_Prod_h2b_B82_B108.xls	VALID[799+115=914(94.03%)]	FAULTY[58(5.97%)]
Test_Prod_h2b_B109_B135.xls	VALID[730+147=877(90.23%)]	FAULTY[95(9.77%)]
Test_Prod_h2b_B136_B162.xls	VALID[739+155=894(91.98%)]	FAULTY[78(7.02%)]
Test_Prod_h2b_B163_B189.xls	VALID[795+104=899(92.49%)]	FAULTY[73(7.51%)]
Test_Prod_h2b_B190_B216.xls	VALID[789+127=916(94.24%)]	FAULTY[56(5.76%)]
Test_Prod_H2b_B217_B243.xls	VALID[739+138=877(90.23%)]	FAULTY[95(9.77%)]
Test_Prod_H2b_B244_B270.xls	VALID[761+124=885(91.05%)]	FAULTY[87(8.95%)]
Test_Prod_H2b_B271_B287.xls	VALID[467+75=542(91.05%)]	FAULTY[38(8.95%)]



ALL: VALID[8155+1382=9537(92.59%) FAULTY[763(7.41%)]

YIELD : 92.59 %(9537)

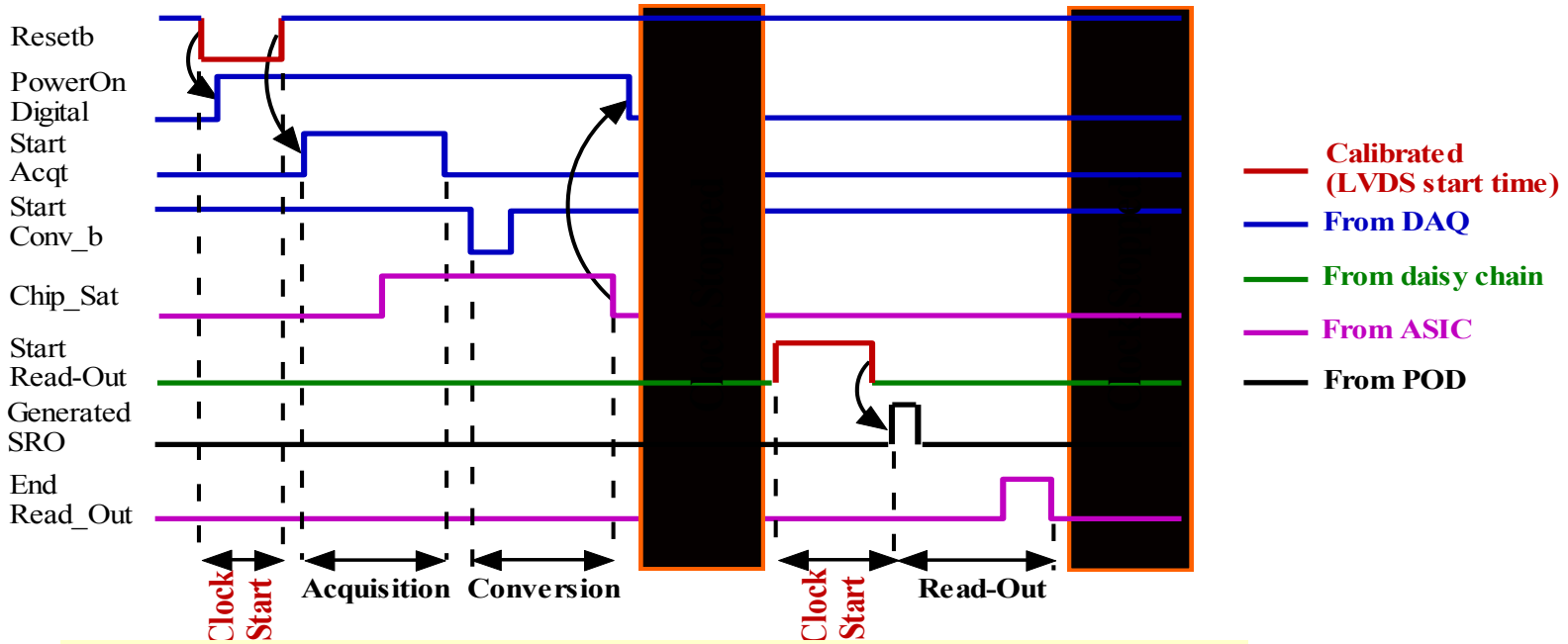
Retail Prod : ftp://lyoftp.in2p3.fr/ilc/TESTS_PROD_H2B/

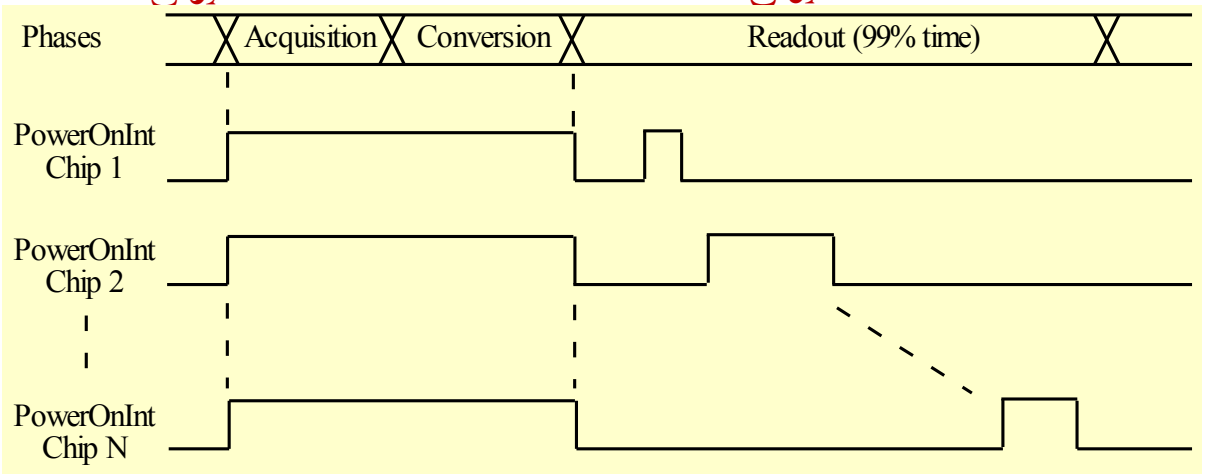
Power pulsing sequence (with 5MHz and 40 MHz)

- 25 µs or 50 µs between pwrON A+DAC and pwr_ON_D
- 200 ns or 500 ns (stabilisation time of LVDS receivers) between rising edge of Pwr_on_D and rising edge of resetb
- 1 µs or 5µs (internal gestion of the digital reset) between rising edge of resetb and rising edge of START_ACQ
- 2µs between falling edge START_ACQ and falling edge PWR_ON_D (gestion of the end of acquisition by the state machin)
- 2 or 10µs (stop of the pod module) between falling edge of PWR_ON_D falling edge of PWR_ON_ A + DAC

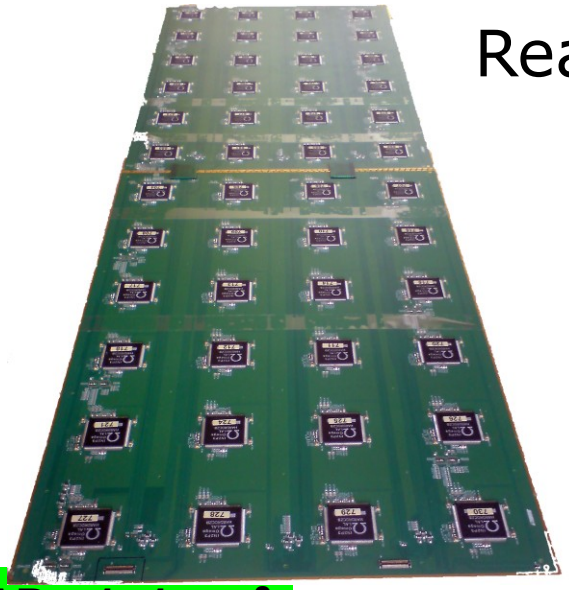
POWER PULSING: Power On Digital (POD) module

- PowerON **start/stop clocks** (40 MHz and 5 MHz) and **LVDS receivers bias current** to meet power budget



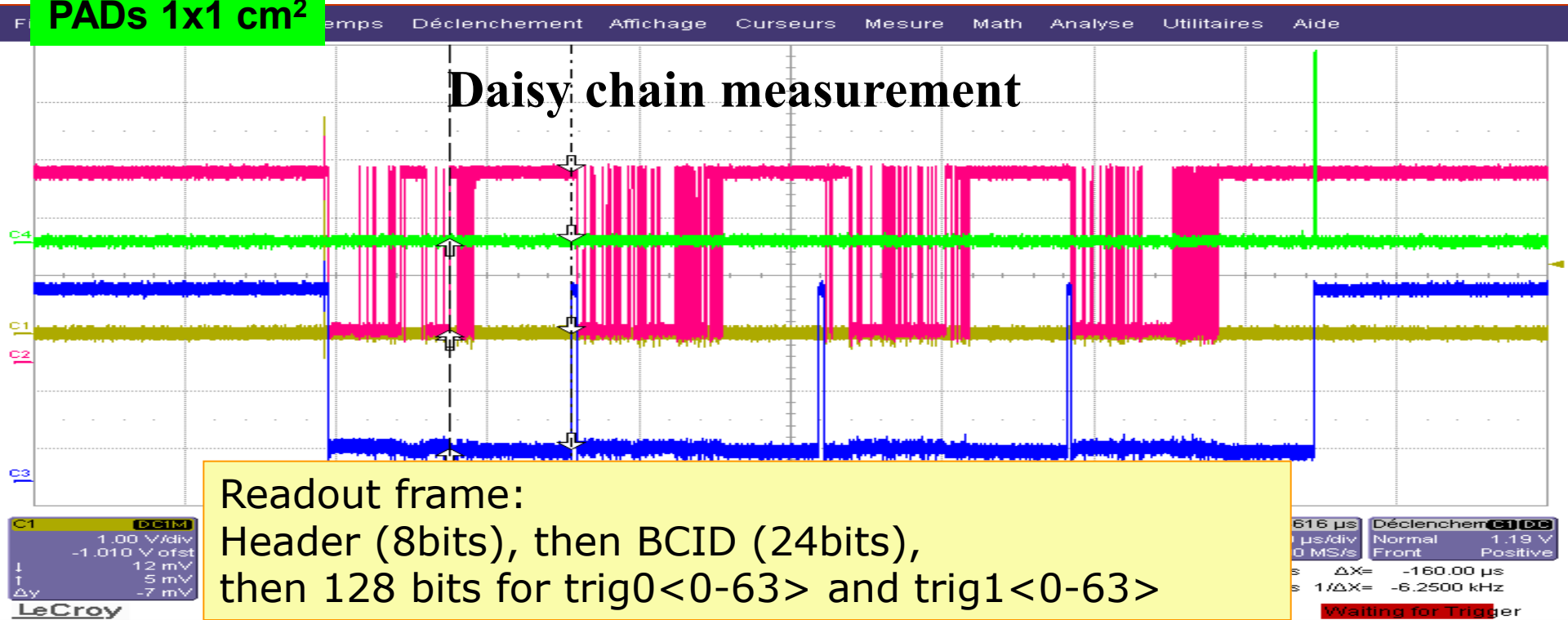


Readout Electronics in TESTBEAM



Semi-digital electronics readout system validated in beam conditions (daisy chain,stability, efficiency, no external componant)

PADs 1x1 cm²



Readout frame:
Header (8bits), then BCID (24bits),
then 128 bits for trig0<0-63> and trig1<0-63>