

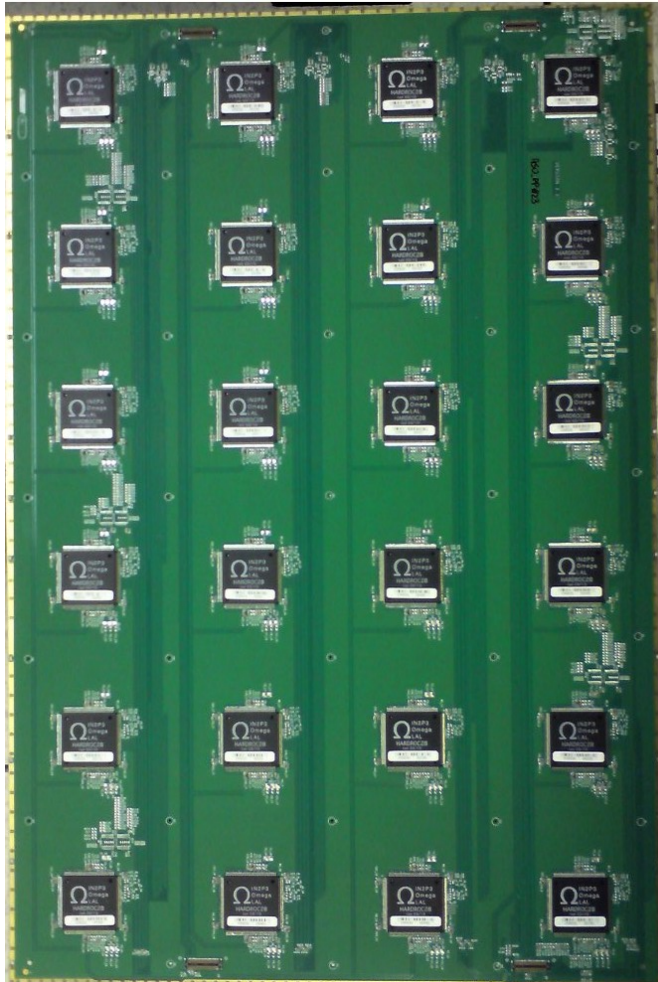
# ASU board: PCB production and testings

GRPC-SDHCAL Review Meeting

# Presentation outline

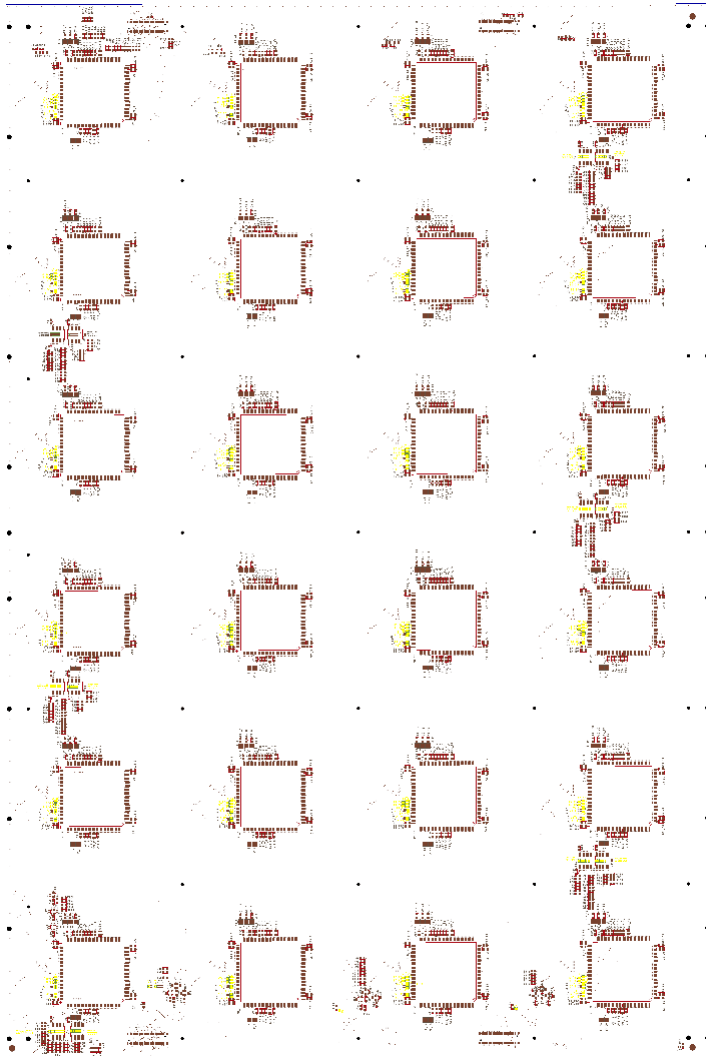
- Active Sensor Unit electronic board
  - quick reminder
  - board functional decomposition
  - testing issues
- square meter (m<sup>2</sup>) board
  - reminder
  - integration scenario
- m<sup>2</sup> boards production: provisional plan

# The ASU board: reminder



- 2 main functions:
  - interface front-end electronics  $\leftrightarrow$  GRPC
  - functional support for 24 HARDROCs
- production outsourcing:
  - PCB fabrication (sample production checks)
  - board assembly (components soldering: visual inspection)
- functional checks performed at IPNL

# ASU board structural aspects



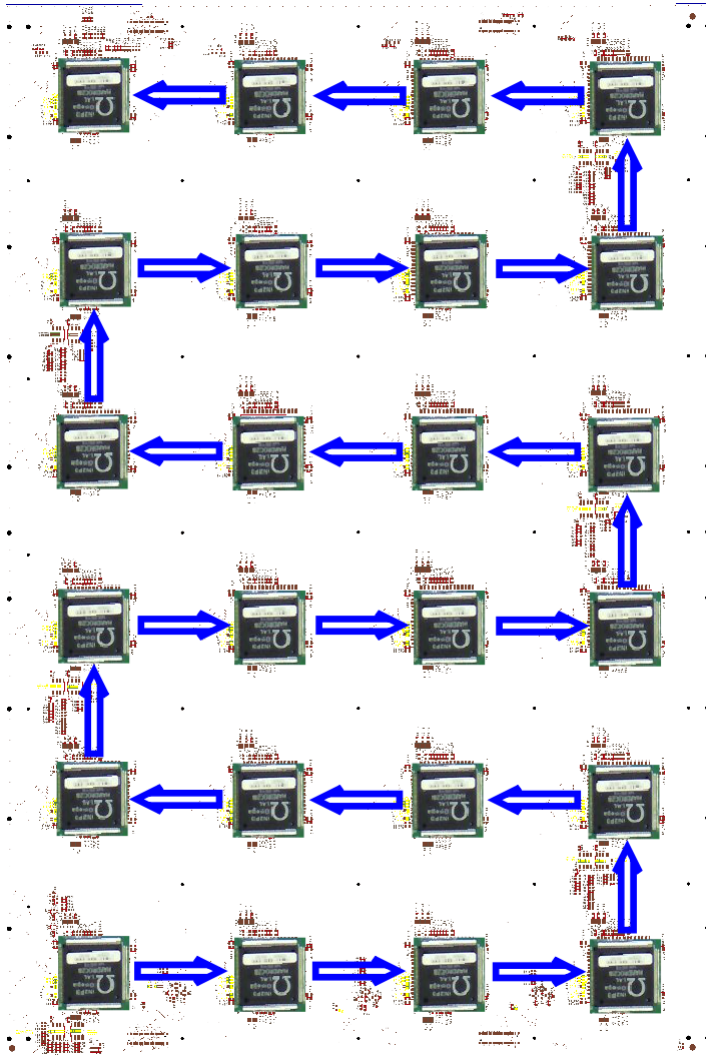
- **HARDROC (HR)**
  - 24 asics/board
  - all asics daisy chained
  - only active device
- input pads
  - 64 pads/HARDROC (1 cm<sup>2</sup>)
  - board BOTTOM side
- interconnections
  - 4x 80pin smd connectors
  - pwr supply + HR ctrl data
- board configurability
  - 3 ASU board configurations
  - 310 closed straps (362 total)
  - 22 matched lines terminations

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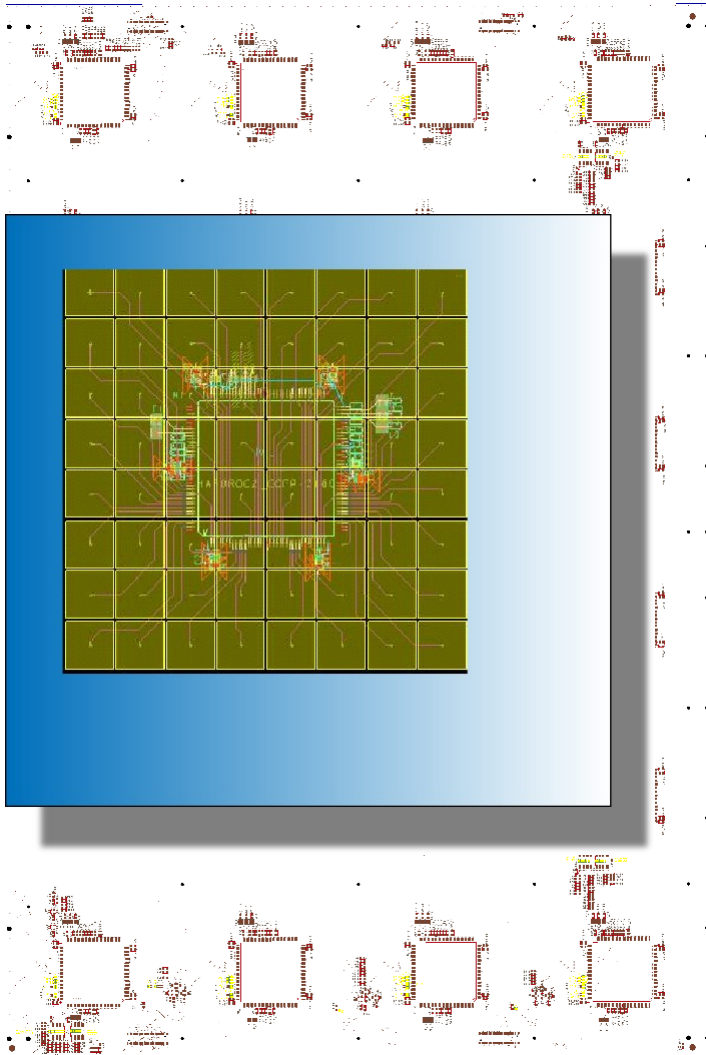
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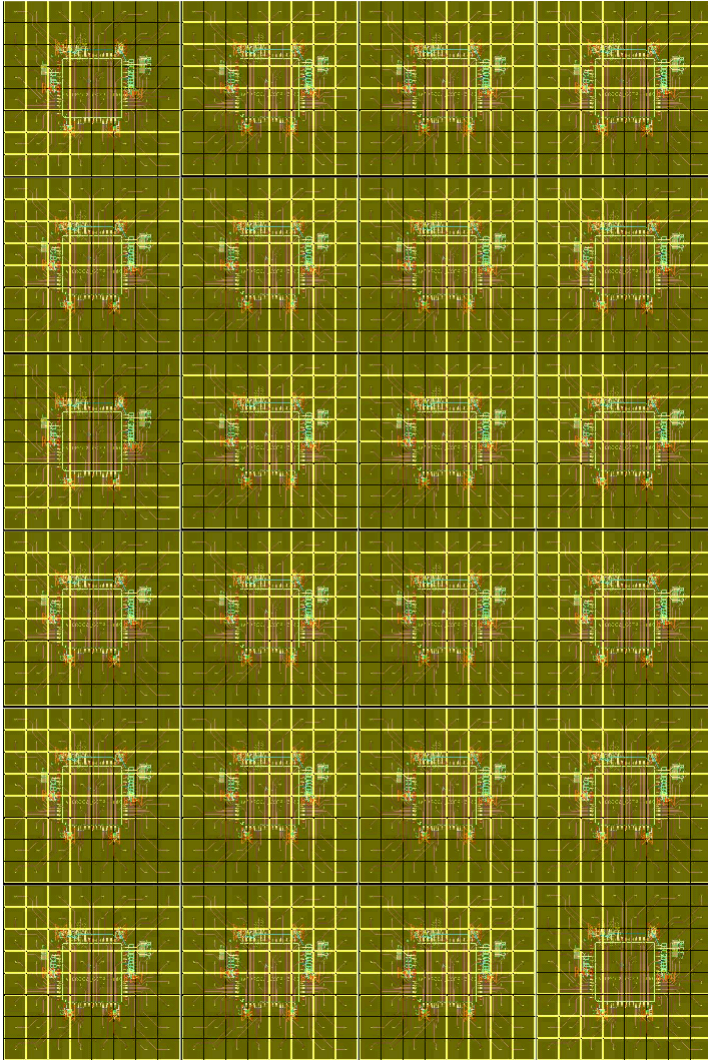
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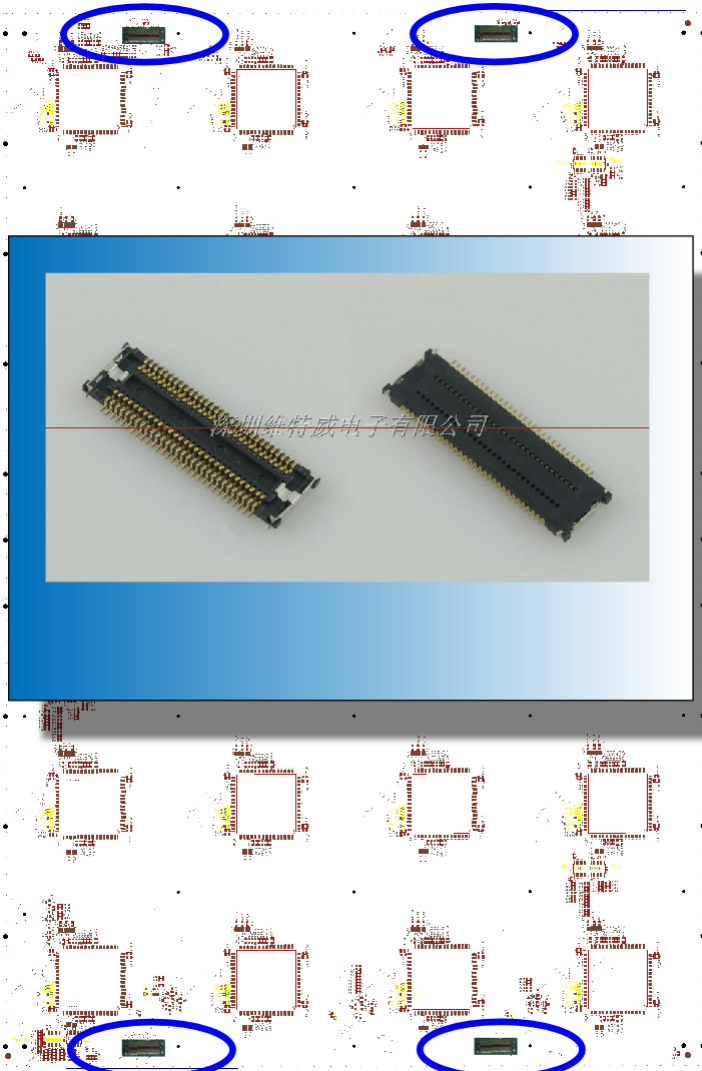
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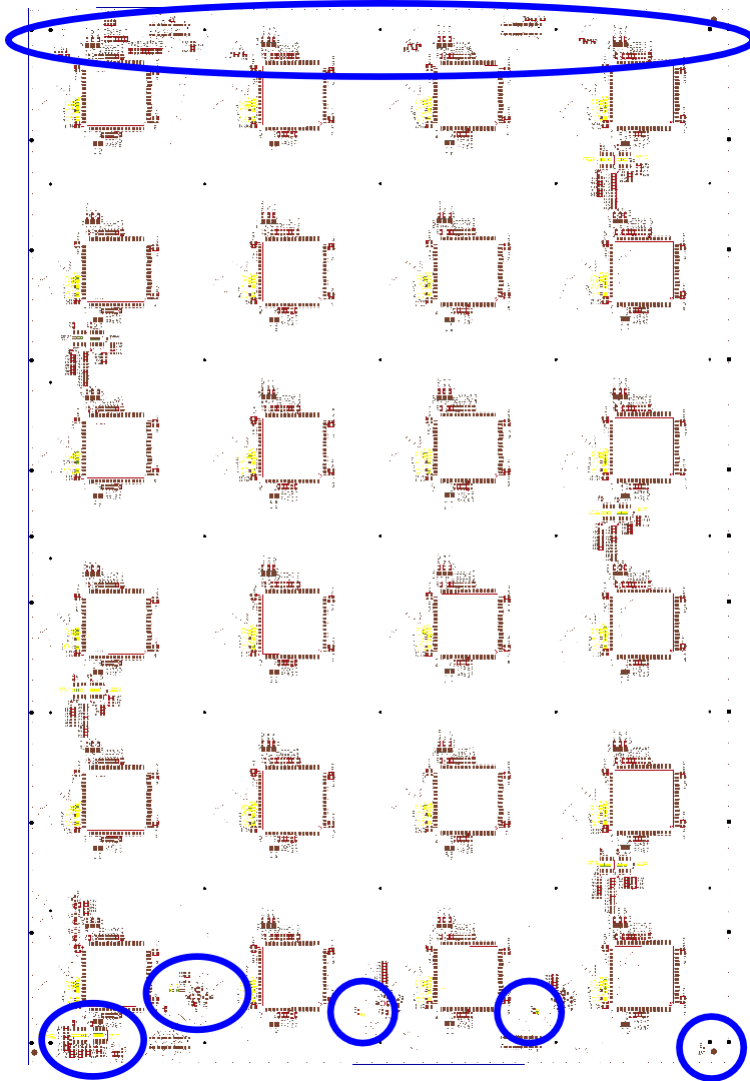


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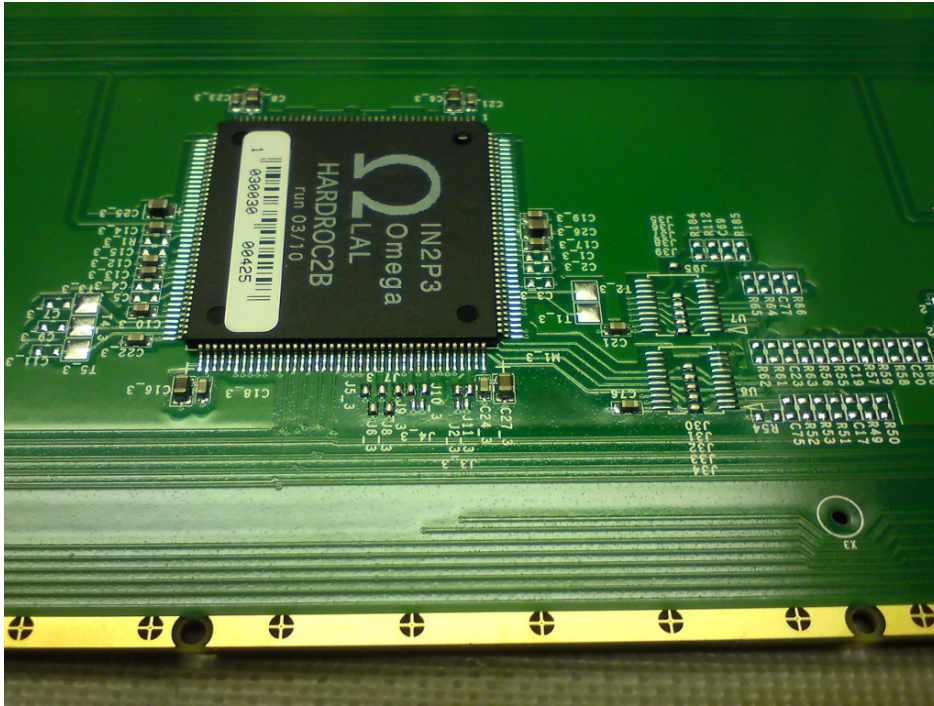
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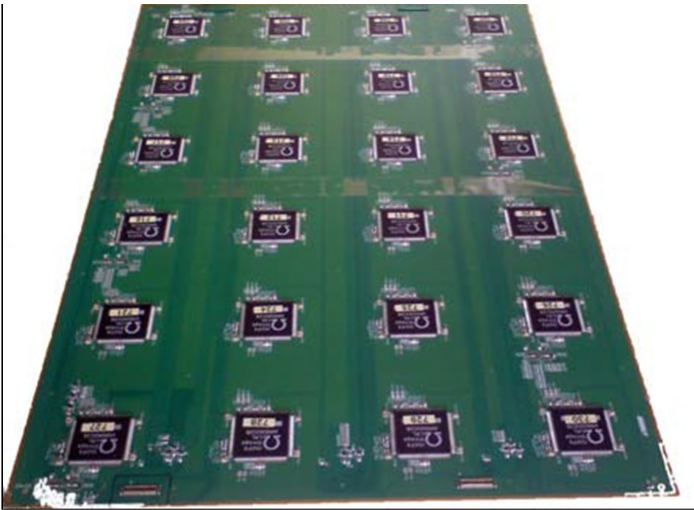
# ASU board: 3 configurations



- **only 2 cfg used for m3 integration**
  - “production” cfg only used for single board testing
  - “slab 1st” + “slab 2nd” used in slab integration
- different configurations made by straps and passive components
- test strategy:
  - all configurations need to be checked

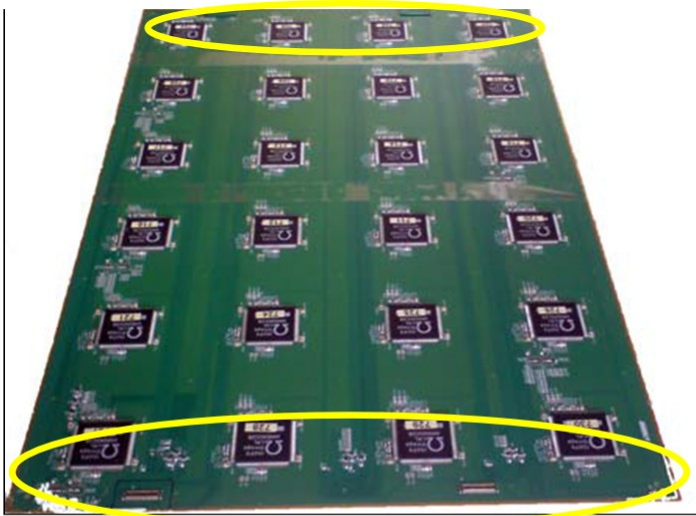
# ASU board: test strategy

- **functional test at each integration stage:**
  - the "production" board must pass a functional test
    - boards are reconfigured either as "slab 1st" or "slab 2nd"
  - the slab is functionally tested
    - 3 slabs are integrated in a m2 board
  - the m2 board is functionally tested before integration with the GRPC
    - the m2 is integrated into his cassette
  - the integrated cassette must pass a complete functional test
- two separate test benches will be used
- functional tests: GO / NO GO strategy

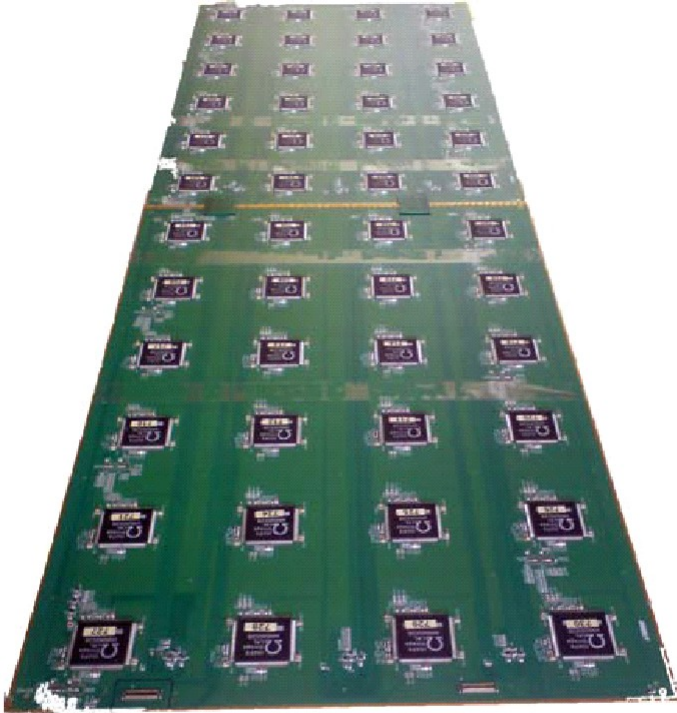


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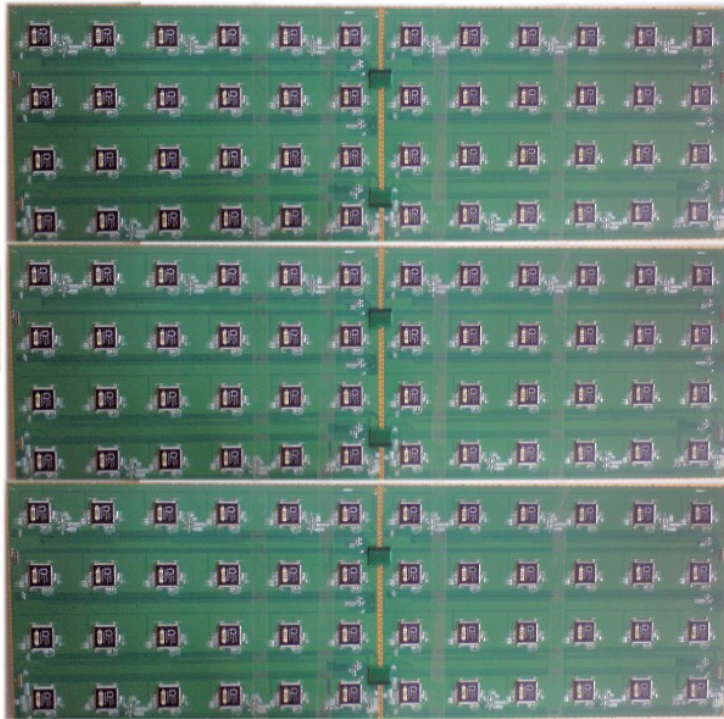


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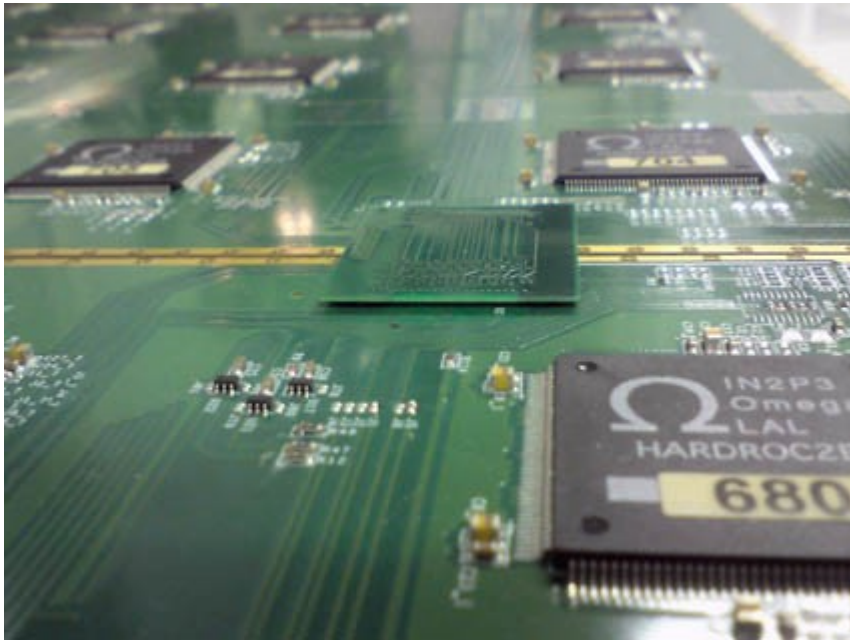
# board/slab/m2 test benches



- two separate test benches:
  - 1 pc with XDAQ
  - DIF + DIF-ASU boards
  - DAQ software
- GO / NO GO strategy
  - no debugging
- only functional tests:
  - power consumption
  - HR slow control
  - pedestal acquisition runs
  - HR calibration feature (CTEST)
- goals:
  - checking all functionalities/connections
  - electronics checks at each integration step



# m2 integration scenario



- components:
  - 6x ASU boards
  - 6x ASU-ASU interlinks
- boards and interlinks already configured and tested before integration
- integration procedure:
  - ASU boards soldered together by the mean of copper gasket
  - m2 board tested as a whole
- goal: one m2 board/day

# m2 boards mass production

- boards' needs for the 40 layers prototype:
  - 240x ASU + 240 ASU-ASU + 120 DIF-ASU
- production run is:
  - 20(pre-series available) + 280(<8weeks availability) ASU
  - 330(PCB available) ASU-ASU
  - 150(PCB available) DIF-ASU
- status:
  - launching of the 280 ASU series still pending
    - testing of prototypes+preseries shows HR mortality (10%)
    - plan: accelerated stress testing of HR production sample
  - DIF-ASU and ASU-ASU **preseries** (assembly) launched
- provisional planning:
  - AST to assess infant mortality of HARDROCs
  - launching of the 280 ASU series (**PCB**: availability of the 1st lot is 4weeks)
  - launching of the DIF-ASU and ASU-ASU **series** (assembly)
  - testing of the DIF-ASU and ASU-ASU **preseries** and **series**
  - ASU boards mass production (producer throughput to be assessed)
  - start m2 boards integration and test (1m2/day)