

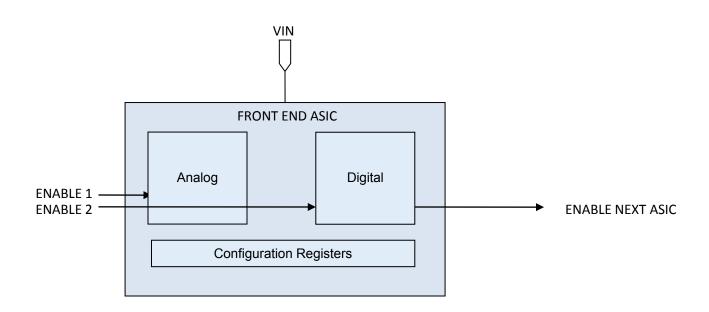
## CLIC and ILC Power Distribution and Power Pulsing Workshop

**Summary Document** 



- Defining "Power Pulsing".
- Power Pulsing Challenges (Marc).
- Main Schemes that were presented.
- How to test / What to test.





- Enable/Disable of internal functions of FE ASICs to reduce current consumption.
- Analog and Digital Functions can be enabled independently.
- Configuration registers are always powered to avoid reconfigurations.
- Enable signals can be daisy chained for sequencing several ASICs.





- Mechanical system issues
  - Mechanical stress due to Lorentz forces
  - Resonant vibration of wire-bonds
- Electrical system issues
  - induced voltage due to cable inductance (and IR drops)
  - Electromagnetic interference
- Other
  - severe mass constraints and lack of space for near chip and near module charge storage
  - severe mass constraints and lack of space for near module regulators and DC-DC converters
  - radiation effects on electronics





- With DC to DC Converters
- With LDO regulators and BestCaps/SuperCaps.
- Constant current source and storage caps + LDO/DCDC
- In serial powering configuration.

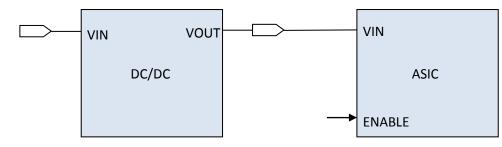




With DC to DC Converters

VOUT is constant, independently of the load current.
VOUT < VIN

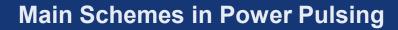
VIN is constant IIN < IOUT, it follows the load current variations.



$$D = \frac{V_{OUT}}{V_{IN}}$$

$$I_{IN} = I_{OUT} \cdot D$$

- ENABLE function implemented at FE ASIC
- Turn on/off times of FE Power Pulsed Function Blocks.
- DCDC follows the load current variations.

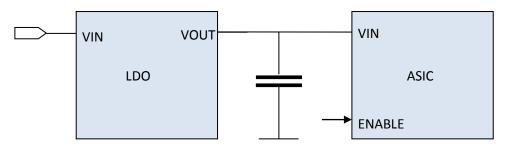




With Regulators

VOUT is constant, independently of the load current.
VOUT < VIN

VIN is constant IIN = <lload>, no peak current at input.



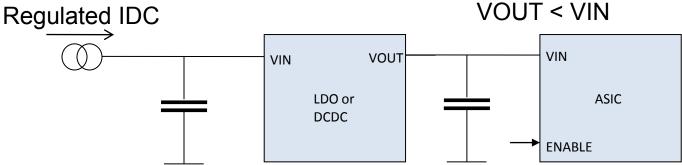
- ENABLE function implemented at FE ASIC
- Turn on/off times of FE Power Pulsed Function Blocks.
- The LDO is unable to deliver the peak current.
  - The transient charge is delivered by a storage capacitor





With constant current source

VOUT is constant, independently of the load current.



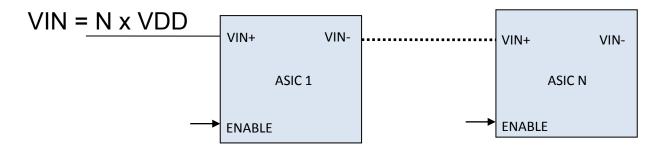
- Keep input current low and stable, energy in first storage cap
- LDO or DCDC to deliver FE voltage with power peak capability
  - Eventually with output storage cap?



Serial Powering

VOUT is constant, independently of the load current.

VOUT < VIN



- High Voltage on VIN, constant current, shunt regulators.
- Load current variations regulated by shunt regulator in ASICs
  - Does not lead to reduced power: the current is just shunted in a resistor.
- Combination with storage caps might be considered.



- Lab condition testing using active loads instead of detectors
  - DCDC dynamic behavior with peak transient currents
  - Dynamic studies of LDO/BestCap behavior.
  - Optimized configurations can after that be tested on real setups.
- What are the real setups available for these tests?