Power Consumption of CMOS Sensors for an ILD Vertex Detector

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Contents

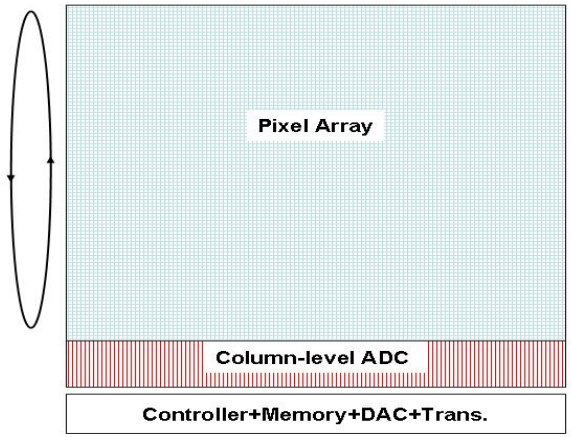
- *Sensor power consumption*
  - ✳ Present power consumption (based on existing sensors)
  - ✳ Evolution expected from final sensor fabrication technology
- *Sensor power pulsing*
  - ✳ Average power expected (not yet measured)

▷ *Caveates*

- —○ power estimates valid for ILC-500 only (3D sensors not discussed here)
- —○ power pulsing will be studied/assessed in AIDA

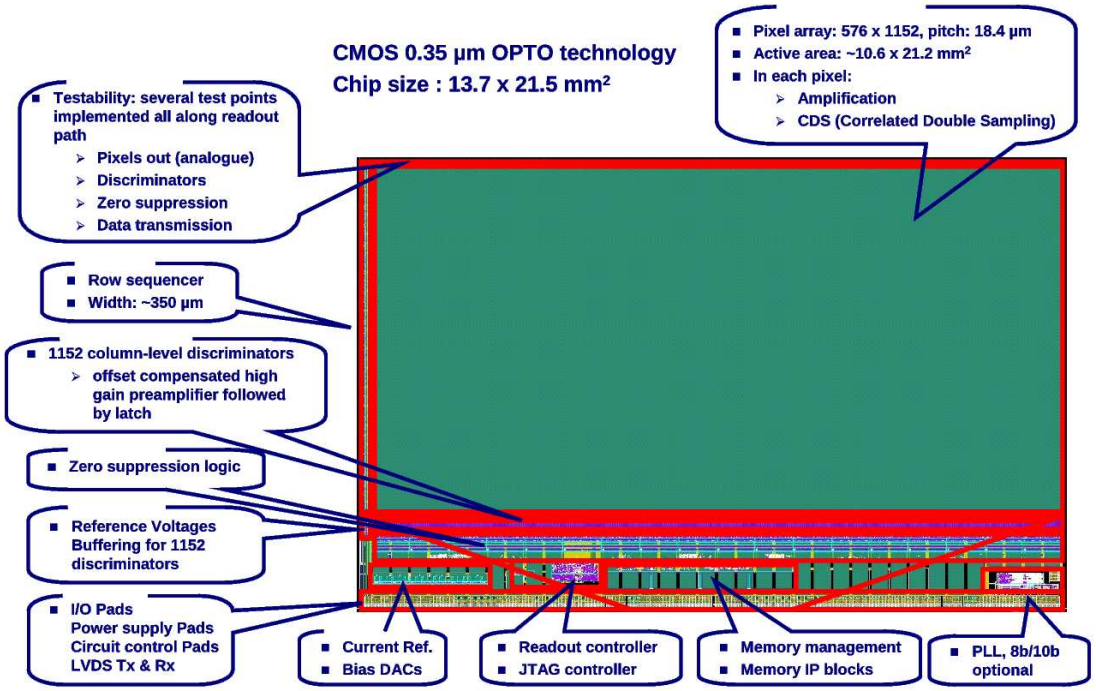
Overview of Sensor Organisation

- **Sensor organisation :**
  - ⁂ functionnalities inside each pixel :
    - ○ conversion of charge into electrical signal (e.g. voltage)
    - ○ average noise (pedestal) subtraction
  - ⁂ signal discrimination (in perspective of zero-suppression)
  - ⁂ discriminator output encoding (sparsification with charge encoding
  - ⁂ data transmission logic ⟼ connection with the outside world

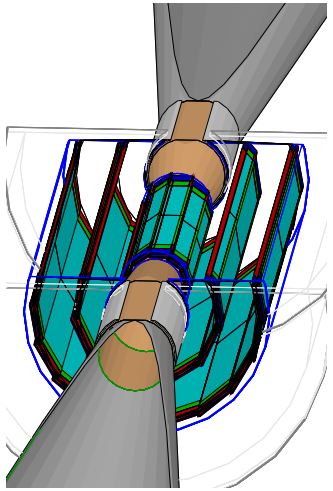


- **Specific aspects :**
  - ⁂ permanent/continuous signal sensing
    - ⇛ no dead time
  - ⁂ read-out in rolling shutter mode
    - (pixels grouped in columns read out in //)
    - ⇛ read-out restricted to 1 raw at a time
    - ⇛ power (pixel array) = power of 1 raw !!!

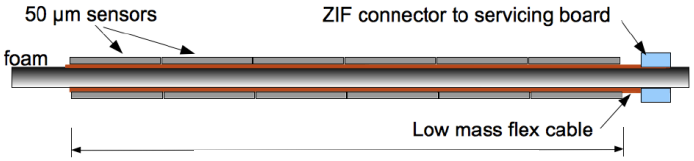
⟜ ILD-VTX pixels ≤ 83 times smaller than ATLAS HPS ...



CMOS sensors for the ILD-VTX



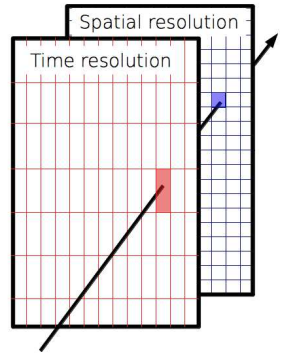
- **Two types of sensors :**
  - ⁂ Inner layers ($\lesssim$ 300 cm^2) : priority to read-out speed & spatial resolution
    - ↪ small pixels (16×16 / 80 μm^2) with binary charge encoding
      - ↪ $t_{r.o.} \sim$ 50 / 10 μs; $\sigma_{sp} \lesssim$ 3 / 5 μm
  - ⁂ Outer layers ($\sim$ 3000 cm^2) : priority to power consumption and good resolution
    - ↪ large pixels (35×35 μm^2) with 3-4 bits charge encoding
      - ↪ $t_{r.o.} \sim$ 100 μs; $\sigma_{sp} \lesssim$ 4 μm



- **2-sided ladder concept** (see J.Baudot's talk) **:**
  - ⁂ R&D of PLUME collaboration (DESY-Oxford-Bristol-IPHC-FNAL)

    (**P**ixelated **L**adder using **Ul**tra-light **M**aterial **E**mbedding)
    - ↪ material budget $\lesssim$ 0.3 % X_0 (goal)
  - ⁂ square pixels (16×16 μm^2) on internal ladder face (σ_{sp})

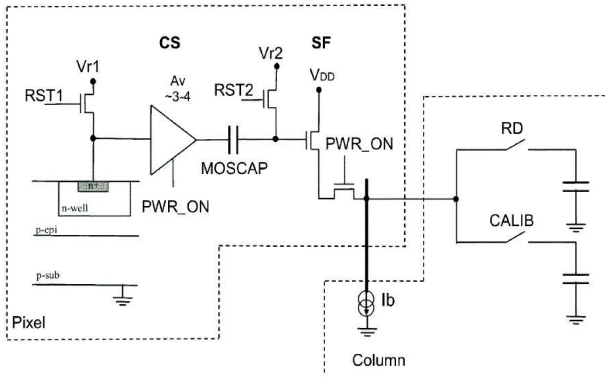
    & elongated pixels (16×80 μm^2) on external ladder face ($t_{r.o.}$)
    - ↪ $\sigma_{sp} \lesssim$ 3 μm & $t_{r.o.} \sim$ 10 μs



Pixel Array of ILD-VTX Sensor

- **Main sensing and read-out micro-circuit elements :**
  - ⁂ charge collection on sensing diode
  - ⁂ sensed charge conversion into signal (voltage)
  - ⁂ pre-amplification
  - ⁂ average noise (pedestal) subtraction (clamping)

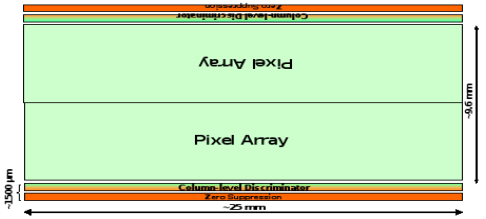
    ▷▷▷ single pixel consumption $\simeq$ 0.2 mW (3.3 V)

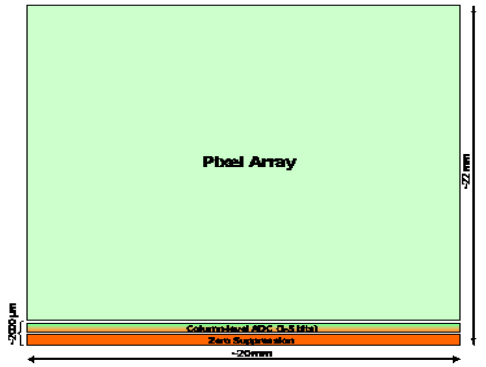


- **Power consumption of pixel array** (0.35 μm process) **:**
  - ⁂ **inner layers :**
    - ○ $\sim$ 1300 columns of 16 μm wide pixels
    - ○ two-sided read-out $\Rightarrow$ 2600 columns/sensor

      ▷▷▷ $\sim$ 520 mW/sensor
  - ⁂ **outer layers :**
    - ○ $\sim$ 600 columns of 35 μm wide pixels
    - ○ single-sided read-out $\Rightarrow$ 600 columns/sensor

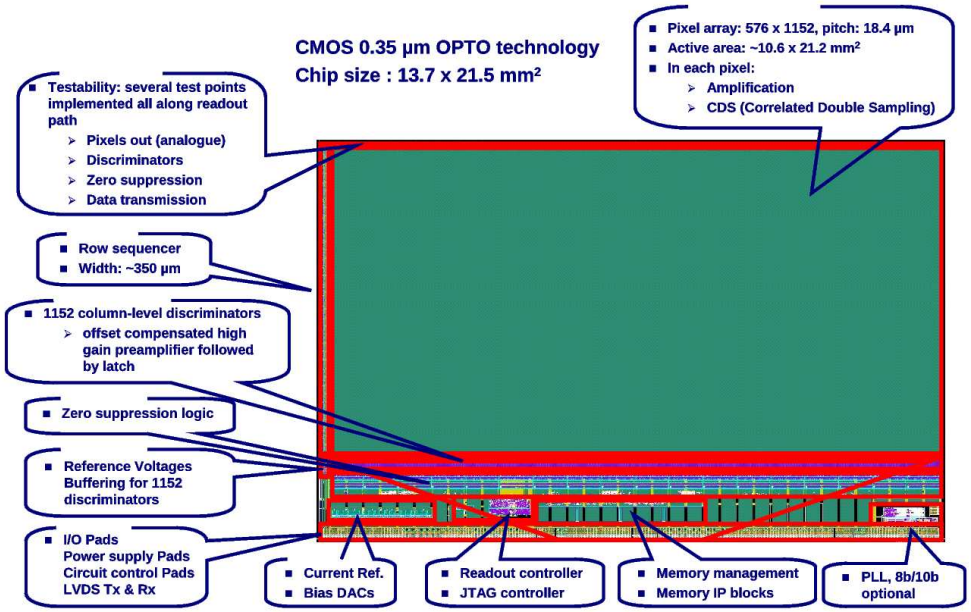
      ▷▷▷ $\sim$ 120 mW/sensor





Peripheral Circuitry of ILD-VTX Sensor

- **Main peripheral circuitry elements :**
  - ⁂ discriminators / ADCs : 300 / 500 μW/col.
  - ⁂ bias DACs (discri. & ADC thresholds, V_{ref}, etc.) : O(1) mW/DAC
  - ⁂ digital circuitry (zero-supp., sequencers, etc.) : $\sim$ 150 μW/col.
  - ⁂ memories (output buffers) : O(1) mW/Mbps
  - ⁂ signal transmission (LVDS) : O(10) mW/channel



- **Power consumption of peripheral circuitry** (0.35 μm process) **:**
  - ⁂ discriminators / ADCs : 800 / 300 mW (in/out)
  - ⁂ bias DACs (discri. & ADC thresholds, V_{ref}, etc.) : 50 / 20 mW (in/out)
  - ⁂ digital circuitry (zero-suppression, sequencers, etc.) : 400 / 100 mW (in/out)
  - ⁂ memories (output buffers) : 200 / 50 mW (in/out)
  - ⁂ signal transmission (LVDS) : 200 / 50 mW (in/out)
    - ▷▷▷ **inner layers :** $\sim$ 1650 mW/sensor
    - ▷▷▷ **outer layers :** $\sim$ 500 mW/sensor

Instantaneous Power Consumption of Full ILD-VTX

- **Sensor and ladder total power consumption** (0.35 μm process) **:**
  - ⁂ **inner layer** ($\sim$ 2 cm^2)**:**
    - sensor : $\sim$ 500 (pixels) + 1700 (periphery) $\simeq$ 2200 mW/sensor
    - ladder : $\sim 12 \times 2200$ mW $\simeq$ 26 W/ladder
  - ⁂ **outer layers** ($\sim$ 4 cm^2)**:**
    - sensor : $\sim$ 100 (pixels) + 500 (periphery) $\simeq$ 600 mW/sensor
    - ladder : $\sim 12 \times 600$ mW $\simeq$ 7 W/ladder
- **ILD-VTX total power consumption** (0.35 μm process) **:**

Double-layer	**R$_{in}$/R$_{out}$**	**N$_{lad}$**	**N$_{sens}$**	**P$_{diss}$**
DL-1	16/18 mm	14	168	$\sim$ **400 W**
DL-2	37/39 mm	26	312	$\sim$ **200 W**
DL-3	58/60 mm	40	480	$\sim$ **300 W**
TOTAL		80	960	$\lesssim$ **900 W**

- **Caveates :**
  - ⁂ values based on existing sensor design not yet optimised for power consumption
  - ⁂ values based on 0.35 μm process : final sensor will be fabricated in $\leq$ 0.18 μm technology
  - ⁂ increase of leakage current consecutive to irradiation not accounted for

Effect of Smaller Feature Size

- **Evolve towards feature size $<<$ 0.35 μm :**
  - ⁂ μcircuits: smaller transistors, more Metal Layers, capacitors, ...
  - ⁂ **sensing:** 3-well, depleted sensitive volume, ...
- **Benefits :**
  - ⁂ higher μcircuit density ⇛ higher data reduction capability
  - ⁂ thinner gates, depletion ⇛ improved radiation tolerance
  - ⁂ large number of ML ⇛ reduced surface of peripheral circuitry, etc.
  - ⁂ faster read-out or lower power ⇛ chose between speed and power ▷▷▷

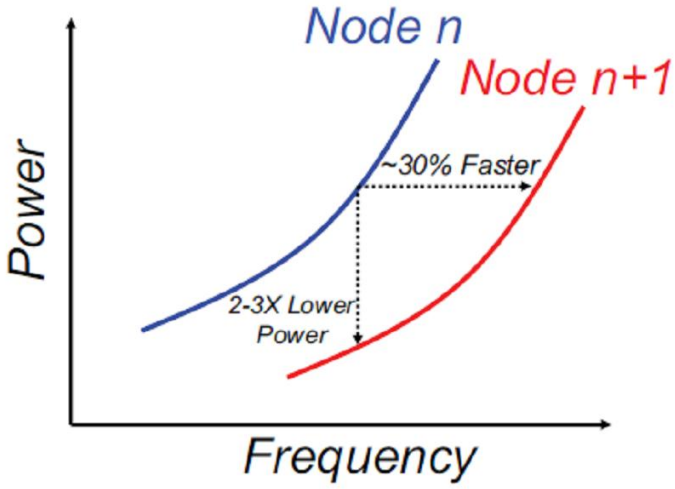


Fig. 2. Historical value of scaling: Moving to node (n=1) from node (n), and operating at lower voltage, one could obtain faster and/or at lower power.

- **Power consumption : ex. of 0.18 μm process** (n ⟼ n+2)
  - ⁂ lower voltage (1.8 V instead of 3.3 V) ⇛ power ↘
  - ⁂ exploit higher signal propagation frequency (memories) ⇛ power ↗
  - ⁂ **digital** circuitry ▷ general (approximate) rule : $P = \alpha \cdot C \cdot V^2 \cdot f + I_{leak} \cdot V + \beta \cdot I_{sc} \cdot V$

    C $\sim$ feat.size^2 ⇛ $P \sim S^2_{feature} \cdot V^2 \cdot f + ... \Rightarrow P^{0.18}_{digi} \simeq 0.1 \cdot P^{0.35}_{digi}$ at fixed frequency
  - ⁂ **analog** circuitry (pixel array, discri., ADC) ▷ power reduction more complicated to assess but $<<$ P_{digi} reduction

⇛ **Total sensor dissipation :** $\sim$ 1600 mW/sensor(in) & $\sim$ 500 mW/sensor(out) (0.35μm values: 2200 & 600 mW)

⇛ **Total Instantaneous VTX Power :** $\lesssim$ **700 W** (0.35μm value: 900 W)

▷▷▷ **Caveate :** I_{leak} increase between 0.35μm and 0.18μm not accounted for

Power Reduction from Power Pulsing

- **Exploiting ILC beam time structure** :
  - beam duty cycle $\sim$ 1/200
  - ILD-VTX duty cycle needs to account for stable functionning of $\sim$ 1,000 sensors
    $\equiv$ 400 Mpixels with $\sim$ 10 T, $4{\cdot}10^5$ discri. & $5{\cdot}10^5$ ADC, $2{\cdot}10^4$ DAC
    $\Rightarrow$ estimated duty cycle in the range 1/50 - 1/100 ($\equiv$ sensors dissipate during 4 ms to 2 ms)

- **Power pulsing** :
  - Pixels : all switched off inbetween trains $\Rightarrow$ 0 W
  - Peripheral circuitry :
    - all elements switched off inbetween trains except of discri. & ADC and bias DAC (tbc) $\Rightarrow$ 0 W
    - discri. & ADC (tbc): $\sim$ 1 % of nominal dissipation
    - bias DAC on stand-by (needs optimisation) : 25 / 10 mW (in / out)
  - **Average VTX power dissipation** (for 2 and 4 ms active time around train) :
    - **switchable components :** 9 - 18 W
    - **discri. & ADC :** $\sim$ 5 W
    - **DAC :** $\sim$ 12 W (conservative)

    $\triangleright\triangleright\triangleright$ **Average power dissipated by full ILD-VTX $\sim$ 20-30 W**

SUMMARY – CONCLUSION

- **Power consumption of ILD-VTX based on CMOS sensors equipping double-layer geometry estimate** :
  - based on existing CMOS (EUDET & STAR) sensors fabricated in 0.35 μm technology
  - optimising sensor architecture for $\sim$ 10 μs time stamp in inner layer $\Rrightarrow$ 150 W overload
  - accounting for reduction expected from translation to 0.18 μm

  $\Rrightarrow$ **Total power consumption $\lesssim$ 700 W**

- **Power pulsing** :
  - Assumptions :
    - full power dissipation during 2 ms – 4 ms
    - all components can be switched off inbetween trains except - potentially - DAC, discri. & ADC
    - DAC, discri. & ADC can at least be put in stand-by
  - **Average VTX power dissipation** (0.18 μm techno.) :
    - **switchable components:** $\lesssim$ 15 W
    - **DAC:** $\sim$ 10 W (conservative assumption)
    - **discri. & ADC:** $\lesssim$ 5 W

  $\Rrightarrow$ **Average power dissipated by full ILD-VTX $\sim$ 20–30 W**

- **Power per surface unit** (normalised to active unit) :
  - during trains : $\sim$ 800/100 mW/cm^2 in inner/outer layers
  - inbetween trains : $\sim$ 15/3 mW/cm^2 in inner/outer layers (conservative assumption)

  $\Rrightarrow$ **Air flow seems sufficient to extract all power dissipated (tbc)**