

Status of firmware DCC & LDA

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DCC

- Firmware is currently stable
- We have 19 cards available
- Main work since few weeks : Try to send a correct busy signal

I have made a test where a trigger is sent by the CCC card to the DIF via the LDA and DCC. The DIF identifies the trigger and sends a busy signal. There are 2 methods : either a level is sent, either a clock is sent. Matt Warren has implemented a clock detection in the LDA for the busy line (next slide figure)

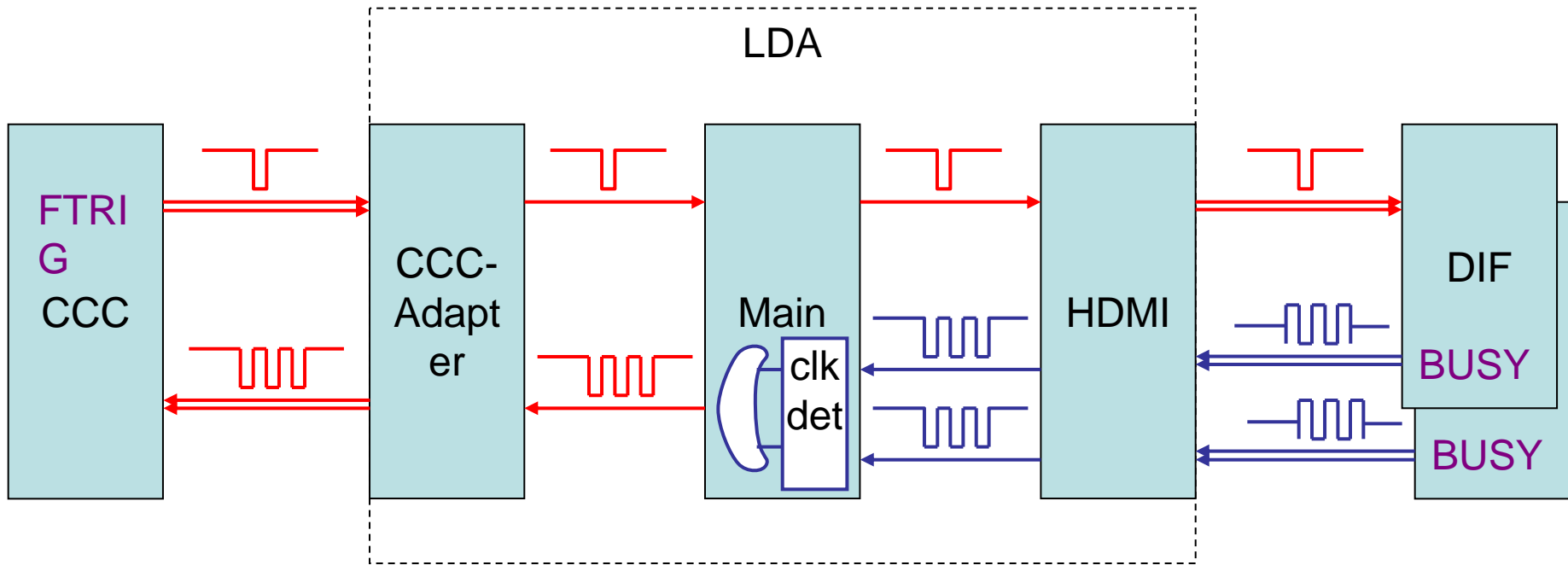
The Busy detection on DCC is a “or logic”.

The clock sent by the DIF is the slow-clock : 2.5 MHz

We have observed a distortion on signal due to the AC-coupling (I suppose)

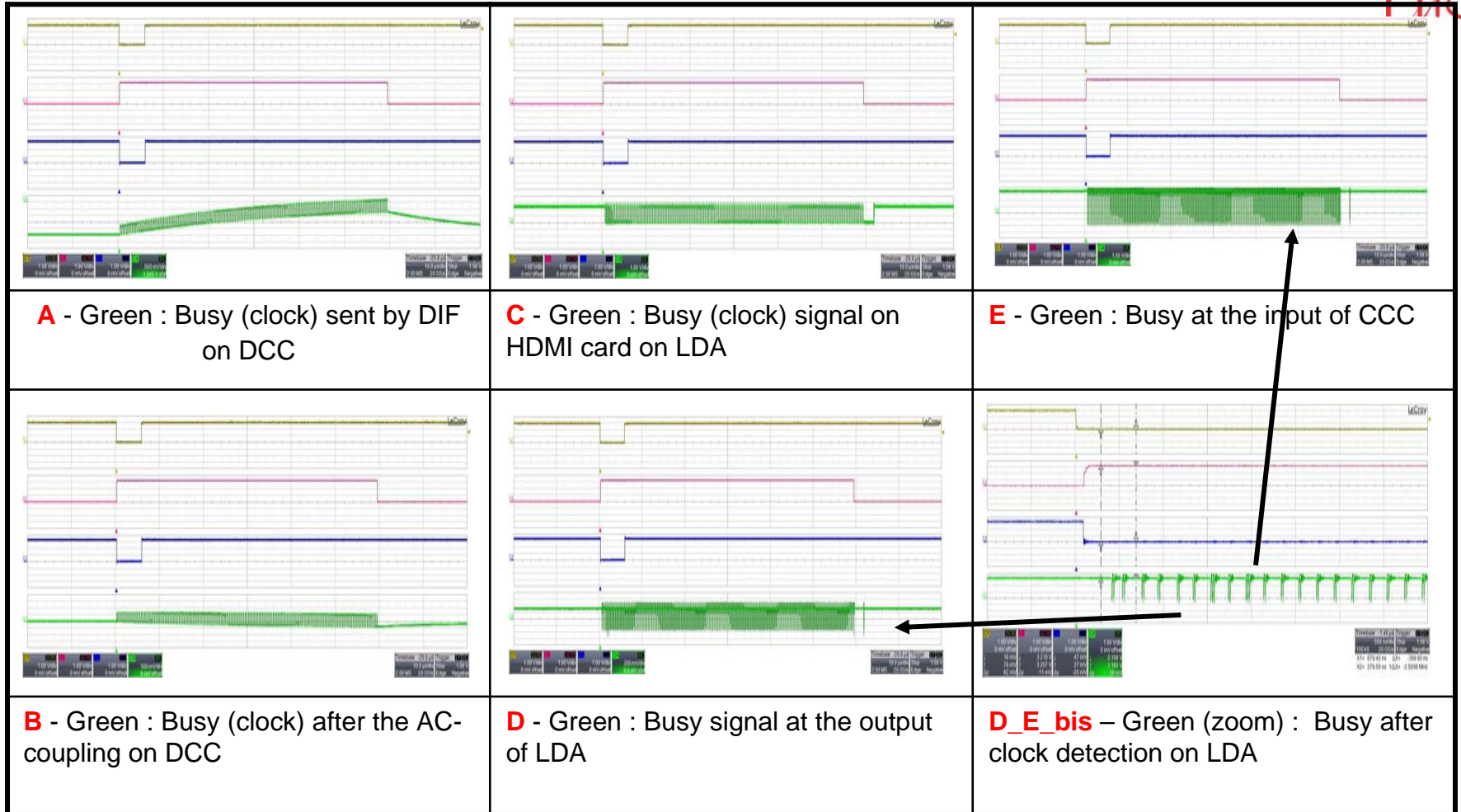
At the output of LDA, the clock detection has shown a noisy signal. We must check if this signal is correctly decoded by the CCC for the busy.

Trig, busy diagram (from UK)



Busy : scope capture

11A



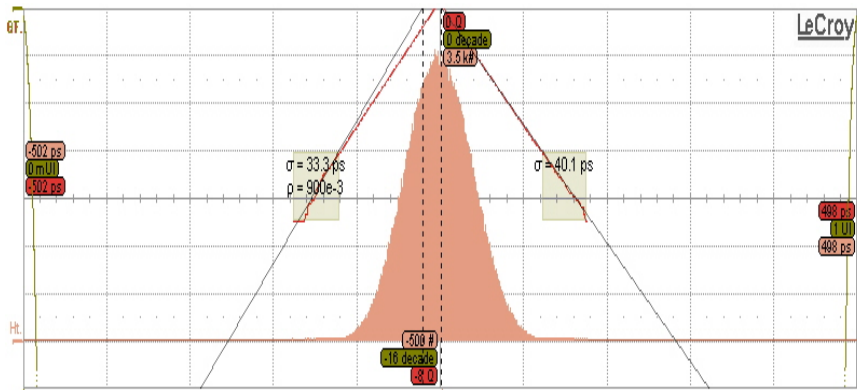
LDA

- We have succeeded to send and to receive data on DIF via DCC with this configuration :
 - 1 LDA
 - 5 DCC
 - 3 DIF/DCC

- The first test has shown a data rate to the PC around 12 Mo. I have looked at the source code and I added a buffer (FIFO) before the GBethernet XILINX IP and we have won 10 Mo, the data rate is now around 22 Mo. But we need to make several tests with more DCC and DIF connected in order to validate the stability of this firmware change.

Jitter measurement

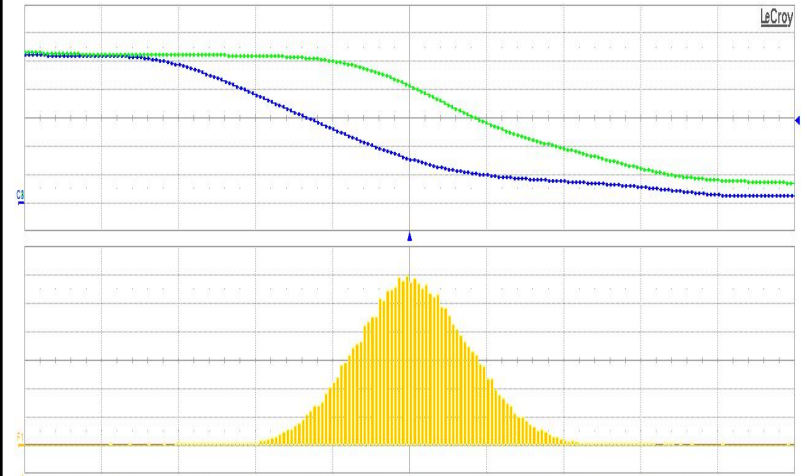
Setup : CCC – LDA – DCC -DIF



Measure	P1:(T)	P2:(EffeR)	P3:(EffeD)	P4:...	P5:...	P6:...	P7:...	P8:...
value	545.0 ps	35.4 ps	53.3 ps					
status	✓	✓	✓					

gFit	BTub	Ht1e
1.00 Q/div	2.00 decades	500 #/div
100 ps/div	100 mV/div	100 ps/div
306.000 k#	306.000 k#	306.000 k#

Timebase	Trigger
0.0 μs	Auto
1.00 MS	Edge
	319 mV
	Positive



Measure	P1:range(F1)	P2:hsdev(F1)	P3:hmas(F1)	P4:ddelay(C3...	P5:...	P6:...	P7:...	P8:...	P9:...	P10:...	P11:...	P12:...
value	88.0 ps	> 7.6 ps	213.9 ps	194 ps								
status	↑	↑	↑	✓								

Timebase	Trigger
0 ps	Normal
100 ps/div	584 mV
20.0 S	20 GS/s
	Edge
	Negative

Clock (50 MHz) jitter at the input of DHCAL DIF
TJ ~ 545 ps

Delay between trigger on 2 DIFs, the delay is around 200 ps, must be confirmed with other test and more DIF connected to a DCC

Conclusion

- DCC firmware is stable
 - See with the trigger and busy tests if we add a modification
- LDA firmware is currently in a correct state for the intensive tests (need to connect with more than 5 DCC)

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- *Trigger and busy must be checked with the CCC and a system that manage these signals*
- *For the data rate, an ODR card may be better than a network card*

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For these 2 items, we don't have the time to make it in a short deadline.