# Silicon Tracking Status

Goals of the SiLC (Silicon Tracking for Linear Collider) collaboration

- Optimisation studies of the geometry of the silicon trackers
- Access to different sensors and electronics technology
- Develop a tool to facilitate the optimisation studies
- Provide drivers for ILD concept and CLIC detectors

Main ideas

- Generate different kind of geometry very easily (number of silicon layers, false/true double-sided, technology …) → dynamic aspect
- Possibility to introduce mis-alignment studies according a mechanical structure
- Materiel budget effects induce by the supports and the cabling
- Could be used in different framework

# Silicon Tracking Status Reminder

History

- Developing a silicon tracker through ILCRoot framework (2008)
  First integration in the 4th concept
- Switch to Mokka framework (end of 2009) for a more detailed description of the ILD concept

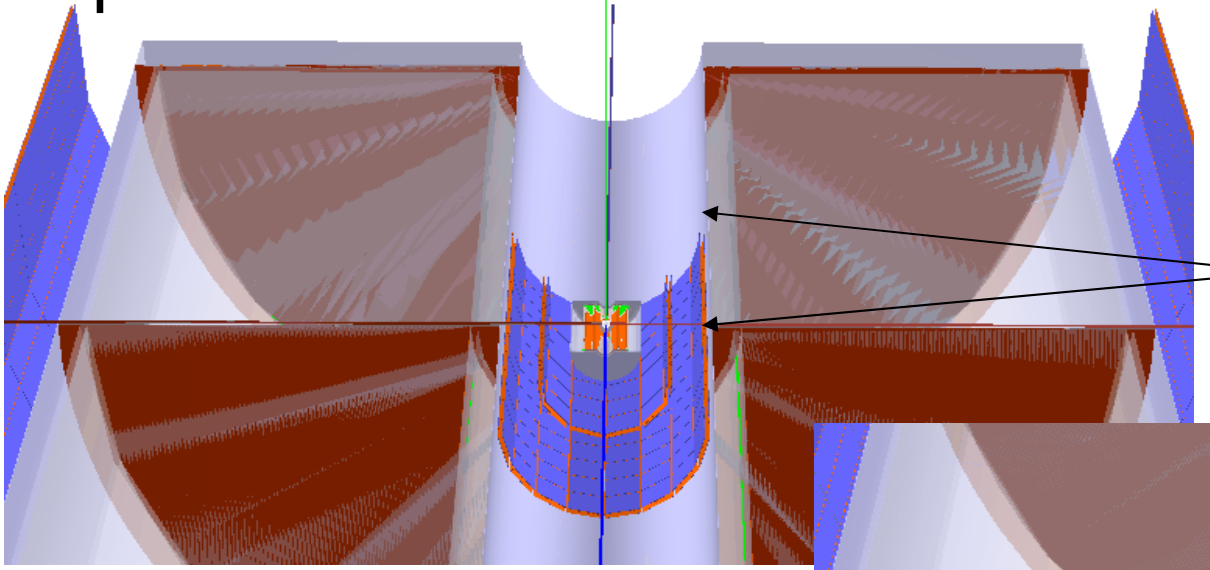
- Re-design the design pattern in 2010 (more flexibility for CLIC study):
  - Integration in different framework
  - More flexibility = fewest fixed parameters
    → creation of sub-detector families
    → sub-detectors configuration
    → cross setup
  - Different input

Availlable for ILD_01 release
Actually in MOKKA trunk version

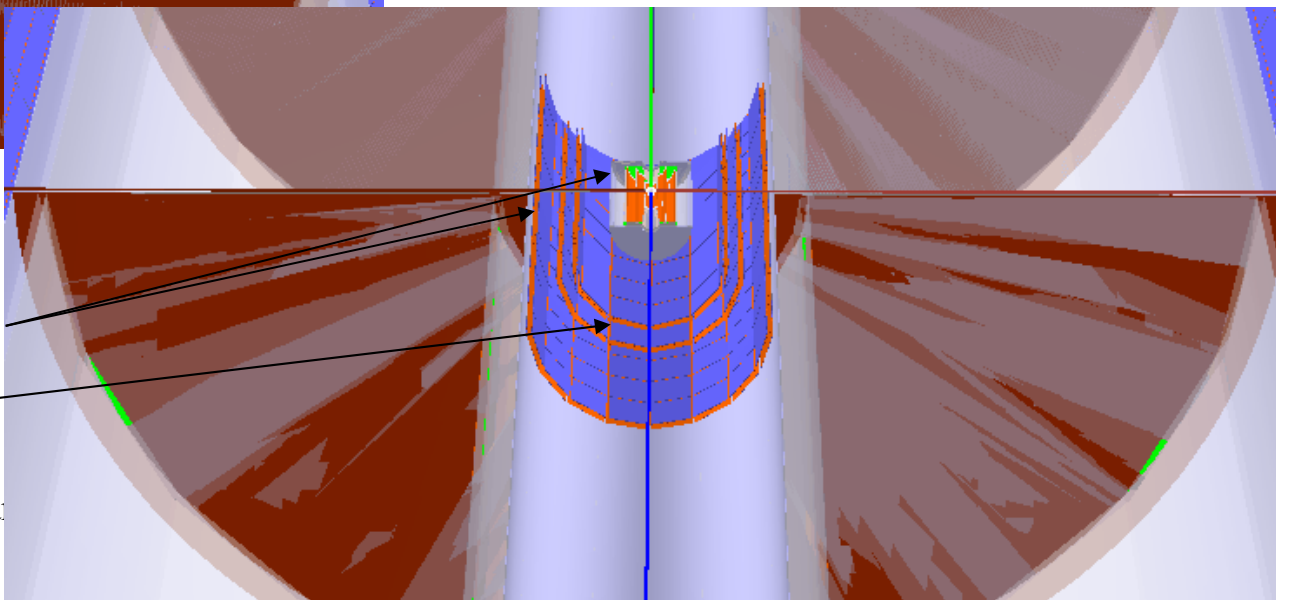
# Silicon Tracking Status

## Easy customisation

Modification of the number of silicon barrels in the internal part of ILD → same code with different database input



SIT (baseline):
2 double « false double » layers

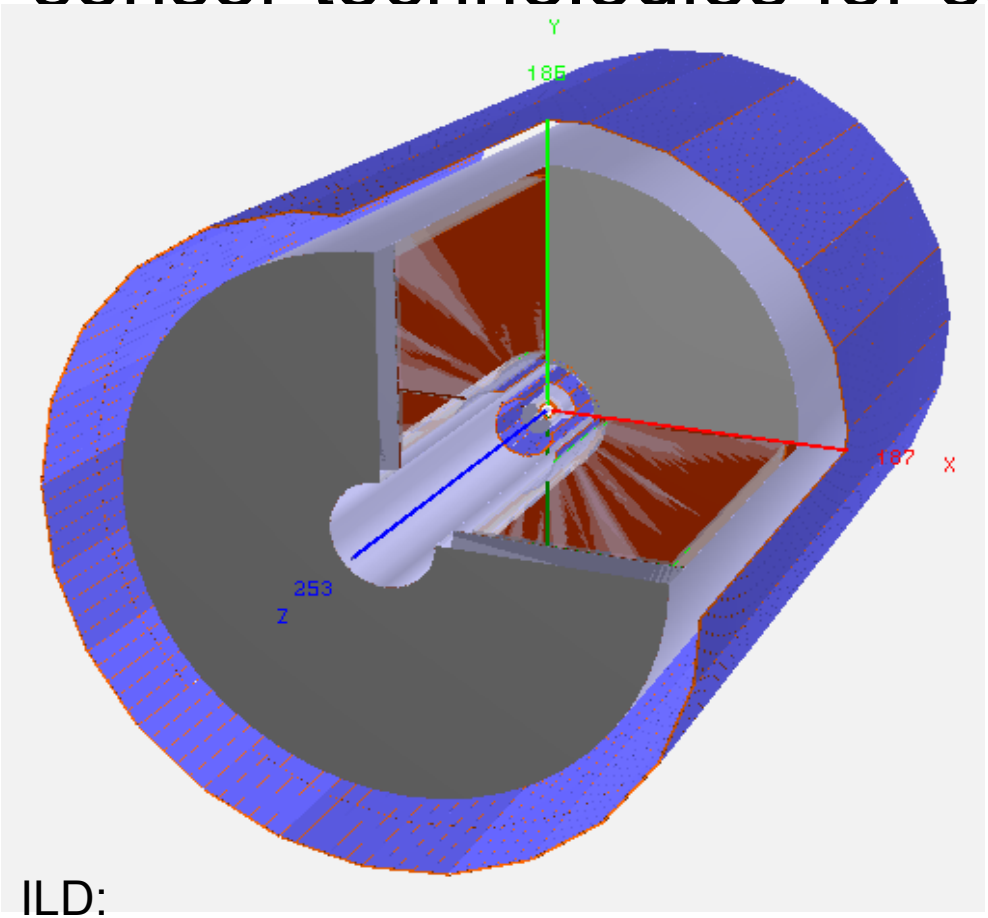


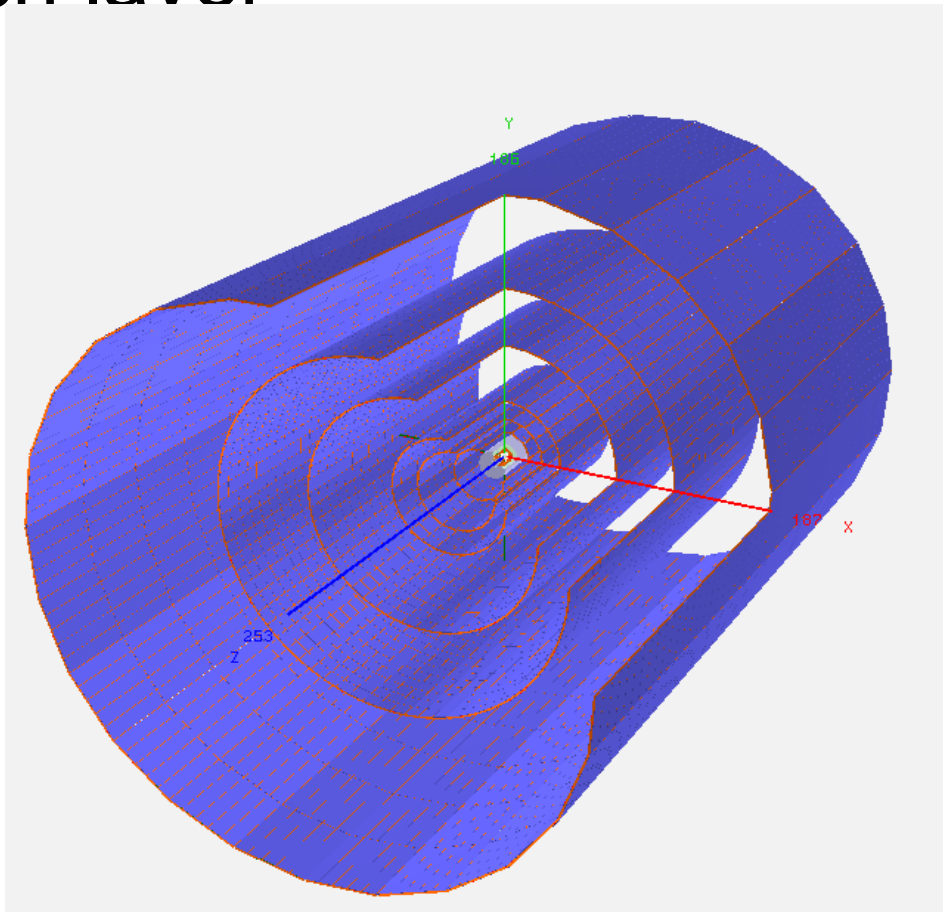
SIT (alternative concept ):
2 double « false double » layers
+1 single or double layer

# Silicon Tracking System

## Not only ILD – CLIC studies

Full Silicon tracker: free to choose the shape and the sensor technologies for each layer



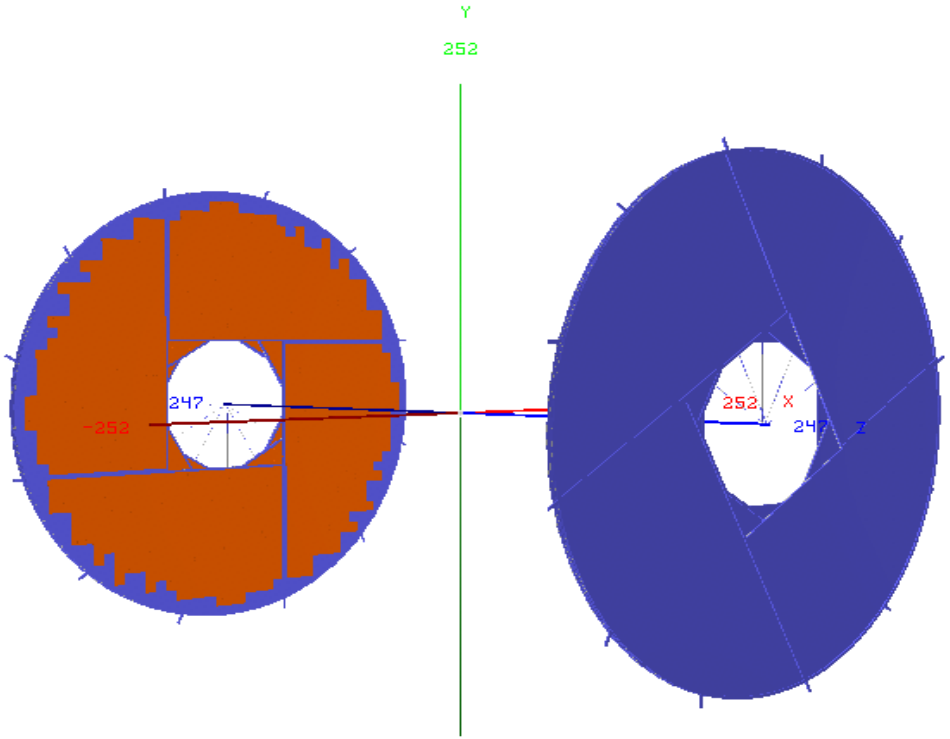



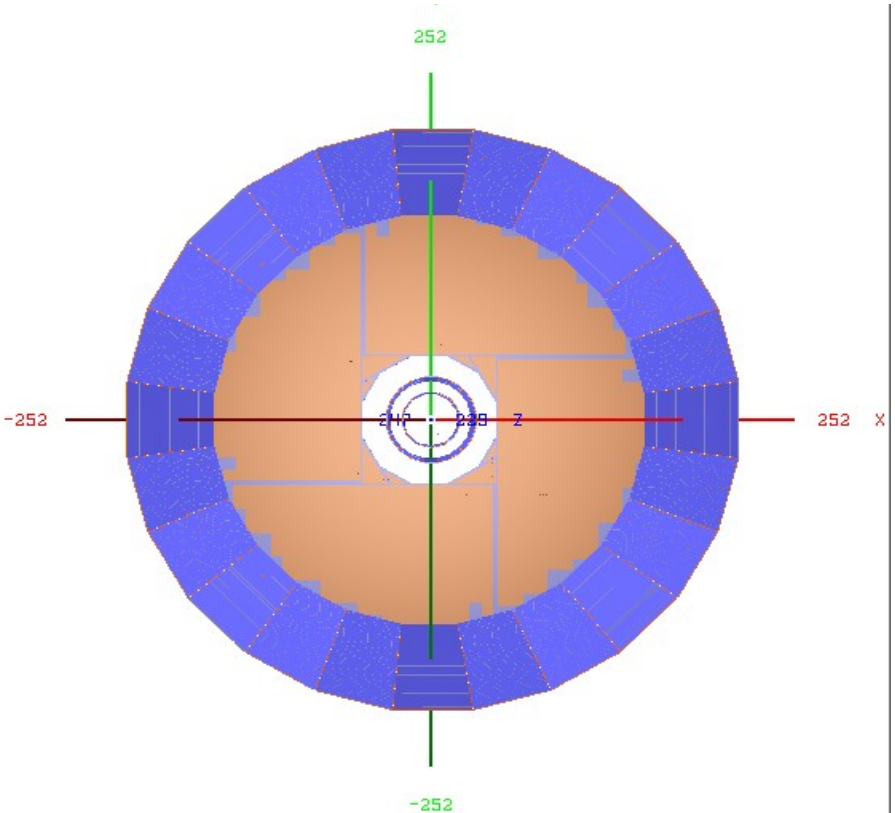

ILD:
VXD+SIT+SET+ETD+TPC

VXD+7couches silicium

# Silicon Tracking System
# ILD-ETD

- Geant 4 description:
  - Using the edgeless properties
  - XUV solution: pixels at small angle have to be implemented (XY alternative solution is available)
  - Gaps: 50 micron gap between modules, super module, Gap between detection Element → dead zone



# Silicon Tracking Status

- Geometry (done, in progress, under discussion, future)

| | Barrel | | Forward | | | | Very Forward |
|---|---|---|---|---|---|---|---|
| | Single Layer | Double Layer | Single Layer | XY | XUV | Rphi | |
| Code Dev | | | | | | | |
| Functionalities | | | | | | | |
| Module Angles | | | | | | | |
| Module Overlapping | | | | | | | |
| Segmentation | | | | | | | |
| Parameter dependency/Alignment | | | | | | | |
| Debugging | | | | | | | |
| Overlapping | | | | | | | |

**ILD baseline is ready. Other baseline in progress.**

- Digitization ?
- Reconstruction ?