Electronic workshop for Si-W ECAL

16 – 17 May 2011

Ki-Hyeon Park

Pohang Accelerator Laboratory

The Pohang Light Source View

Energy : 3.0 GeV

Current : 400mA

2011-05-16

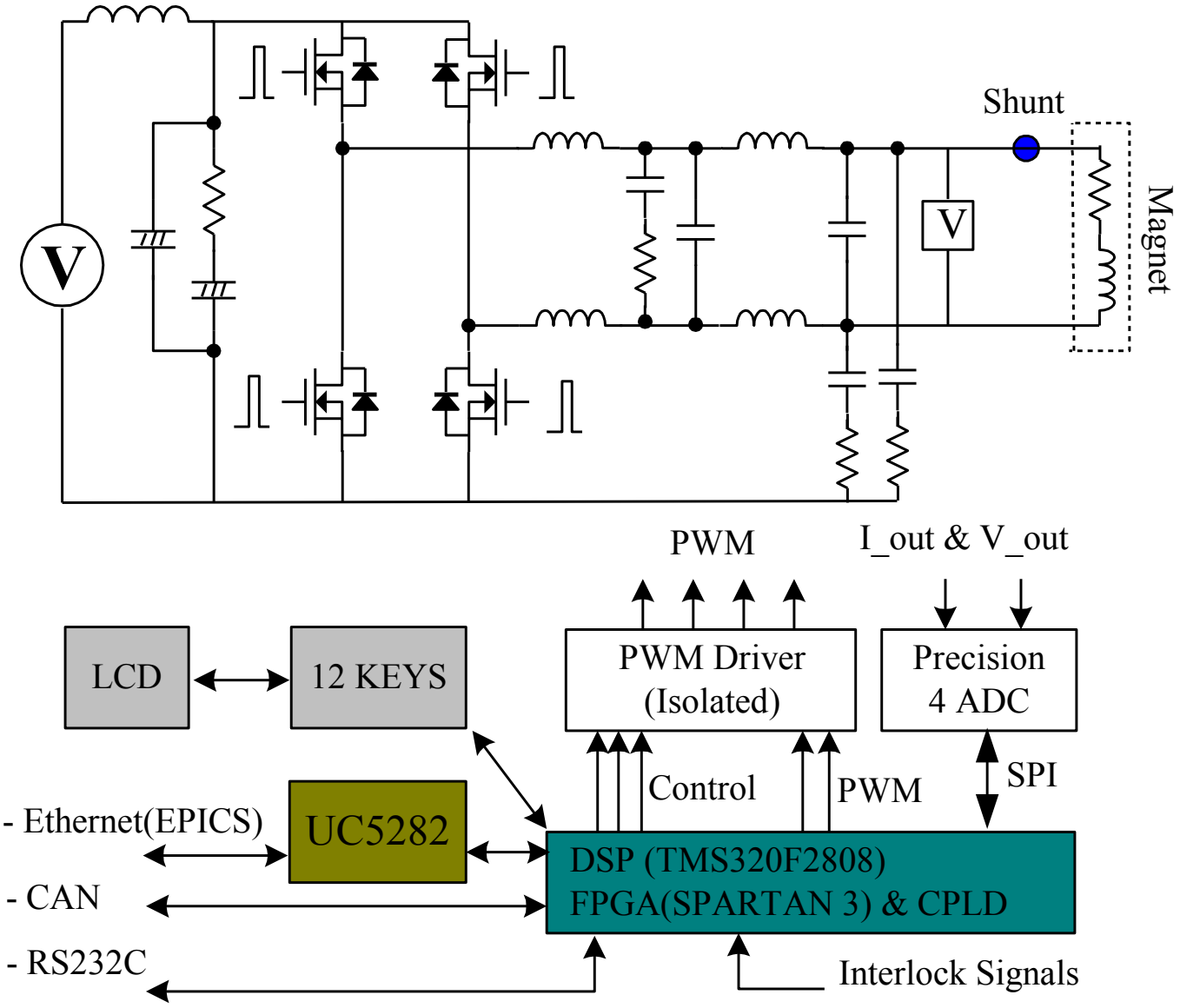
Digital Controller Design for the Magnet Power Supply

- Intput Filter
- Output Filter
- Control Loop
- Simulink Simulation
- DSP & ADC board
-5A High Stable Power Supply

Power Supply Description

► DC Regulator Voltage:	24 [V]
► DC Output Current :	±5 [A] at bipolar mode
► Output Voltage:	6 [V]
► FET Switching Frequency:	25 KHz
► FET:	4 ea (IRF540)
► ADC:	AD977A from Analog Devices
► Digital Signal Processor:	TMS320F2808 Texas Instrument
►Current Stability:	< **5** ppm

Block Diagram

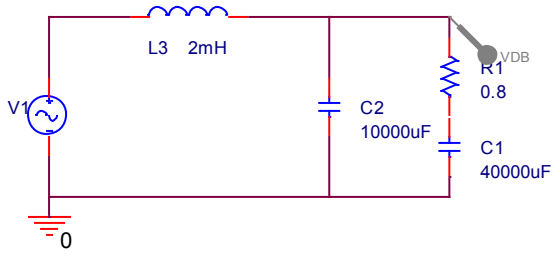


Input Filter Design

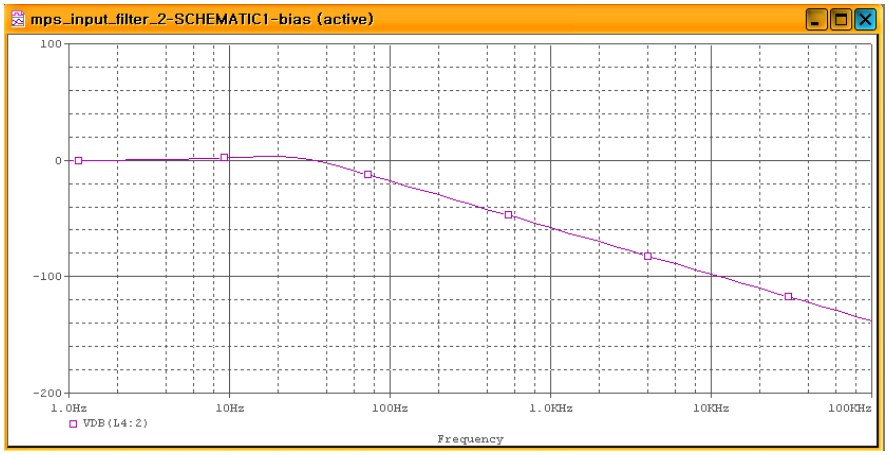
The rectified input voltage has harmonic components, thus it should be attenuated. The parallel damped filter was preferred to build the MPS

The condition of the $C_1 = 4C_2$ was chosen, because its transfer function was slightly under-damped

The cutoff frequency of the input filter should be ranged ~10Hz,

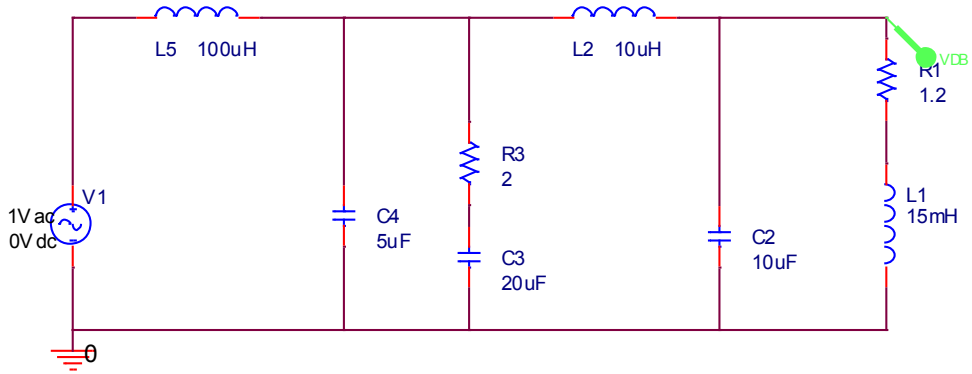


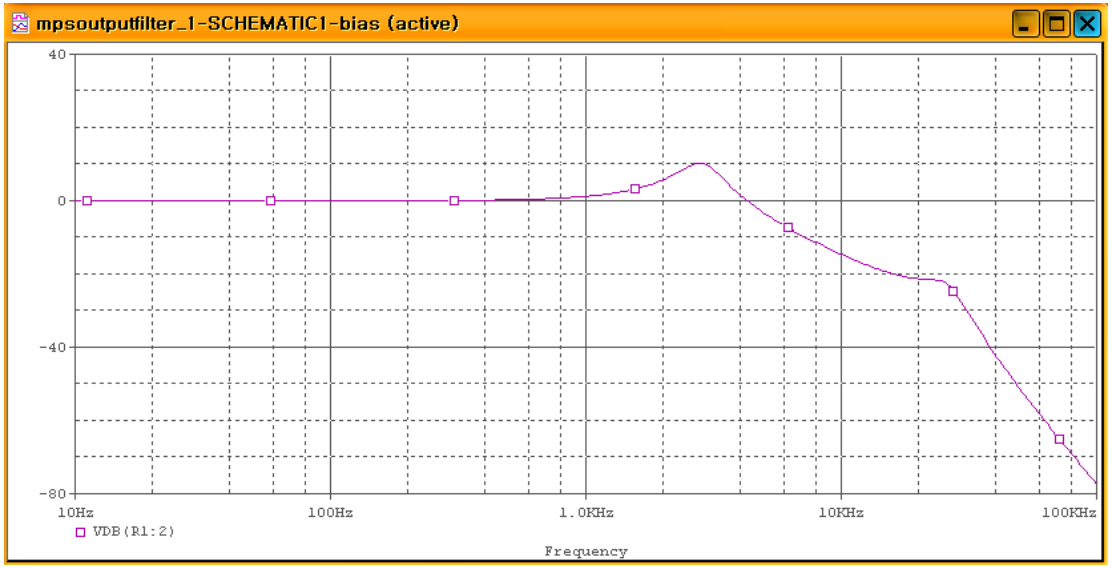
$$\frac{V_{out}}{V_{in}} = \frac{1 + sC_1R_1}{s^3L_3C_2C_1R_1 + s^2L_3R_1(C_2 + C_1) + sC_1R_1 + 1}$$



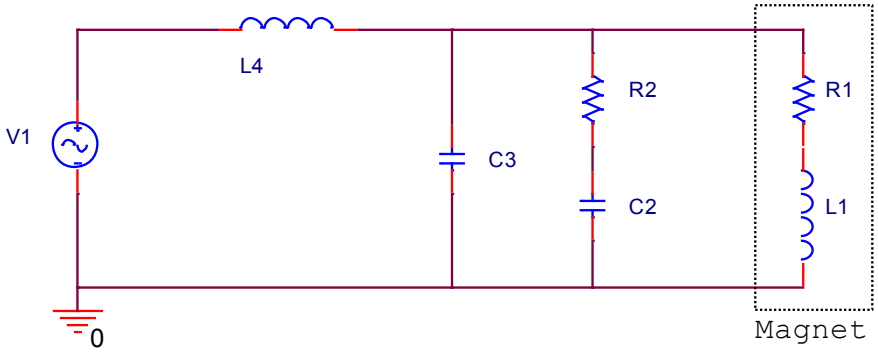
Output Filter (+Magnet Load) Design

The pole of the first filter located about ~KHz while the switching frequency is above ~10 KHz. If pole located to lower, the overall system response became worse, thus it is not good for the system dynamic responses. The second pole is placed after half of the switching frequency





Transfer function of Output Filter (+Magnet Load)

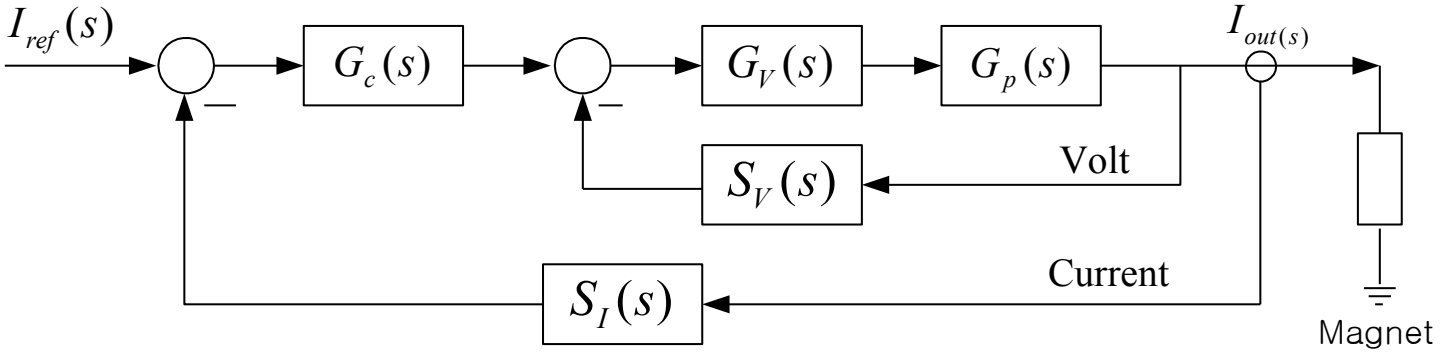


$$\frac{I_{out}}{V_{in}} = \frac{1 + sC_2R_2}{a_4s^4 + a_3s^3 + a_2s^2 + a_1s \times a_0}$$

Where

$$a_4 = L_1L_4R_1C_2C_3$$
$$a_3 = L_1L_4C_2 + L_4R_1R_2C_2C_3 + L_1L_4C_3$$
$$a_2 = C_2L_4R_2 + C_2L_4R_1 + L_4C_3R_1 + C_2R_1R_2$$
$$a_1 = R_1$$

Control Loop Equation



A conventional PI controller is $Gc(s) = \frac{Kps + Ki}{s}$

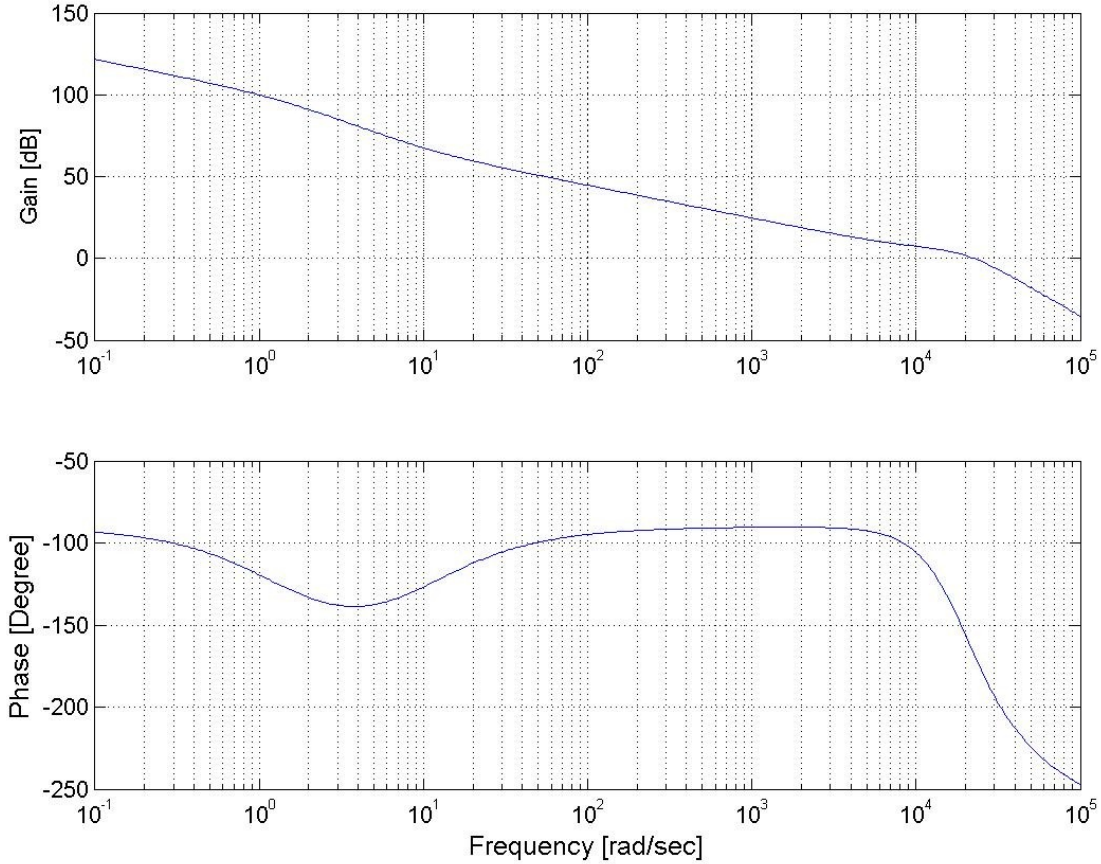
The closed-loop transfer function of the power supply is given by:

$$H(s) = \frac{I_{out}(s)}{I_{ref}(s)} = \frac{G_c(s)G_{in}(s)H_I(s)}{1 + G_c(s)G_{in}(s)H_I(s)}$$

The equivalent transfer function of the inner loop :

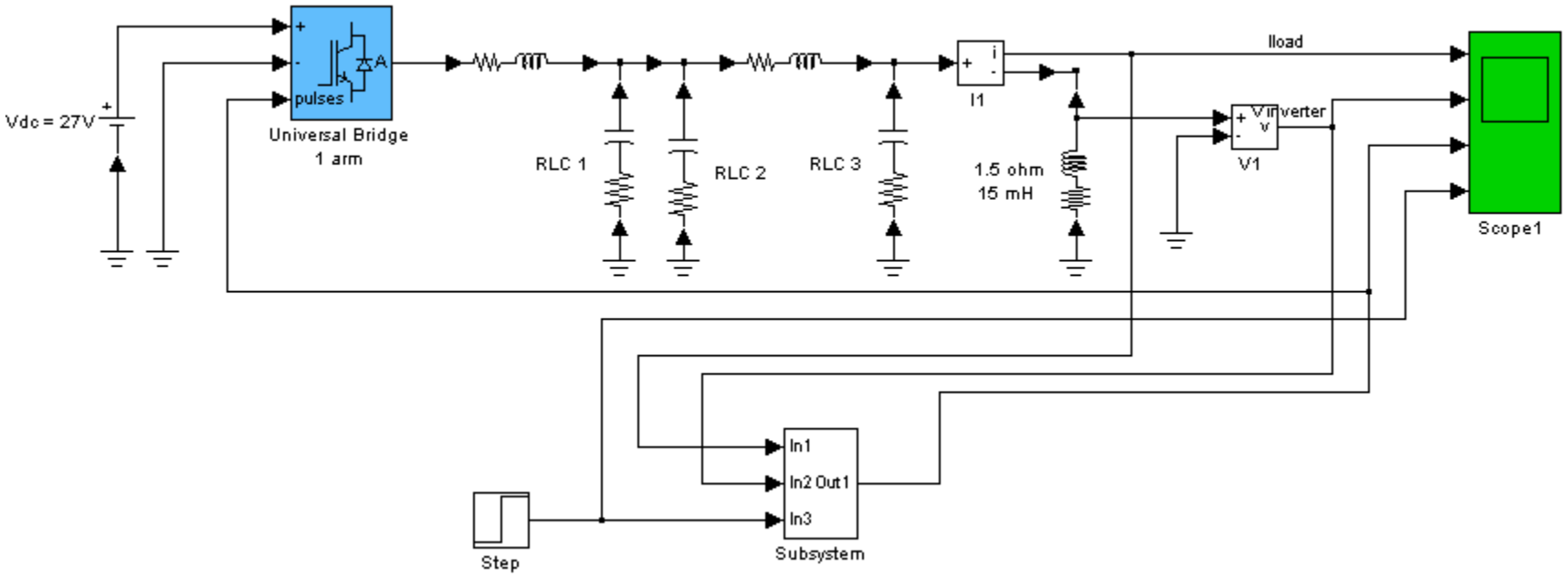
$$G_{in}(s) \equiv G_P(s)G_V(s)/(1 + G_P(s)G_V(s))$$

Open-Loop Frequency Response

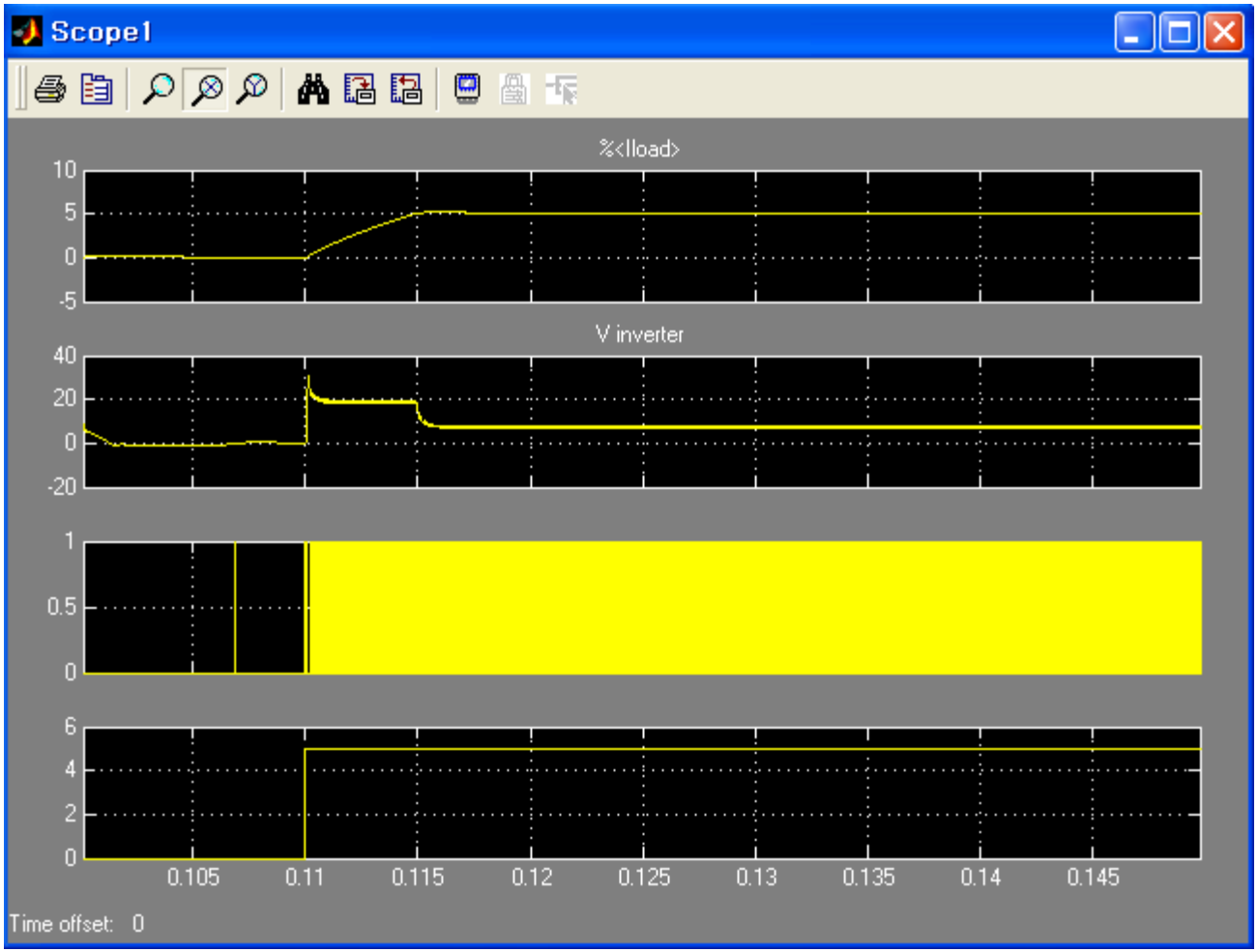


The crossover frequency is about 5KHz with small phase margin.

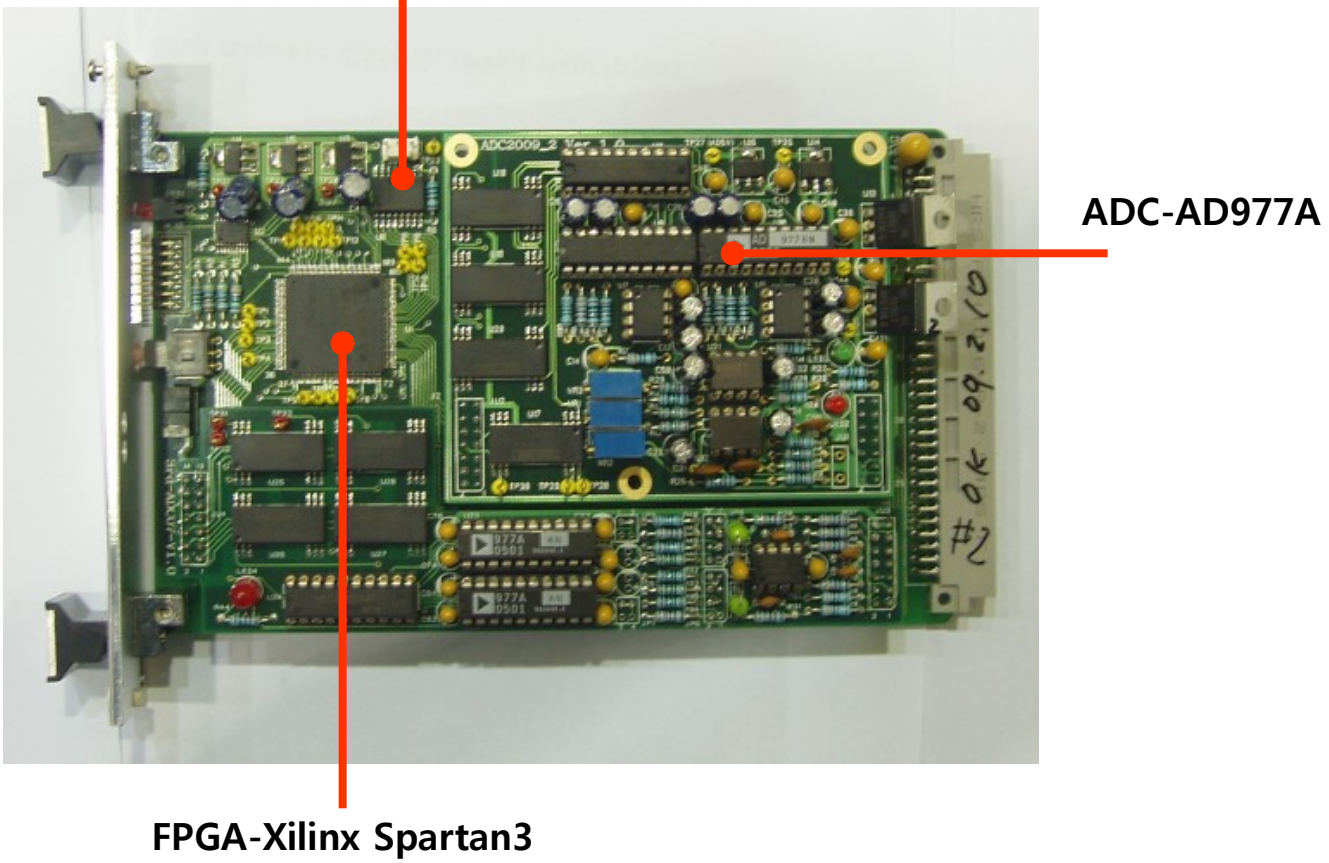
Simulink Model



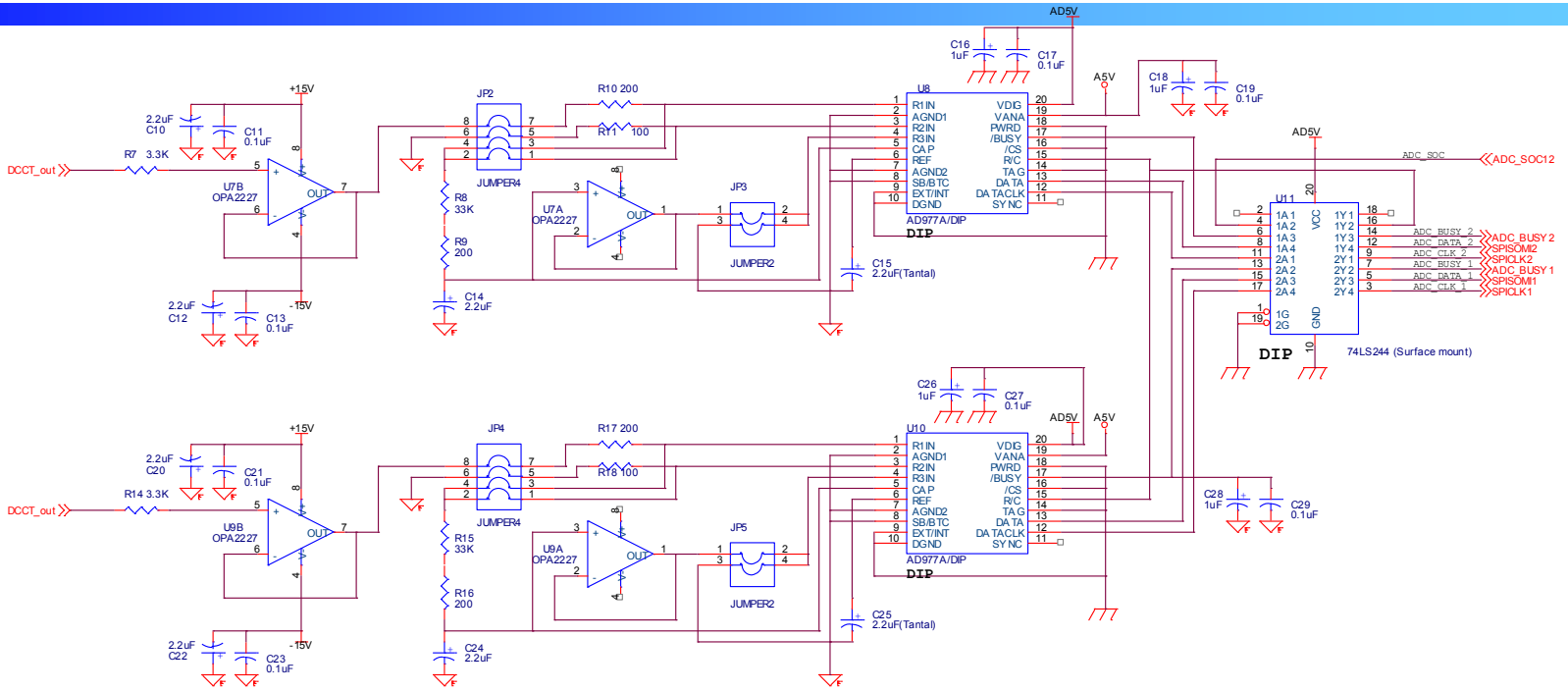
Continuous Mode Simulation



ADC Board (1)



ADC Board (2)

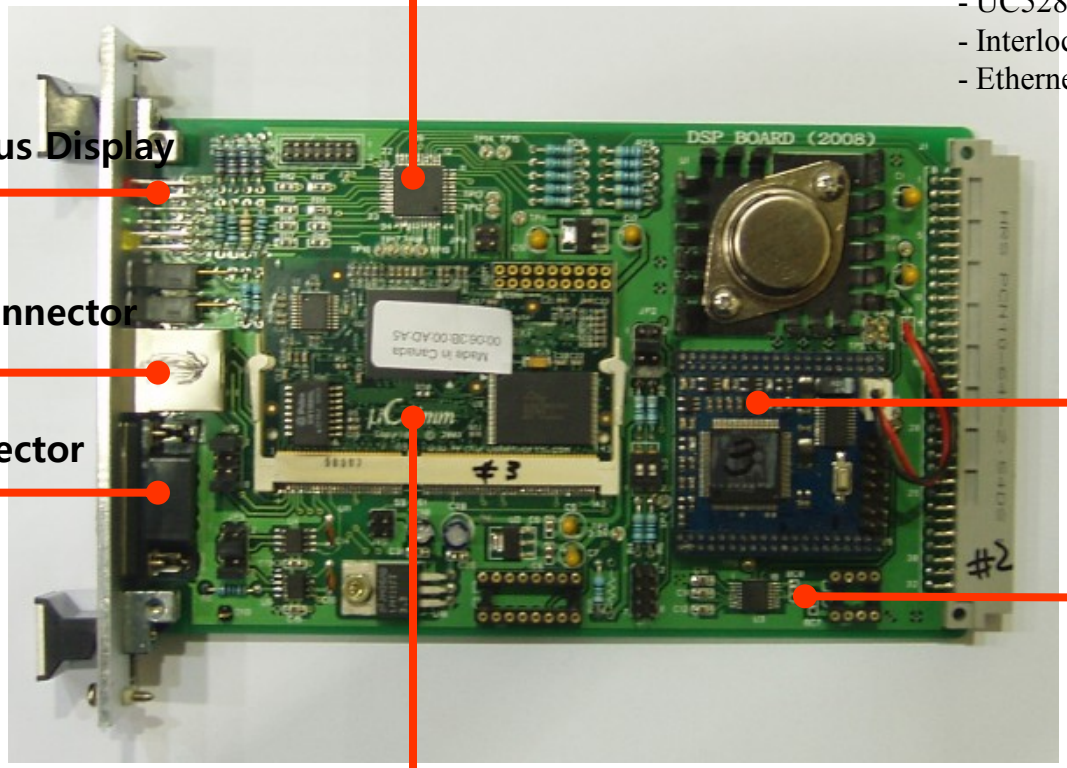


ADC board specifications

- 16 bit ADC AD977A : 4 channel
- Input Range : ±5V, ±10V, 5V, 10V
- Using the Isolated DC Power
- AD977 Linearity : ±2.0 LSB
- FPGA(Xilinx Sprtan3) : Generate control signals for ADCs
- ADC Data transmitted whenever DSP required
- DAC chip DAC714 (16-bit 200KHz) for ADC Debugging

DSP(CPU) Board

DSP board specifications :
- 100MHz Fixed point TMS320F2808 DSP
- PWM : 1a, 1b, 2a, 2b, 3a, 3b, 4a, 4b
- PWM Frequency : up to 100 KHz
- Output : 24V relay control
- UC5282 Board : Ethernet(EPICS)
- Interlock : Flexibility with the Cool-Runner FPGA
- Ethernet & CAN Connector : At front Panel



Programmable Interlock Logic

LEDs : Status Display

Ethernet Connector

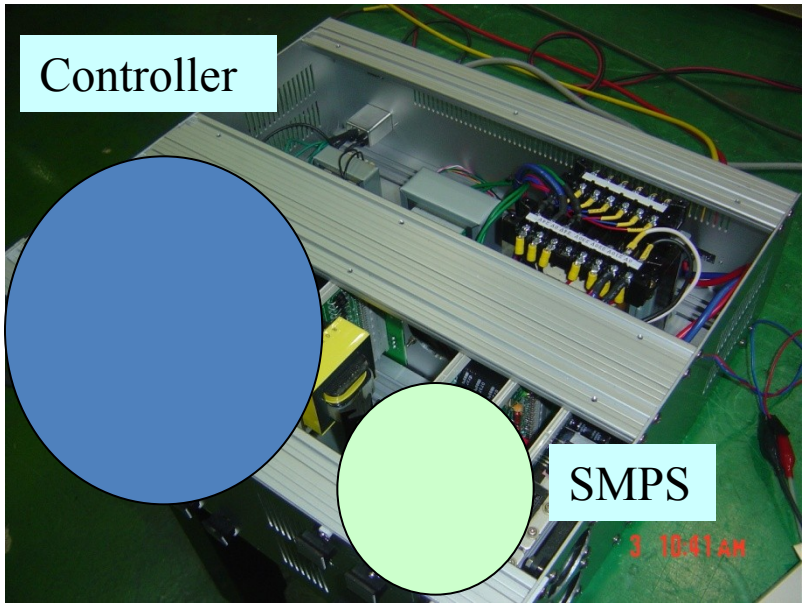
CAN Connector

DSP Board

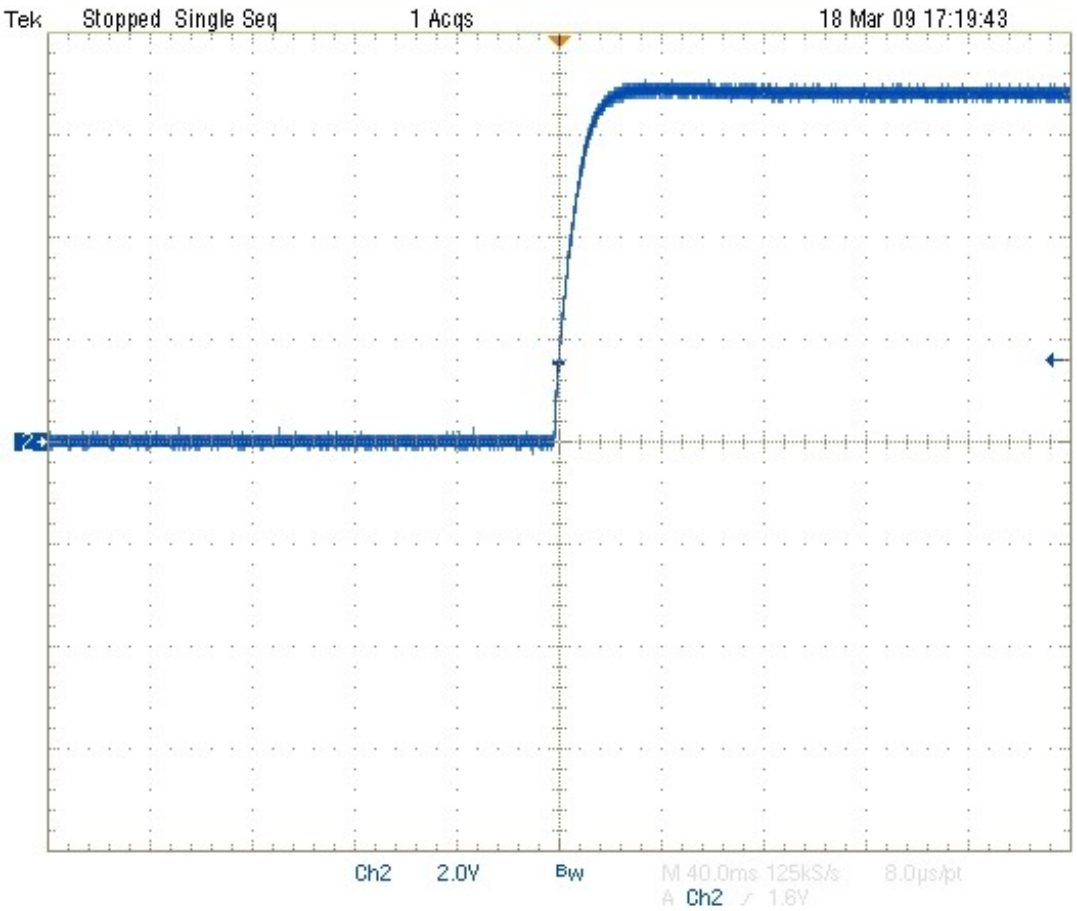
RS232C to Mother Board

ColdFire 5282 Board

Fully Fabricated MPS Shelf

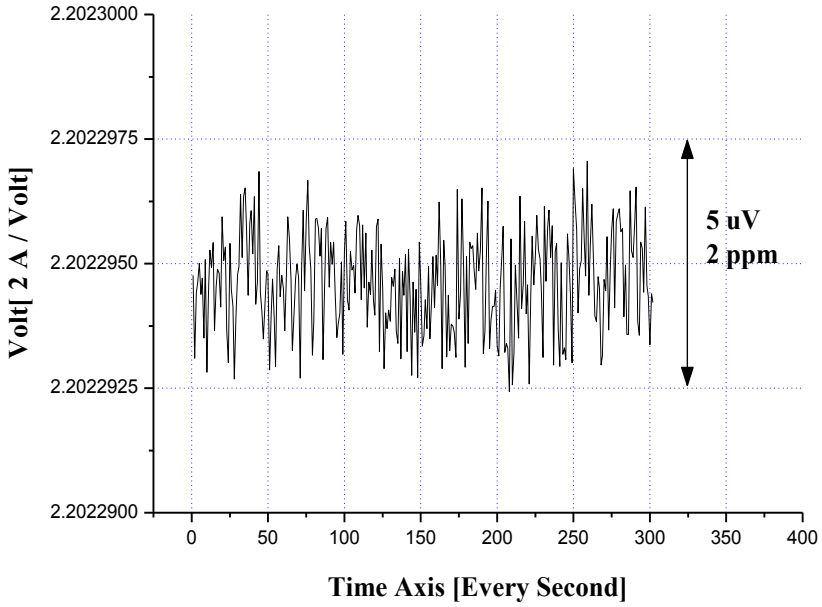


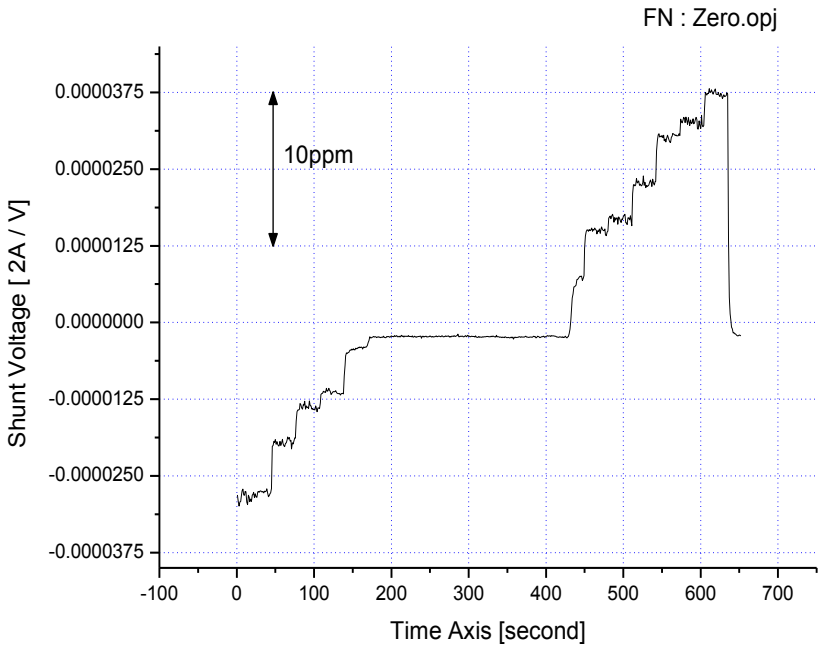
Step Function Response



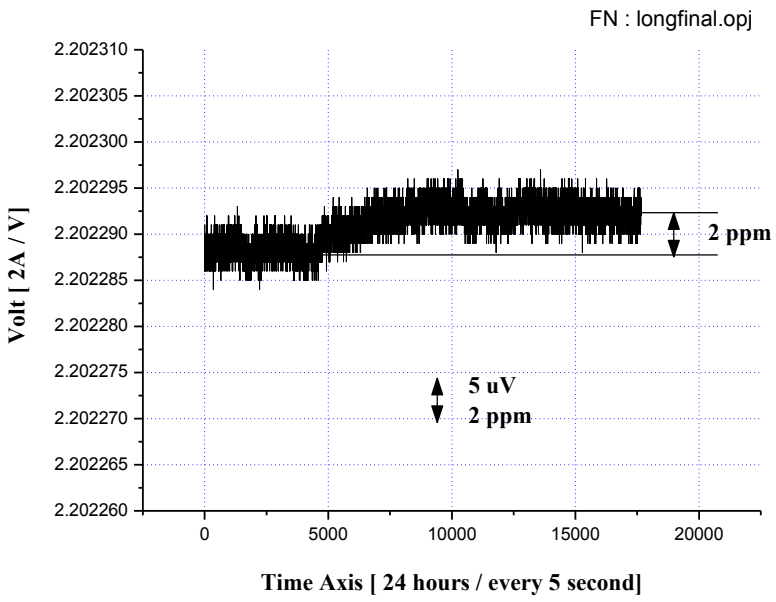
Step Response of the MPS (0 to 5A, 40ms scale)

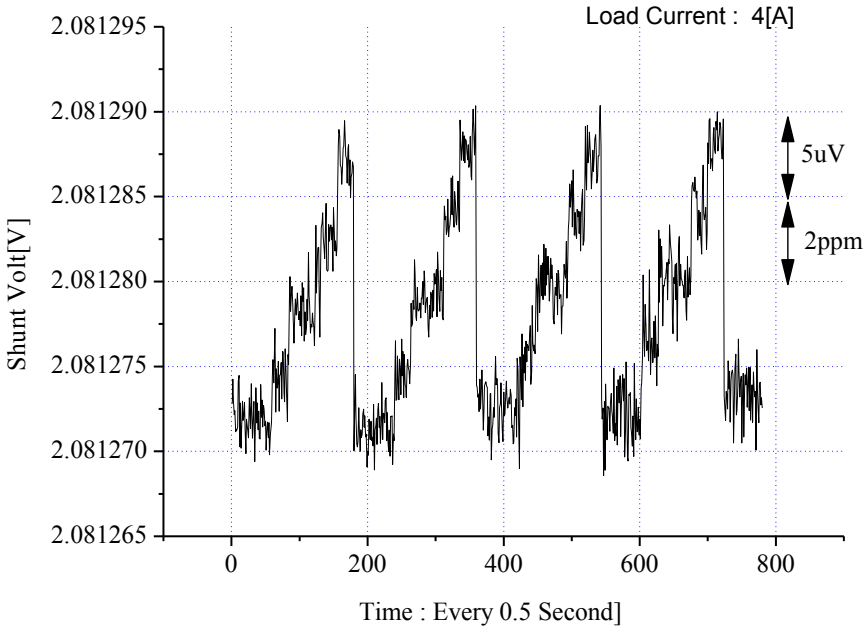
Short Term Stability and Zero Cross



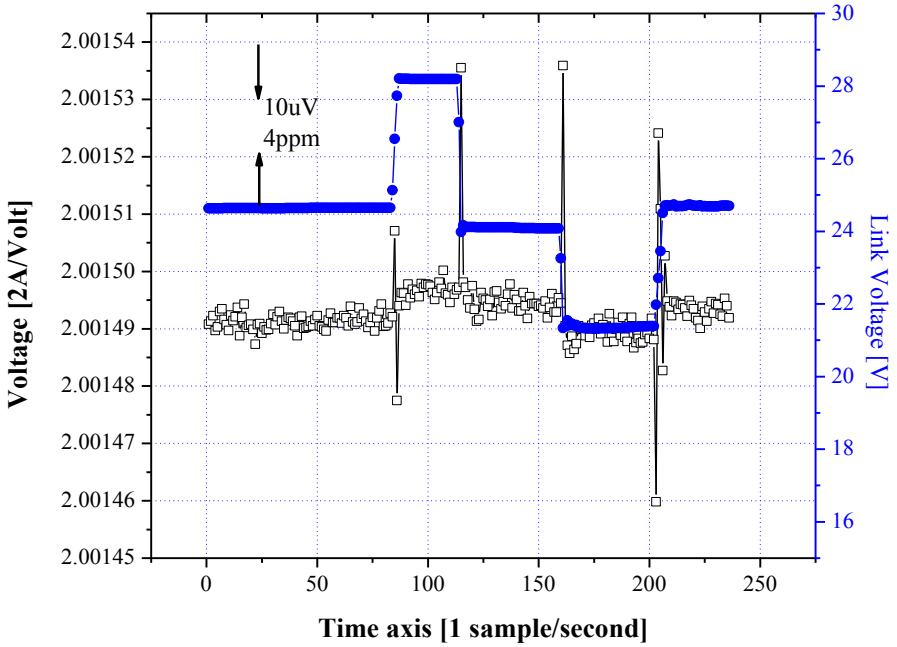


Long Term Stability & Repeatability

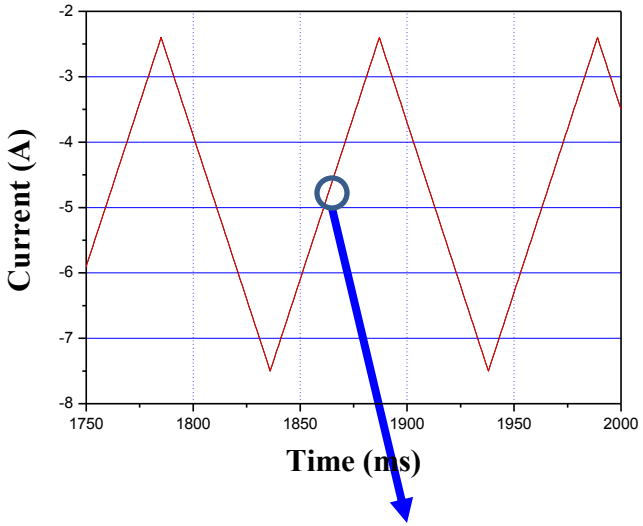


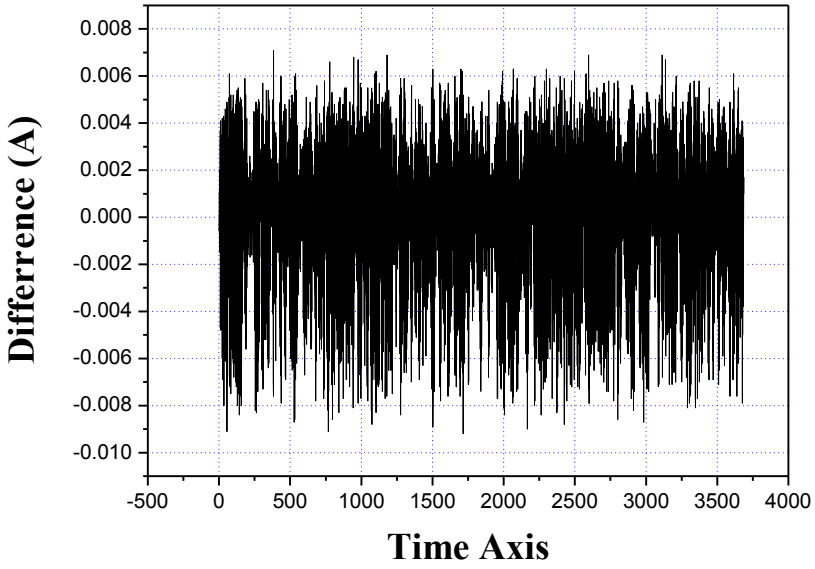


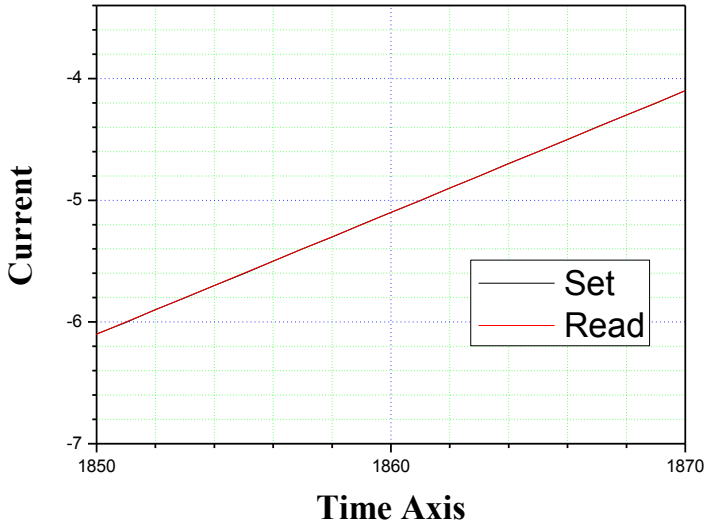
Link voltage variation



Current difference between set and read value







Remarks

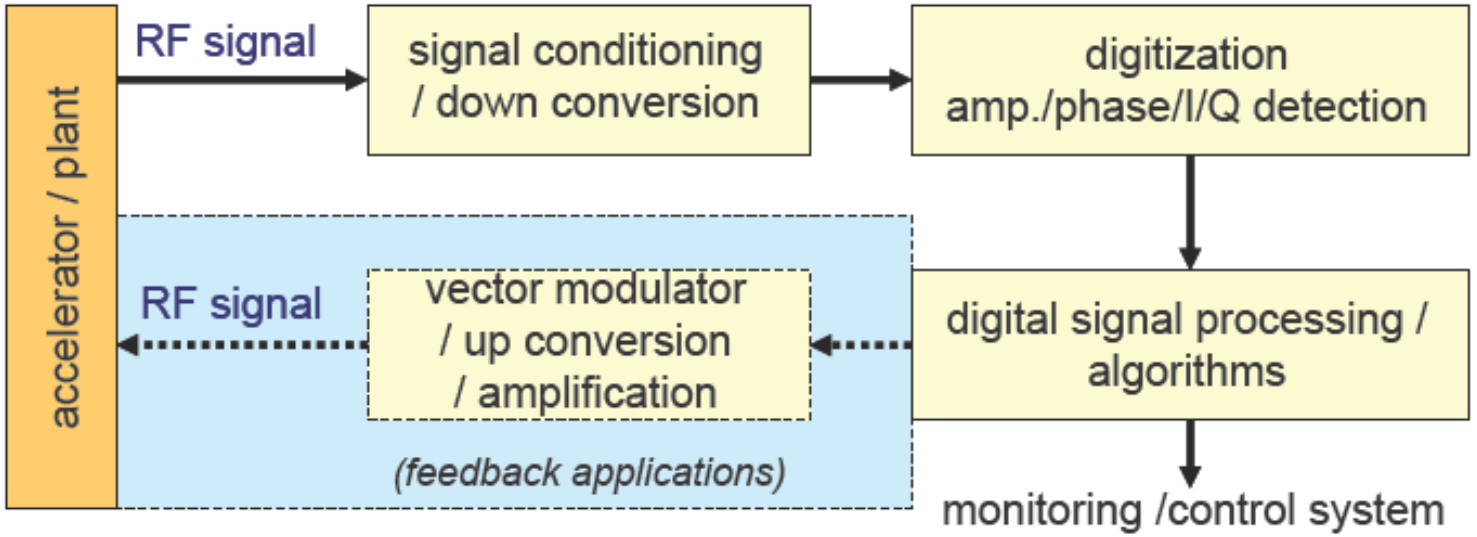
1. Fully Digital Control
2. Stability : Less than 5ppm
3. Output Current : up to 1000A
4. Unipolar and Bipolar Power Supply
5. Ethernet (+EPICS), CAN and RS232C
6. Interlock
7. Easy access : Key and Display
8. Configuration : programmable
9. Easy maintenance

LLRF for PLS-II

Contents

1. Introduce the general concept for the control system
2. Cavity Modeling
3. Signal processing
4. CORDIC algorithm
5. IQ demodulator
6. PI controller
7. Digital Filters
8. IQ output
9. Local Oscillator
10. Digital Hardware system

Digital LLRF system



LLRF looks very similar to many other applications,
e.g. diagnostics (bunch-by-bunch feedback, position monitoring, …)

for feedback systems: ultimate error is dominated by the measurement process
(systematic error, accuracy, linearity, repeatability, stability, resolution, noise)

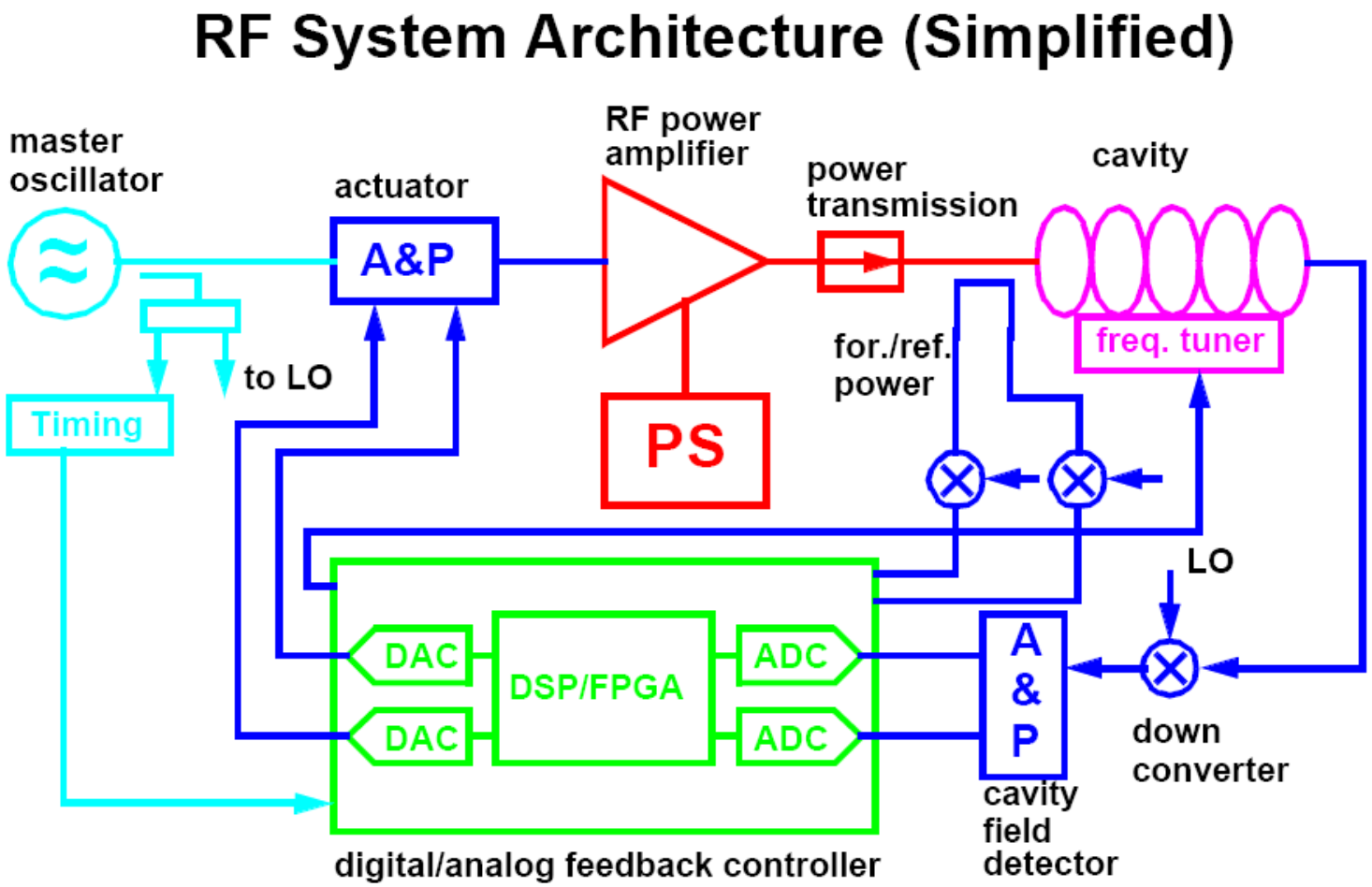
: By Thomas Schilcher

Technical Specifications of the LLRF for SC

Cavity Parameters	Unit	Value
Cavity frequency	MHz	499.66
Half cavity bandwidth	KHz	4.34
Number of SC cavity	ea	2+1
LLRF loop gain	dB	?
Phase stability	Degree	±1
Amplitude stability	%	±1
RF frequency error in steady state	Hz	±10 ?

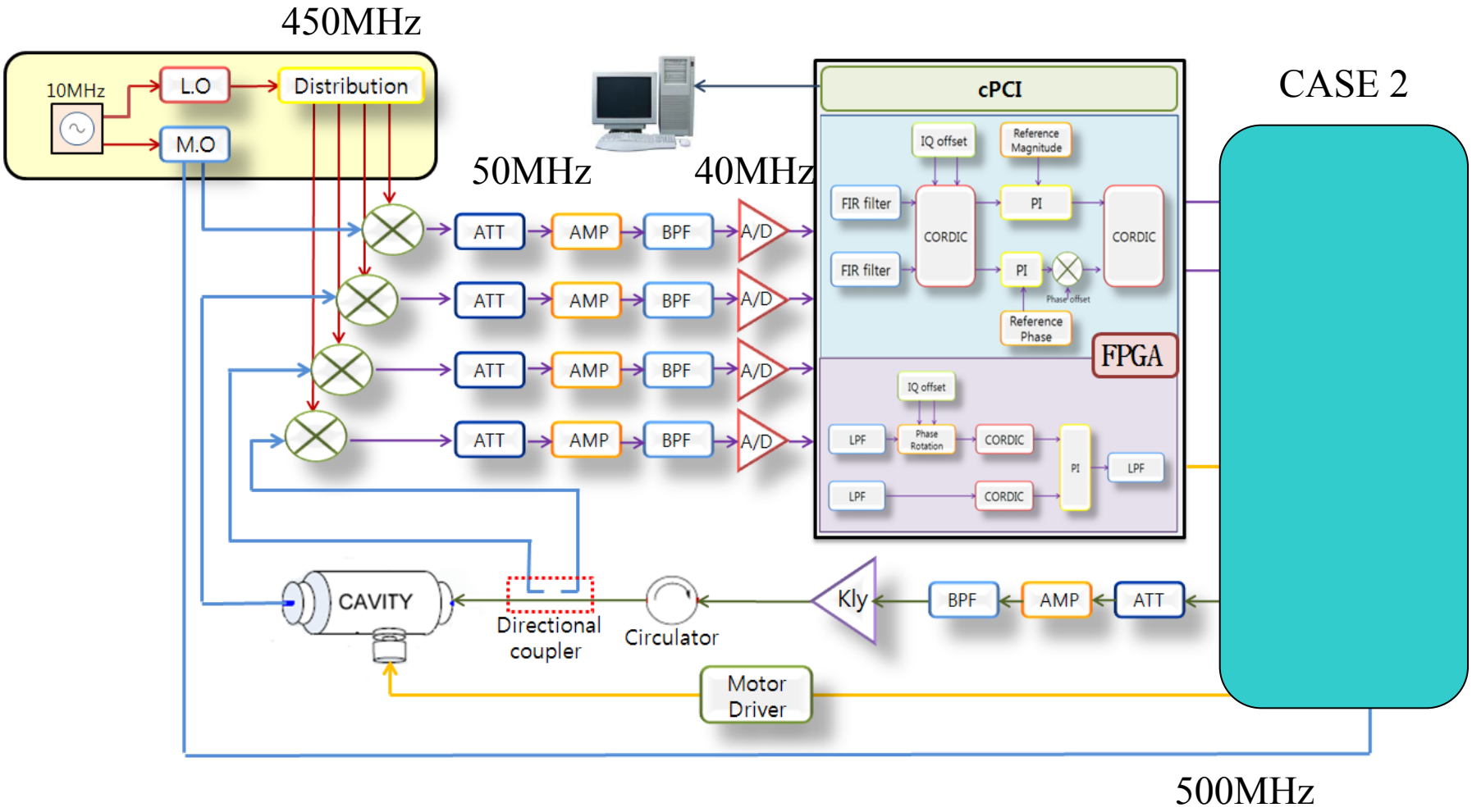
Signal Processing

Concept for the LLRF system



By : Stefan Simrock

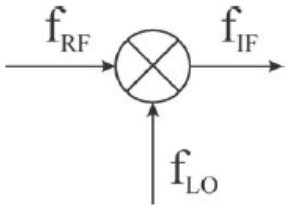
System Block Diagram



I/Q demodulation

RF Down Conversion

$$y_{RF}(t) = A_{RF} \cdot \sin(\omega_{RF} t + \varphi_{RF})$$



$$y_{IF}(t) = y_{RF}(t) \cdot y_{LO}(t)$$

$$y_{LO}(t) = A_{LO} \cdot \cos(\omega_{LO} t + \varphi_{LO})$$

$$\Rightarrow y_{IF}(t) = \frac{1}{2} A_{LO} A_{RF} \cdot \Big(\boxed{\sin[(\omega_{RF} - \omega_{LO})\, t + (\varphi_{RF} - \varphi_{LO})]} + \boxed{\sin[(\omega_{RF} + \omega_{LO})\, t + (\varphi_{RF} + \varphi_{LO})]} \Big)$$

lower sideband

upper sideband

After low pass filter

$$y_{IF}(t) = A_{IF} \sin(\omega_{IF} t + \varphi_{IF})$$

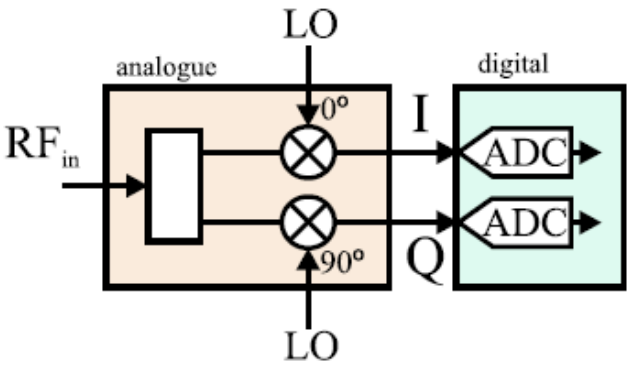
: RF properties are conserved (Amplitude ,Phase)

$$\omega_{IF} = \omega_{RF} - \omega_{LO}$$

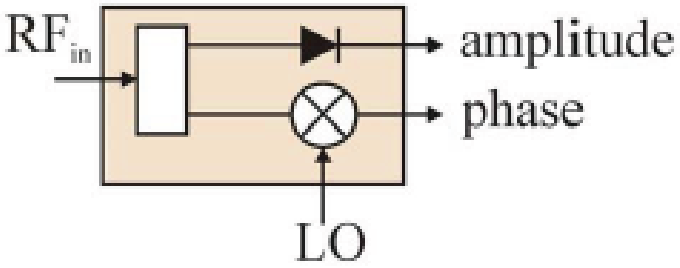
$$A_{IF} = \frac{1}{2} A_{LO} A_{RF}$$

$$\varphi_{IF} = \varphi_{RF} - \varphi_{LO}$$

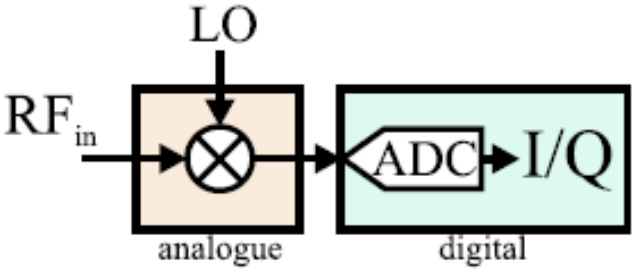
1. Analog IQ detection



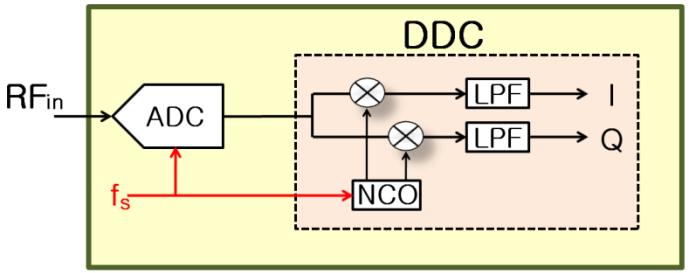
3. Direct amplitude and phase detection



2. Digital IQ sampling / non-IQ sampling



4. Digital Down Conversion (DDC)

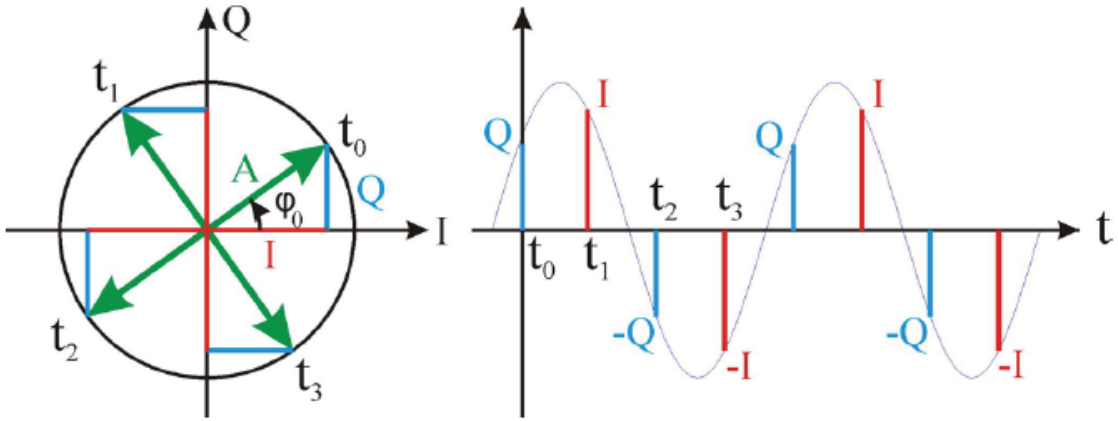


IQ sampling

$$f_s = \frac{4}{2n+1} \bullet f_{IF}$$

n = 0,1, 2, 3,---

Degree : 90, 270, 450, ---



$$f_s = 4f$$

In case of n = 0

$k=0 \quad t_0 \quad y_s(t_0) = Q$

$k=1 \quad t_1 \quad y_s(t_1) = I$

$k=2 \quad t_2 \quad y_s(t_2) = -Q$

$k=3 \quad t_3 \quad y_s(t_3) = -I$

$$I(n) = [x(4n-1) - x(4n-3)]/2$$

$$Q(n) = [x(4n) - x(4n-2)]/2$$

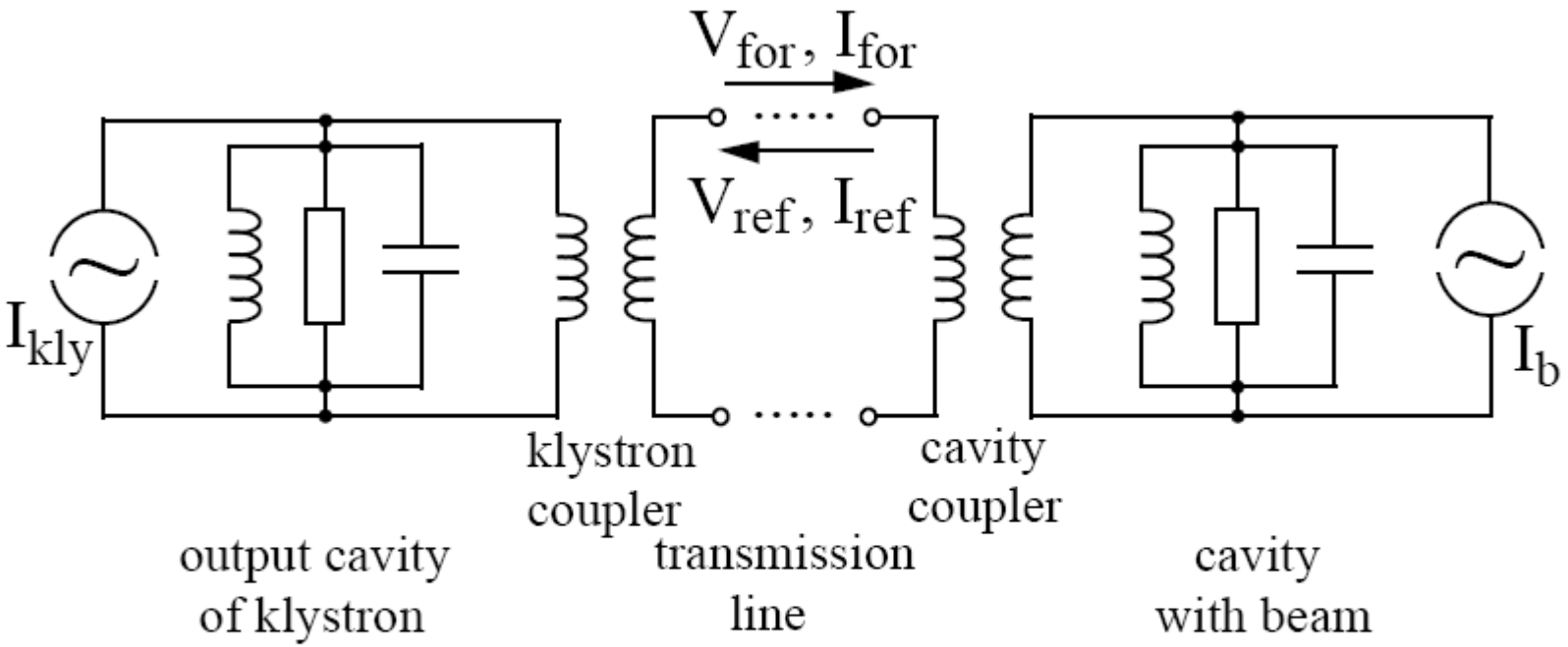
Cancel out offset

PID Controller Design

Controller Specifications

- System bandwidth : ~100KHz
  - Cavity bandwidth : 4.5KHz
- Gain margin : > 6 dB
- Phase margin : > 45°

Cavity Modeling



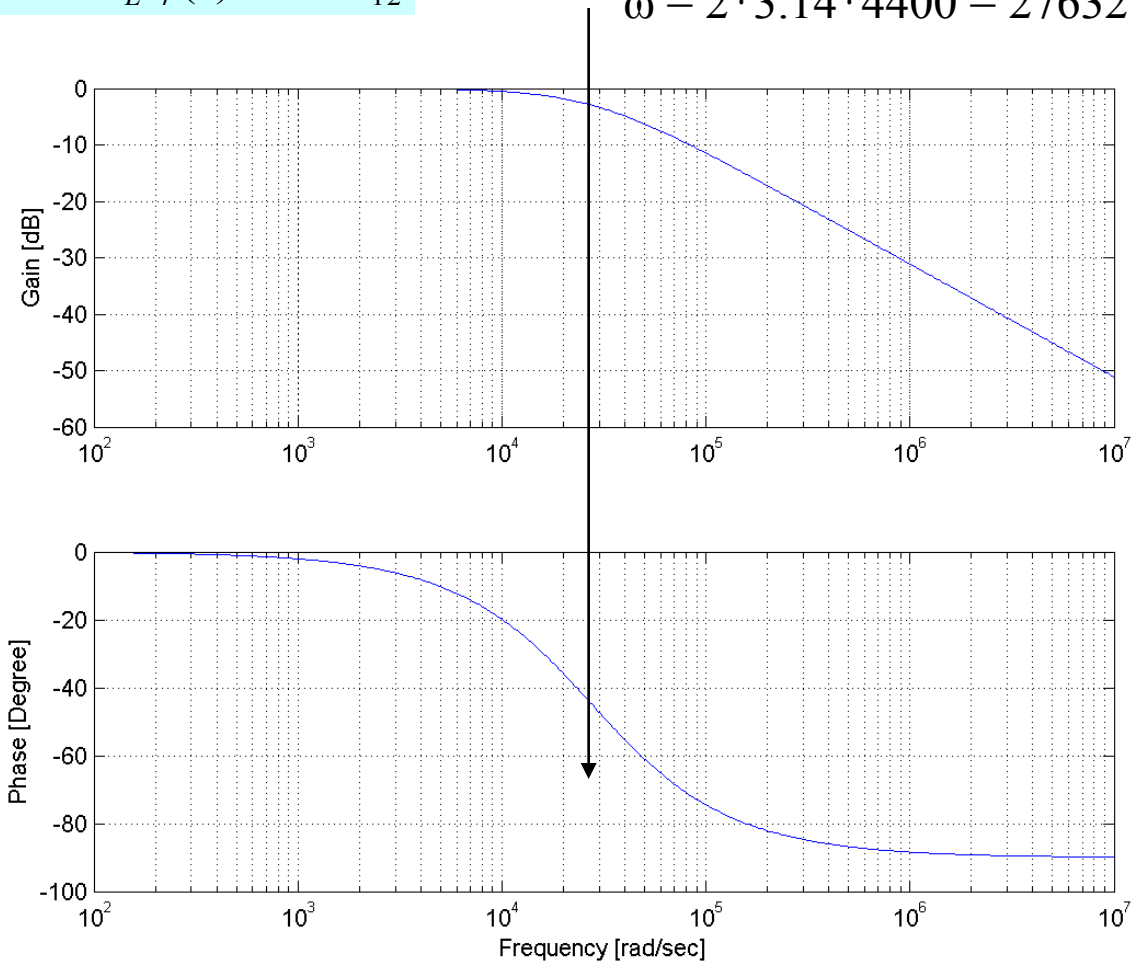
Model of a cavity with beam coupled to a klystron by couplers and transmission lines.

Matlab Simulation

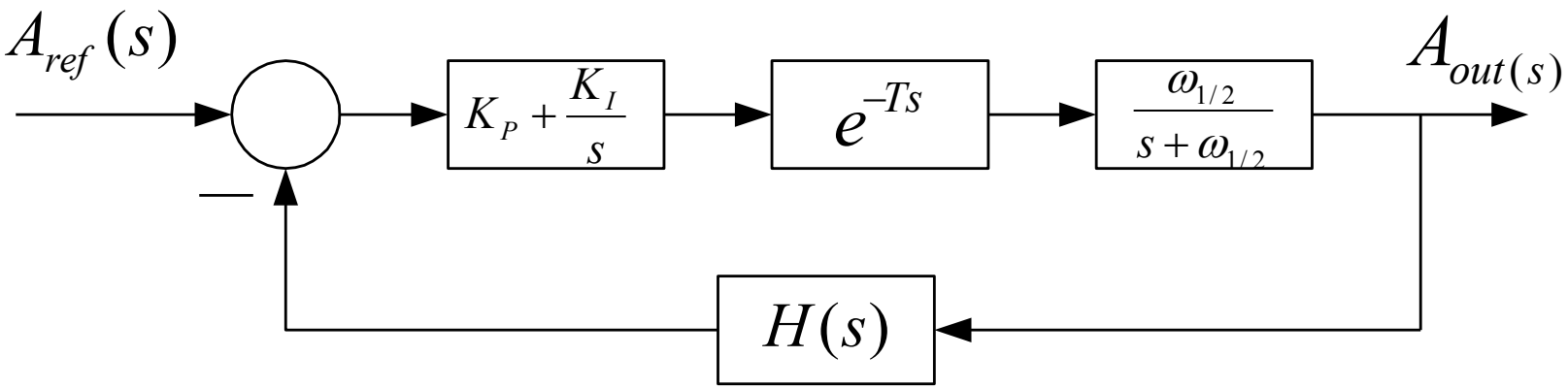
The transfer function *H(s)* defined as

$$H_{cav}(s) = \frac{V_r(s)}{R_L I_r(s)} = \frac{\omega_{12}}{s + \omega_{12}}$$

ω = 2*3.14*4400 = 27632 rad/sec



LLRF Model



$K_I = \omega_{1/2}$ of 4.4 KHz

T is 1.5 μs with the second order Pade approximation of the time delay

$K_P = 15$

$$G(s) = K_P \bullet g \bullet \left(1 + \frac{Ki}{s}\right) \bullet \frac{\omega_{1/2}}{s + \omega_{1/2}} \bullet \frac{\omega_{bpf}}{s + \omega_{bpf}} \bullet e^{-Ts}$$

$$\cong K_P \bullet g \bullet \left(1 + \frac{Ki}{s}\right) \bullet \frac{\omega_{1/2}}{s + \omega_{1/2}} \bullet e^{-Ts} \qquad \text{when} \quad \omega_b << \omega_{bpf}$$

where $\omega_{1/2}$ half-bandwidth , ω_{bpf} output band-pass filter | 5MHz and 1MHz

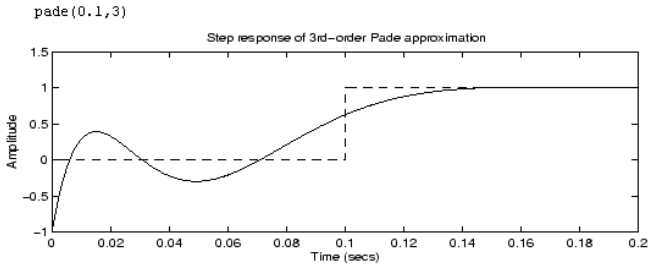
k_p proportional gain , k_i integral gain

g lumped gain (analog + others)

T total loop delay

Closed-loop transfer function with unit gain is :

$$GB(s) = \frac{G(s)}{1 + G(s)} = \frac{gK_p\omega_{1/2}(s + k_i)e^{-Ts}}{s(s + \omega_{1/2}) + gK_p\omega_{1/2}(s + k_i)e^{-Ts}}$$



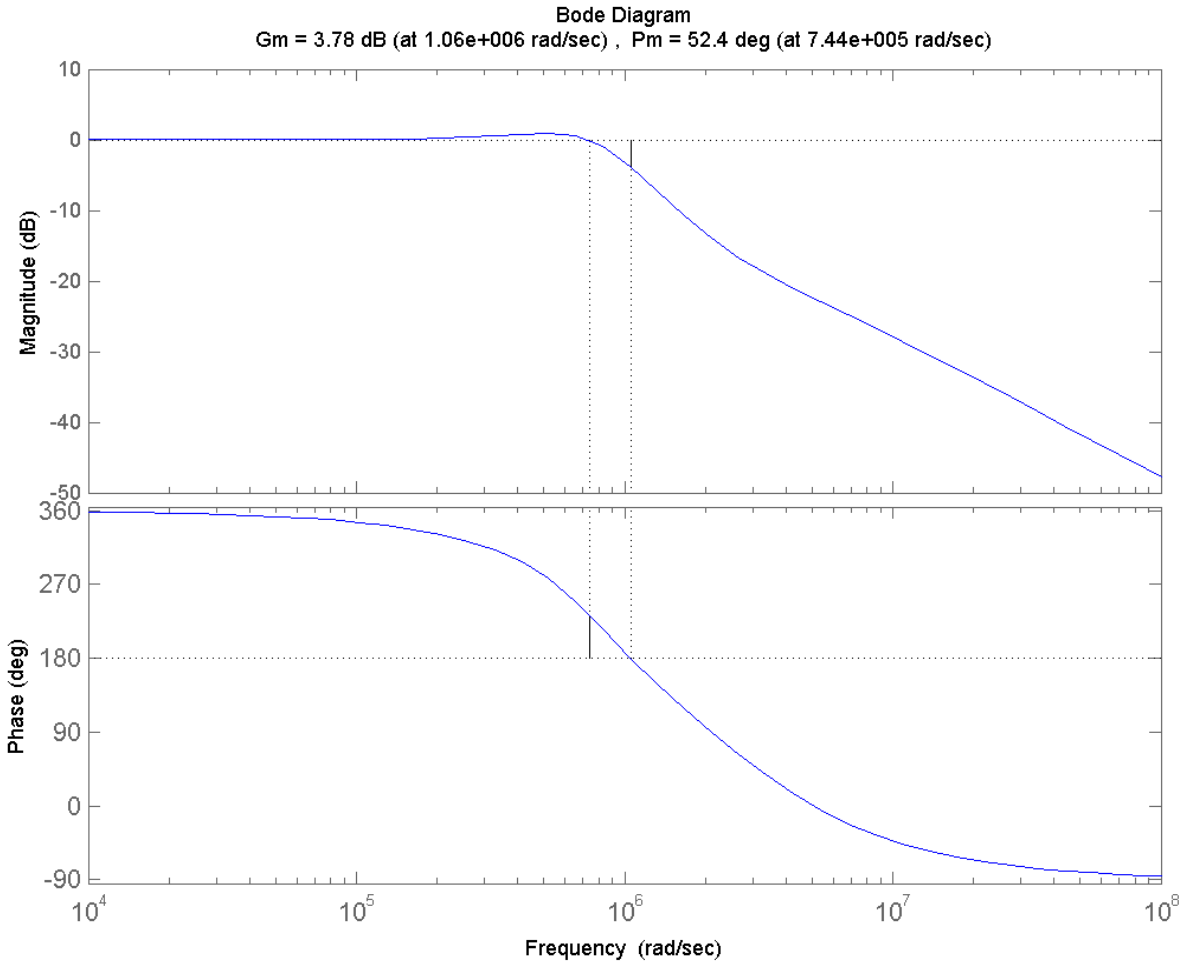
First order Pade approximation

$$P_d(s) = \frac{1 - Ts/2}{1 + Ts/2}$$

Second order Pade approximation

$$P_d(s) = \frac{1 - Ts/2 + (Ts)^2/12}{1 + Ts/2 + (Ts)^2/12}$$

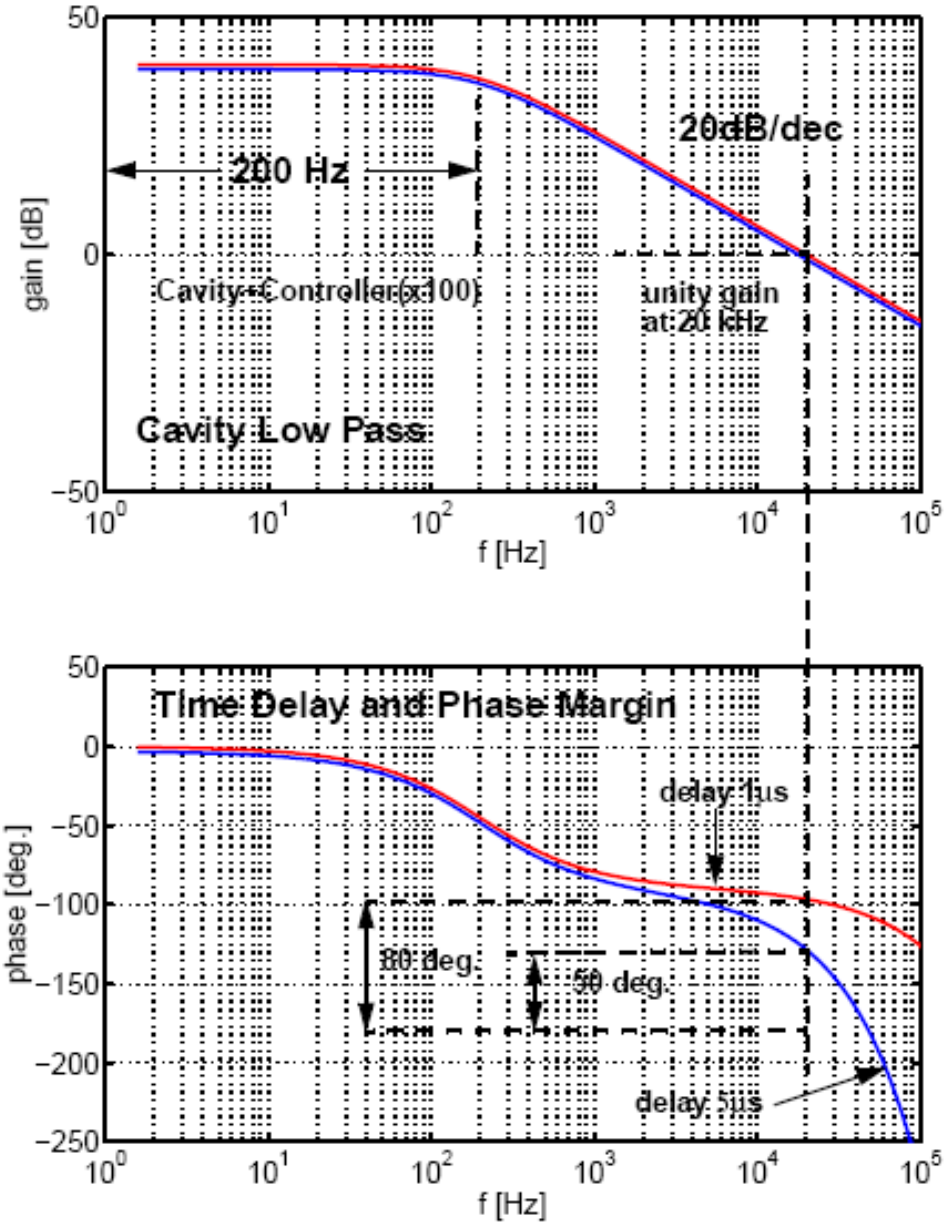
Frequency Responses



The close loop response showed that the phase margin was about 52° and gain 3.8 dB.

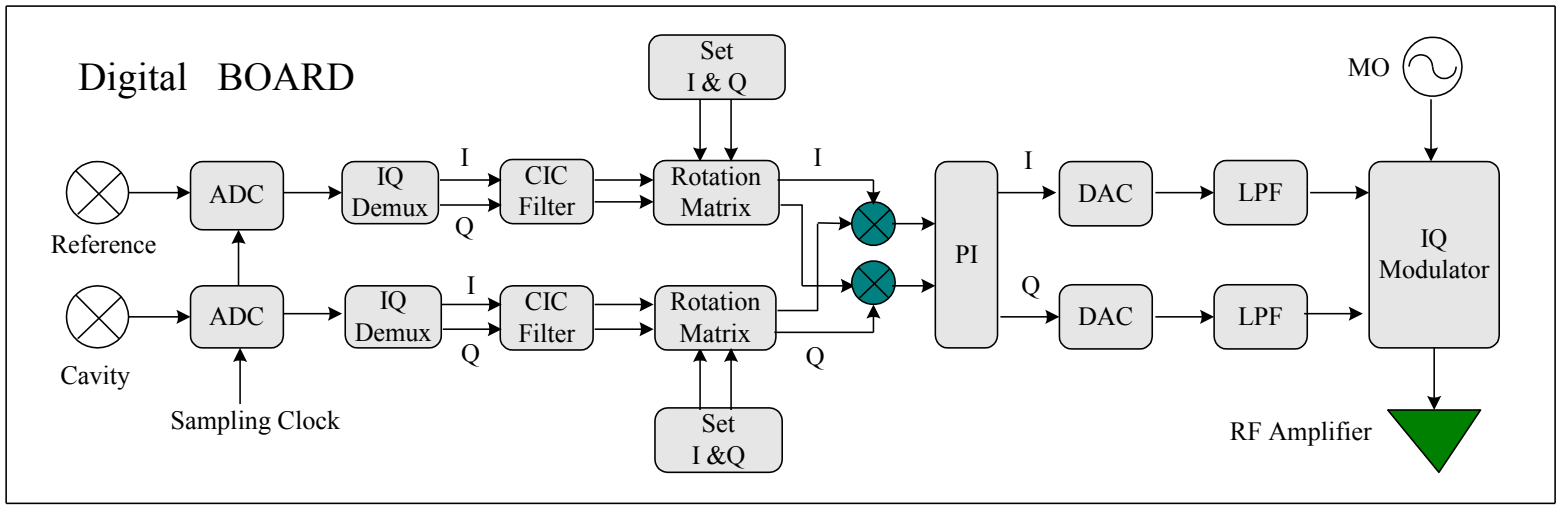
Expected Latency

1	Cable	100ns	20m
2	Klystron	100ns	
3	Waveguide	100ns	
3	ADC	100ns	
4	FPGA	200ns	
5	DAC	50ns	
	TOTAL	650ns	



Vector Signal Output

The gain bandwidth product is limited to about 1MHz due to the low-pass characteristics of the cavity, the bandwidth limitations of electronics and Klystrons and cable delay.



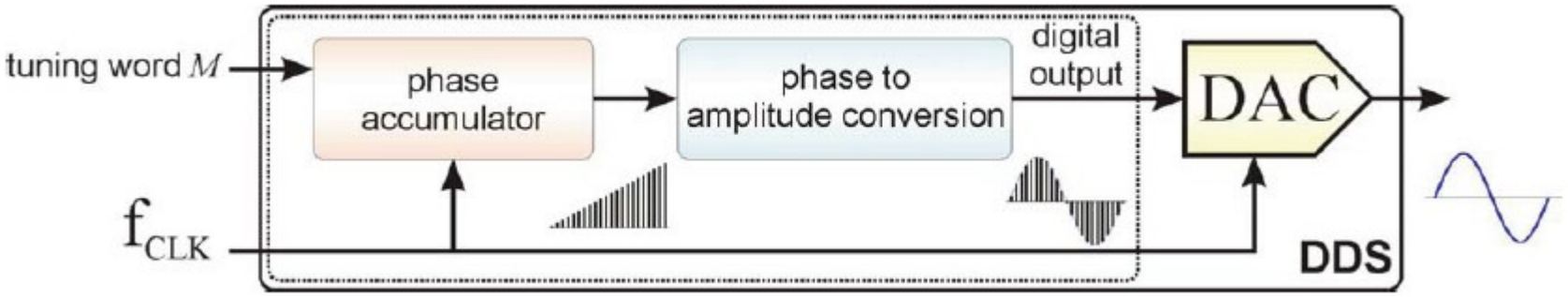
1. 16-bit ADC 40MHz
2. IQ de-multiplex : I & Q output 20 MHz
3. CIC filter with decimation : 2 MHz
4. PI : Amplitude and Phase regulation
5. Vector out (Mux out : 50MHz)

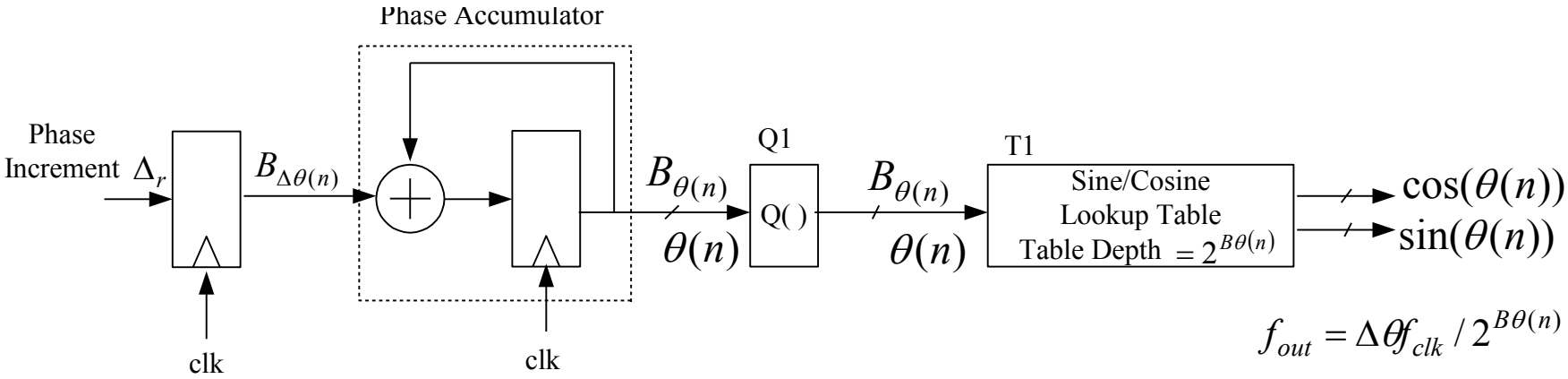
Rotation Matrix

$$\begin{pmatrix} I_{out} \\ Q_{out} \end{pmatrix} = A \begin{pmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{pmatrix} \begin{pmatrix} I_{in} \\ Q_{in} \end{pmatrix}$$

Output to the Klystron

Direct Digital Synthesizer





$$f_{out} = \Delta\theta f_{clk} / 2^{B\theta(n)}$$

$$f_{out} = \frac{f_{clk} \times \Delta\Theta}{2^N}$$

$\Delta\Theta = 12$: Phase Increment

$f_{clk} = 120MHz$

$N = 10$

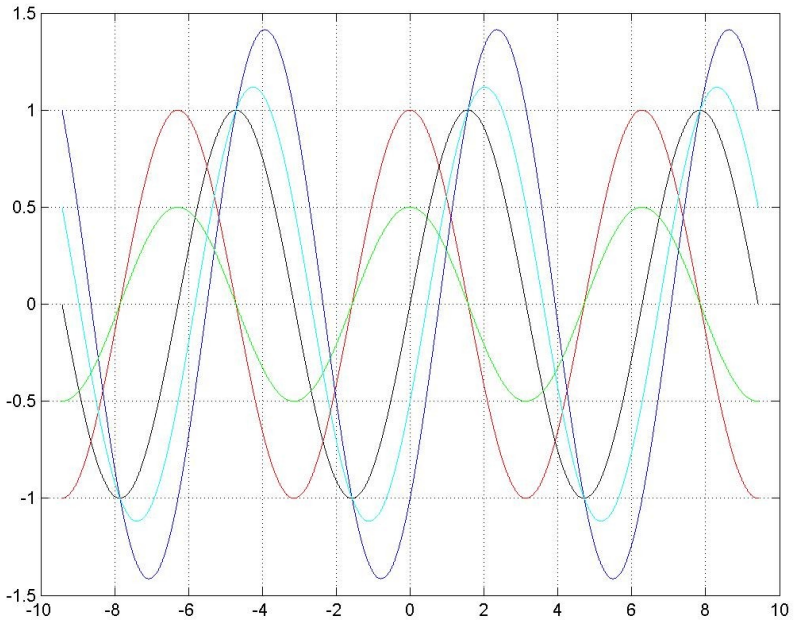
$$f_{out} = \frac{f_{clk} \times \Delta\Theta}{2^N} = 1.4062\text{MHz}$$

Vector Output (1)

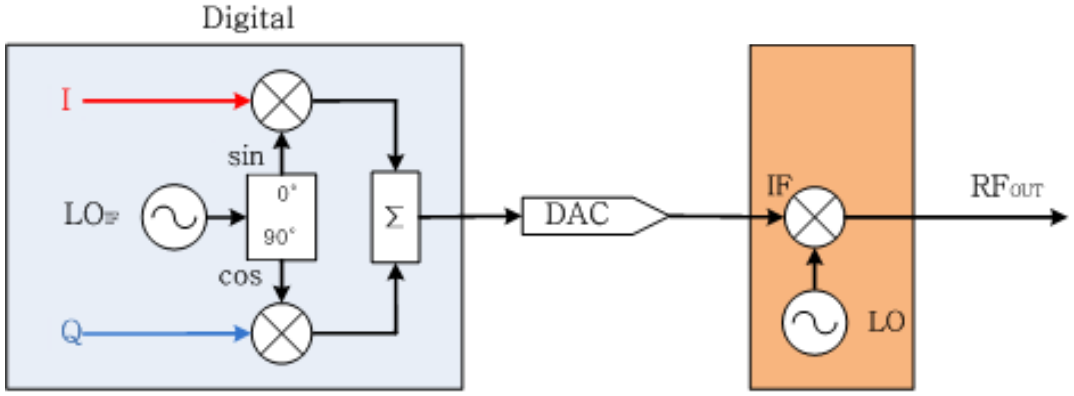
$$f_{out} = \frac{M \times 160MHz}{2^N} = 50\text{MHz}$$

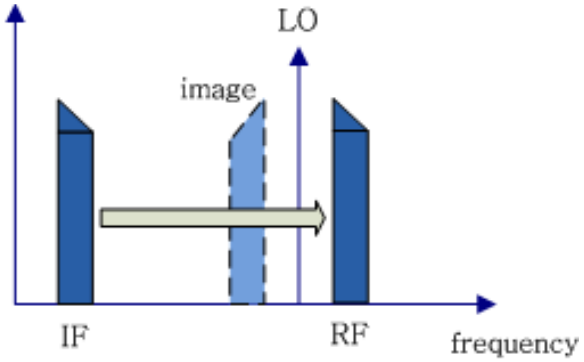
where $M = 5$ and $N=4$

Phase Increment : 112.5°



Black = sin(t);
Red = cos(t);
Blue = y1-y2;
Green = 0.5*cos(t);
Cyan = y1-y4;



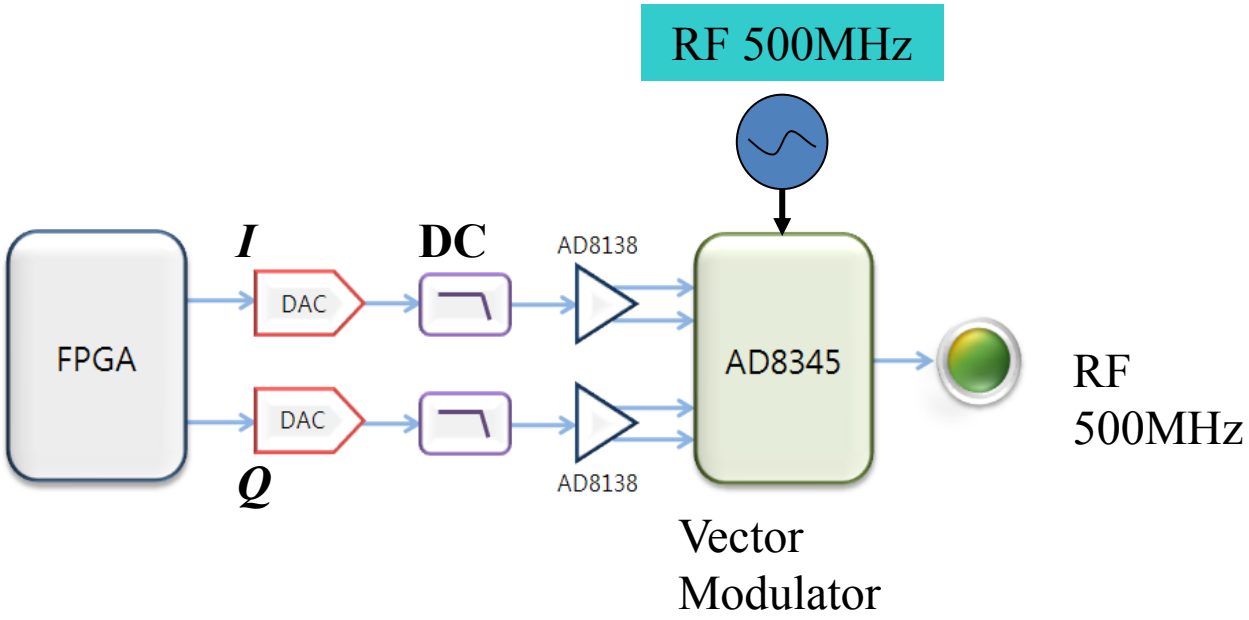


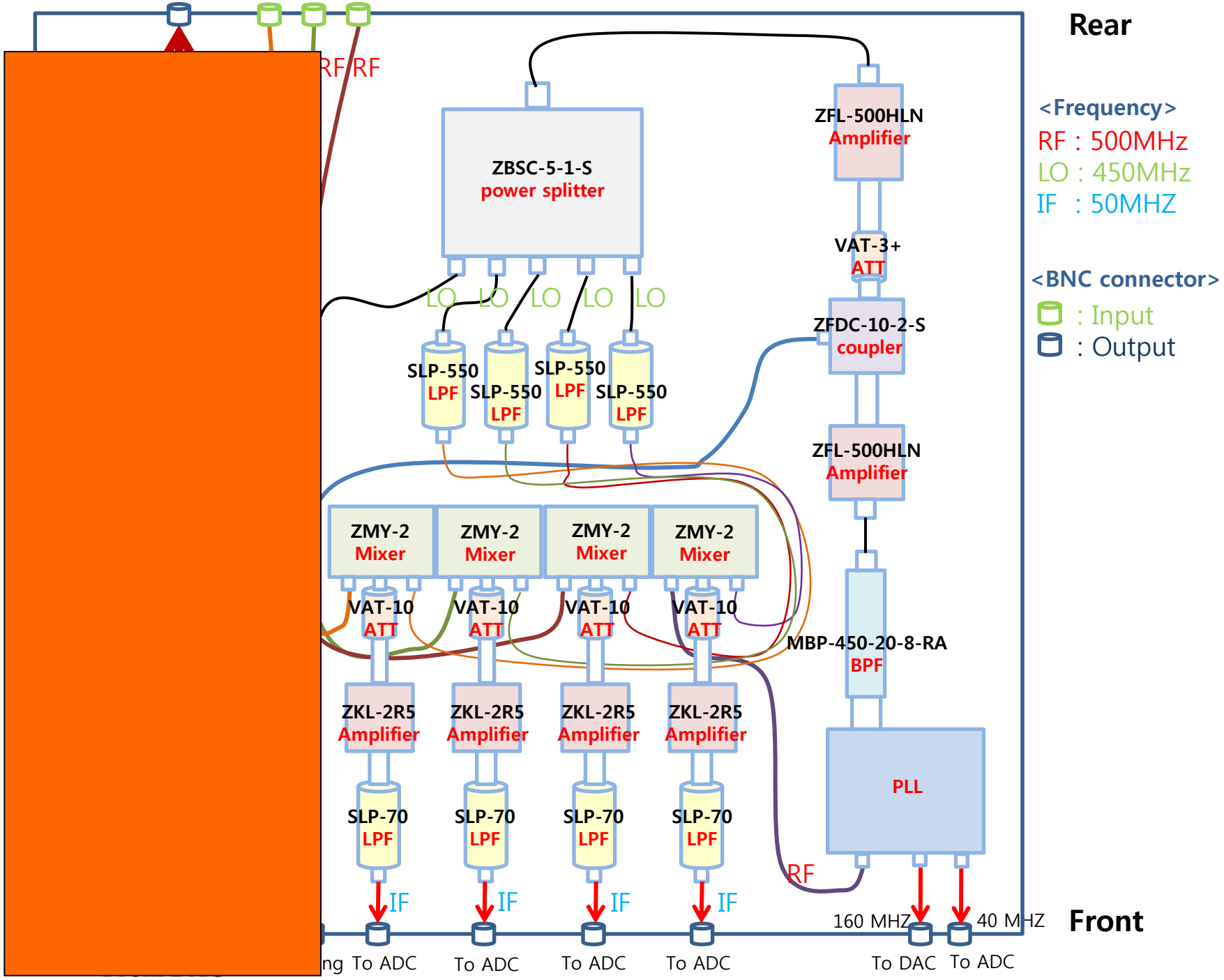
In FPGA

Vector Output (2)

$$\begin{aligned} RF_{out}(t) &= I \cdot A_{RF} \cdot \sin\omega t + Q \cdot A_{RF} \cdot \cos\omega t \\ &= A_{out} \cdot \sin(\omega t + \varphi_0) \end{aligned}$$

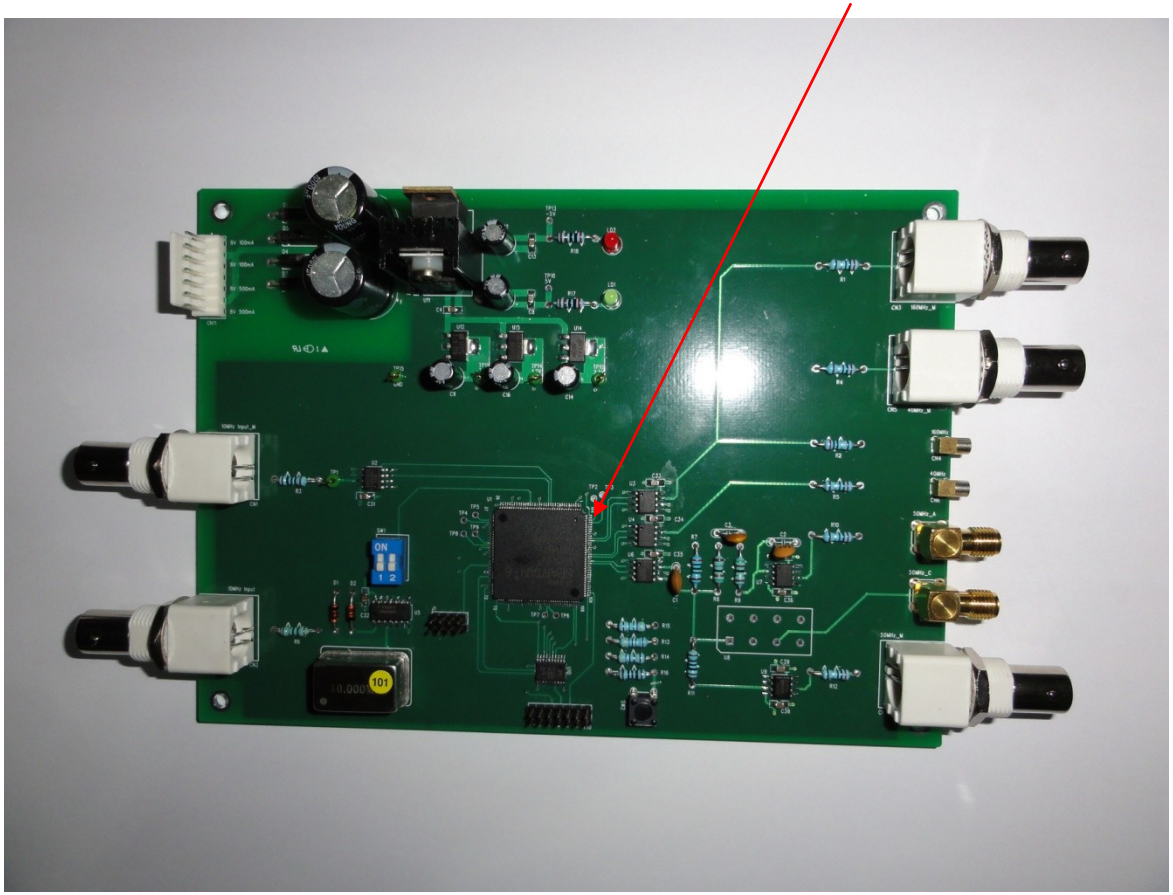
$$A_{out} = A_{RF}\sqrt{I^2 + Q^2} \qquad \varphi_0 = \operatorname{atan}\left(\frac{Q}{I}\right)$$




Rear
<Frequency>
RF : 500MHz
LO : 450MHz
IF : 50MHZ
<BNC connector>
: Input
: Output
RF RF
ZBSC-5-1-S
power splitter
ZFL-500HLN
Amplifier
VAT-3+
ATT
LO LO LO LO LO
ZFDC-10-2-S
coupler
SLP-550
LPF
SLP-550
LPF
SLP-550
LPF
SLP-550
LPF
ZFL-500HLN
Amplifier
ZMY-2
Mixer
ZMY-2
Mixer
ZMY-2
Mixer
ZMY-2
Mixer
VAT-10
ATT
VAT-10
ATT
VAT-10
ATT
VAT-10
ATT
MBP-450-20-8-RA
BPF
ZKL-2R5
Amplifier
ZKL-2R5
Amplifier
ZKL-2R5
Amplifier
ZKL-2R5
Amplifier
PLL
SLP-70
LPF
SLP-70
LPF
SLP-70
LPF
SLP-70
LPF
RF
IF
IF
IF
IF
160 MHZ
40 MHZ
Front
ng To ADC
To ADC
To ADC
To ADC
To DAC
To ADC

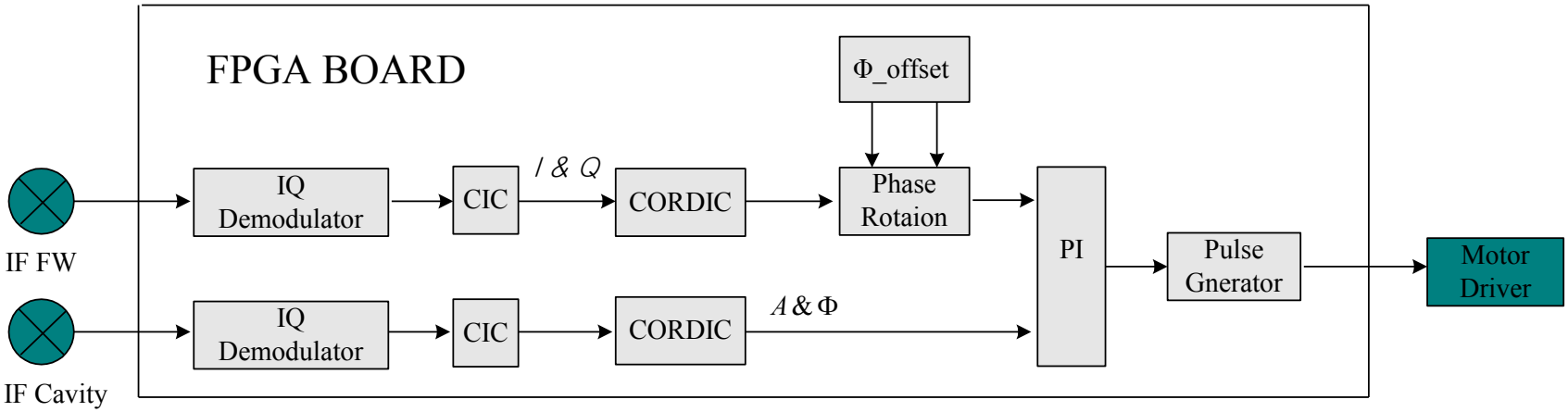
Generating Local Frequency (DDS)

Using the FPGA Xilinx Spartan-6



- External Reference or Internal Source
- Output Frequency : programmable

- CORDIC calculates phase difference between cavity and forward power
- ~10 iterations to get the resolution better than 0.001º .
  if 16 iterations for 1/80MHz is 200ns



- Frequency regulation loop
  - Range : ±200KHz
  - Resolution : 2 Hz
  - Bandwidth : < 5Hz

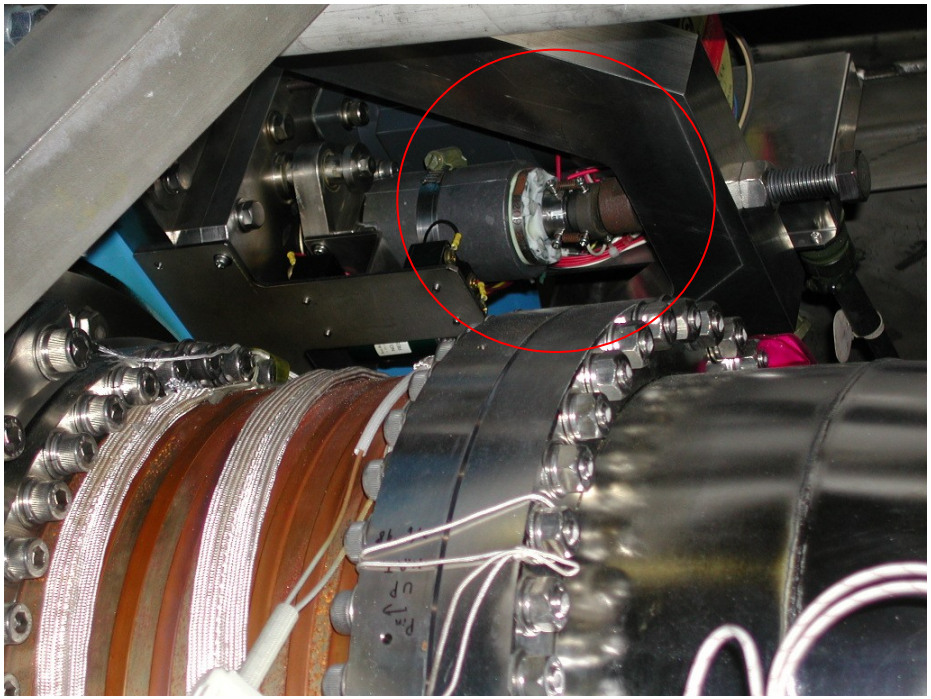
- Don't consider the piezo actuator
  - Range : ±500 Hz
  - Resolution : 1Hz
  - Bandwidth : ~1000 Hz
  - Voltage : ~100V

Module of accelerating SC

◆ Important components: frequency tuner

Motor tuner (coarse tuning)
- range of 400 kHz

Piezo tuner (fine tuning)
- tuning range of 6 kHz
- response of 20 Hz



Digital Hardware

1) Virtex-6 and LTC2205
2) VHS-ADC Lyrtech (CANADA)

Virtex-6 FPGA

Virtex-6 FPGA Feature Summary

Table 1: **Virtex-6 FPGA Feature Summary by Device**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices[2]	Block RAM Blocks			MMCMs[4]	Interface Blocks for PCI Express	Ethernet MACs[5]	Maximum Transceivers		Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)		18 Kb[3]	36 Kb	Max (Kb)				GTX	GTH		
XC6VLX75T	74,496	11,640	1,045	288	312	156	5,616	6	1	4	12	0	9	360
XC6VLX130T	128,000	20,000	1,740	480	528	264	9,504	10	2	4	20	0	15	600
XC6VLX195T	199,680	31,200	3,040	640	688	344	12,384	10	2	4	20	0	15	600
XC6VLX240T	241,152	37,680	3,650	768	832	416	14,976	12	2	4	24	0	18	720
XC6VLX365T	364,032	56,880	4,130	576	832	416	14,976	12	2	4	24	0	18	720
XC6VLX550T	549,888	85,920	6,200	864	1,264	632	22,752	18	2	4	36	0	30	1200
XC6VLX760	758,784	118,560	8,280	864	1,440	720	25,920	18	0	0	0	0	30	1200
XC6VSX475T	476,160	74,400	7,640	2,016	2,128	1,064	38,304	18	2	4	36	0	21	840
XC6VHX250T	251,904	39,360	3,040	576	1,008	504	18,144	12	4	4	48	0	8	320
XC6VHX255T	253,440	39,600	3,050	576	1,032	516	18,576	12	2	2	24	24	12	480
XC6VHX380T	382,464	59,760	4,570	864	1,536	768	27,648	18	4	4	48	24	18	720
XC6VHX565T	566,784	88,560	6,370	864	1,824	912	32,832	18	4	4	48	24	18	720

Issue is DSP Slices

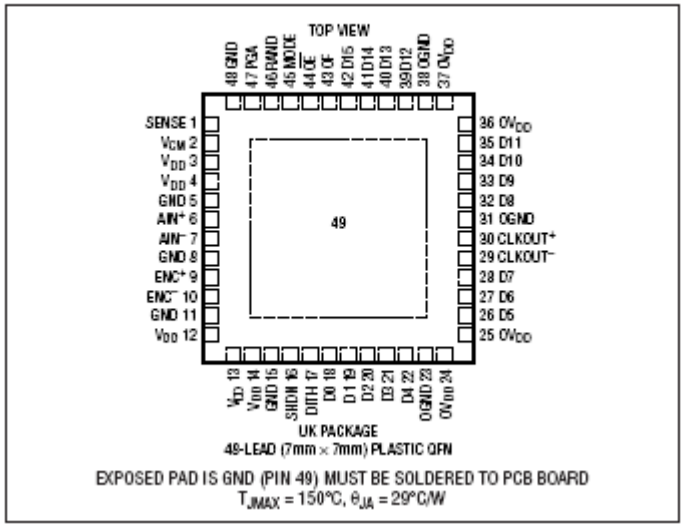
LINEAR TECHNOLOGY

LTC2205/LTC2204
16-Bit, 65Msps/40Msps
ADCs

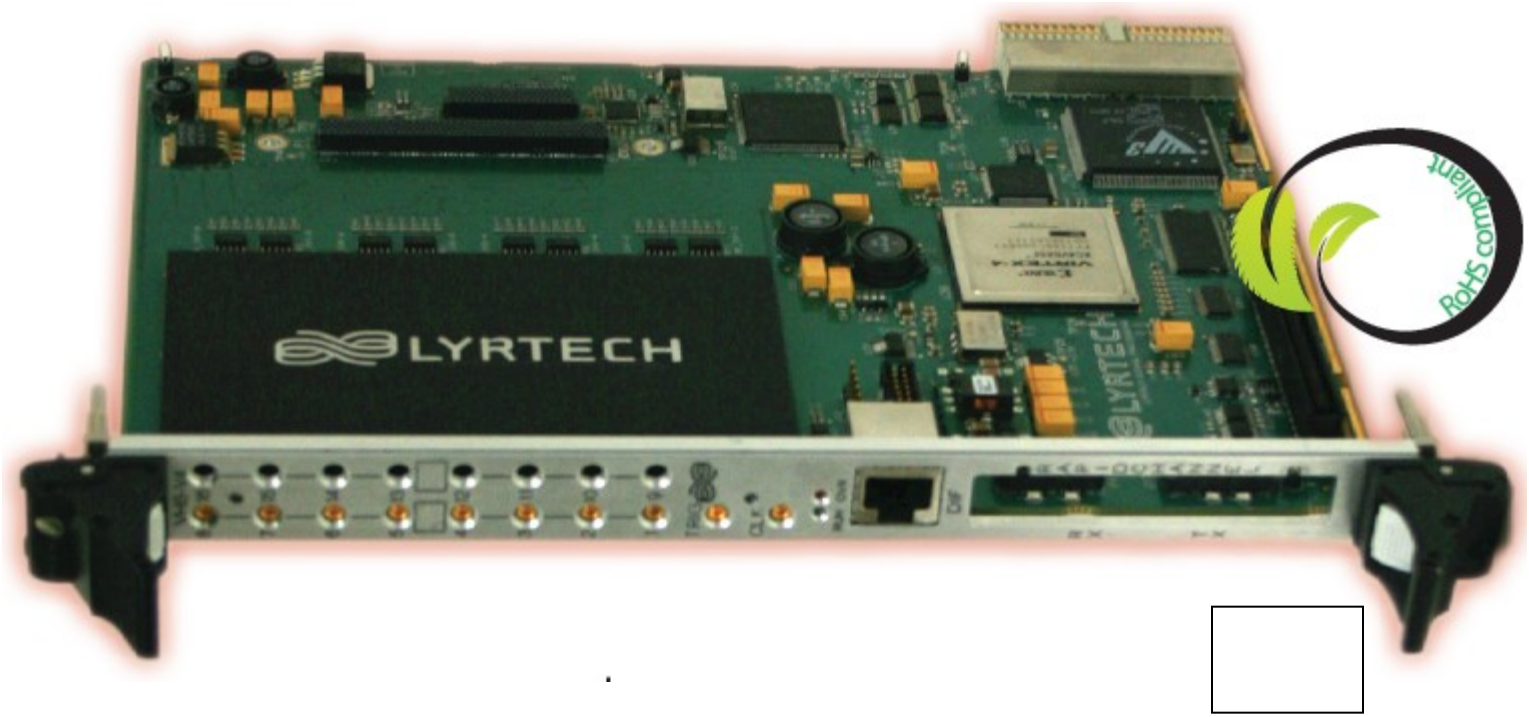
FEATURES

- **Sample Rate: 65Msps/40Msps**
- **79dB SNR and 100dB SFDR (2.25V_{P-P} Range)**
- **SFDR >92dB at 140MHz (1.5V_{P-P} Input Range)**
- **PGA Front End (2.25V_{P-P} or 1.5V_{P-P} Input Range)**
- **700MHz Full Power Bandwidth S/H**
- **Optional Internal Dither**
- **Optional Data Output Randomizer**
- Single 3.3V Supply
- Power Dissipation: 610mW/480mW
- Optional Clock Duty Cycle Stabilizer
- Out-of-Range Indicator
- Pin Compatible Family
  - 105Msps: LTC2207 (16-Bit), LTC2207-14 (14-Bit)
  - 80Msps: LTC2206 (16-Bit), LTC2206-14 (14-Bit)
  - 40Msps: LTC2204 (16-Bit)
- 48-Pin (7mm × 7mm) QFN Package

PIN CONFIGURATION



VHS-ADC Lyrtech (CANADA)



- AC coupled with programmable gain
- 0.4 MHz to 200 MHz analog input bandwidth (–3 dB)
- –18 dBm to 4 dBm full-scale input
- 75.78 dBc SFDR at 70 MHz F_{in} (bandwidth = 50 MHz)
- Interchannel crosstalk insulation: –87 dB at 70 MHz F_{in} (minimum to maxmum gain)

DAC module

Add-on module for VHS-DACs and VHS-ADCs

The DAC module is a high-speed, multichannel digital-to-analog conversion add-on module for VHS-DACs and VHS-DACs. The module is equipped with eight phase-synchronous DACs operating at a maximum refresh rate of 480 MSPS using on-chip interpolation. The DAC channels are identical to those of VHS-DACs and VHS-ADCs, and offered with the same analog coupling output options. When installed on VHS-DACs or VHS-ADCs, all the channels are tightly phase synchronized to the same clock reference. To better understand this information, refer to the VHS-DAC and the VHS-ADC.

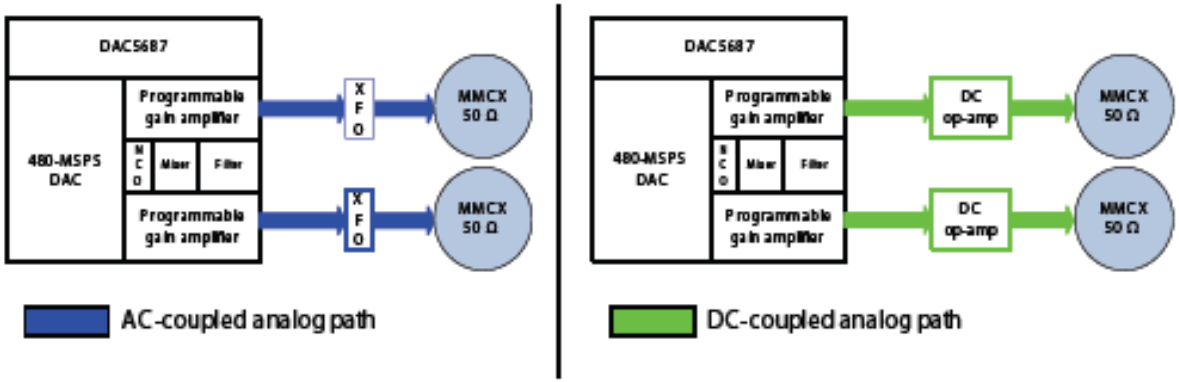
At a glance

- Eight, 14-bit, 480 MSPS, digital-to-analog conversion channels
- Outstanding clock synchronization

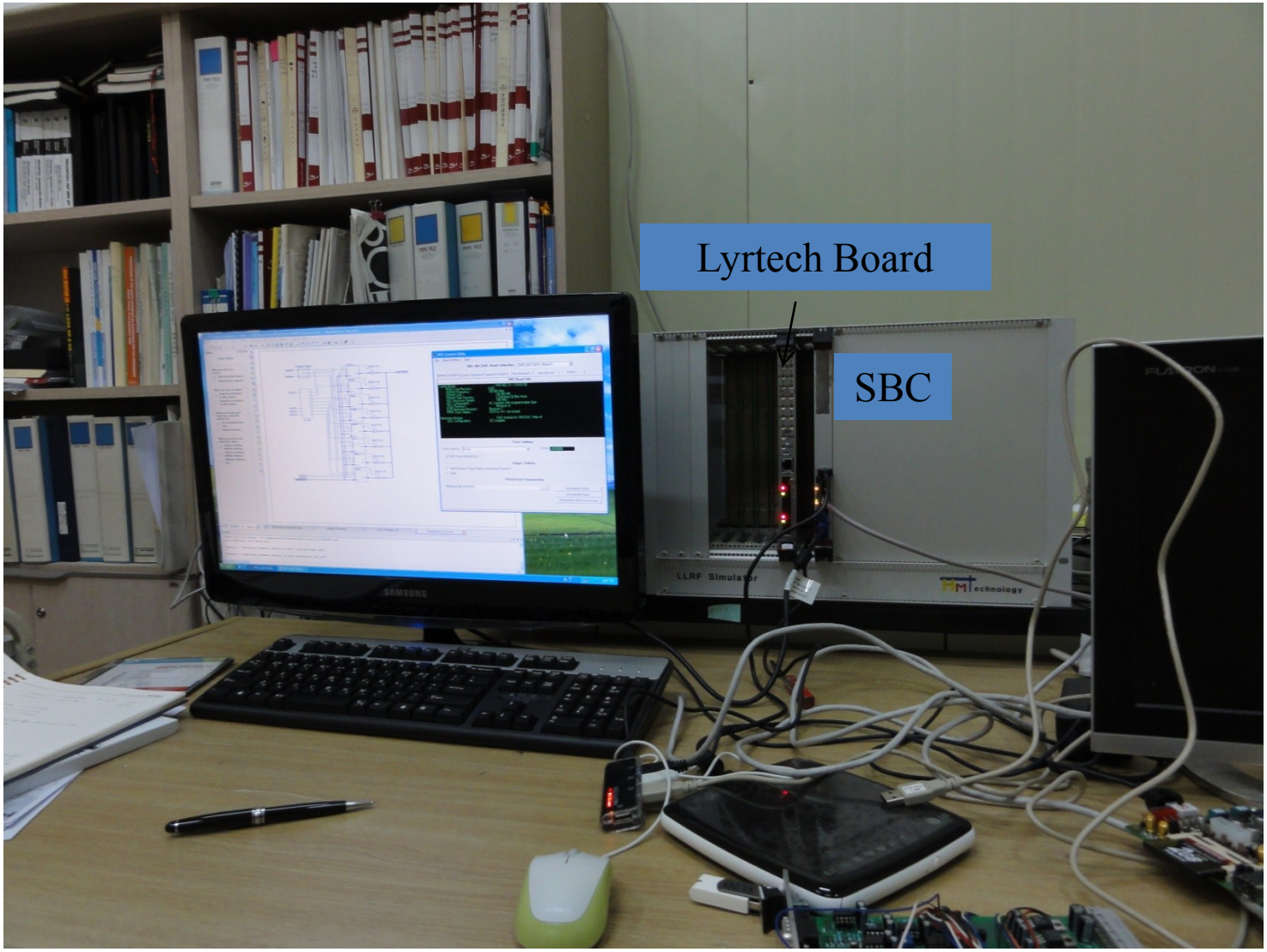
Hardware options

The DAC module has the following optional hardware packages:

- AC-coupled I/Os—features AC-coupled D/A channel output analog paths
- DC-coupled I/Os—features DC-coupled D/A channel output analog paths



Program Development using Xilinx ISE



Summary

1. Introduce the general concept for the control system
2. Cavity Modeling
3. Signal processing
4. CORDIC algorithm
5. IQ demodulator
6. PI controller
7. Digital Filters
8. IQ output
9. Local Oscillator
10. Digital Hardware system

Thanks for your attention

Any questions?