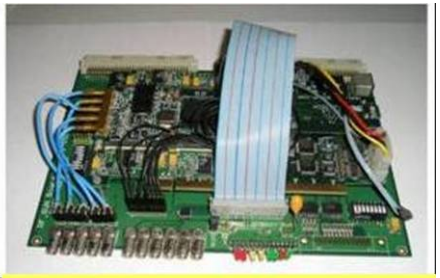
ILC LLRF Status

Ruben Carcagno, Brian Chase
(on behalf of the FNAL LLRF Working Group)
5/25/06

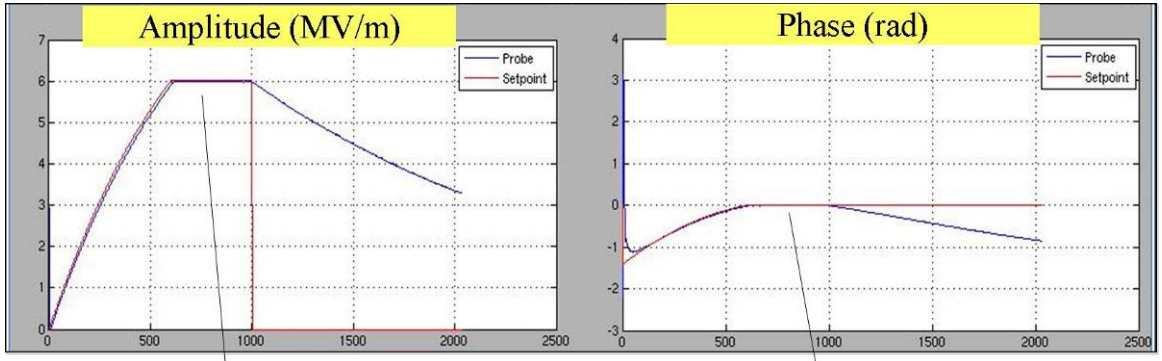
Outline

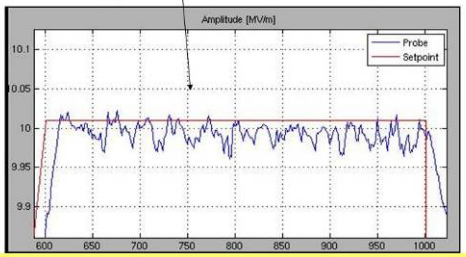
- Simcon 2.1 Testing at A0 with CC1
- Simcon 3.1 Testing at A0 and ILCTA_MDB with CC2
- SNS System Testing at A0 and ILCTA_MDB with CC1 and CC2
- Piezo Tuner Testing at ILCTA_MDB with CC2
- Simcon 3.1 Noise Characterization
- ILC Cryomodule Simulator
- ILC RF Unit Block Diagram
- Master Oscillator, 3.9 GHz Up/Down Converter, 32-Ch Field Controller Module (B. Chase)
- Next Steps

Simcon 2.1 Testing at A0 with CC1 (3/05 to 12/05)

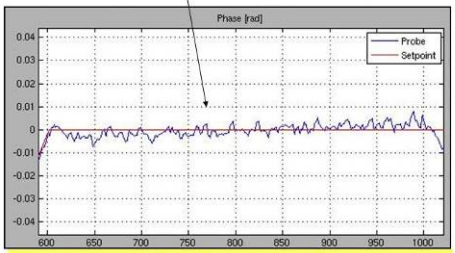


Simcon 2.1 board





Zoom on the flat top amplitude:
RMS Noise ≈ 0.07%



Zoom on the flat top phase:
RMS Noise ≈ 0.2°

Drive Vector Modulator and Downconverter
Vector Modulator/Mixer (New FNAL design, upgradeable to 3.9 GHz operation)

VME Modules:

-Sparc CPU-56 running DOOCS and Matlab

-8-Ch Timer Module (FNAL design)

-8-Ch, 10 MHz fast digitizer (DESY design)

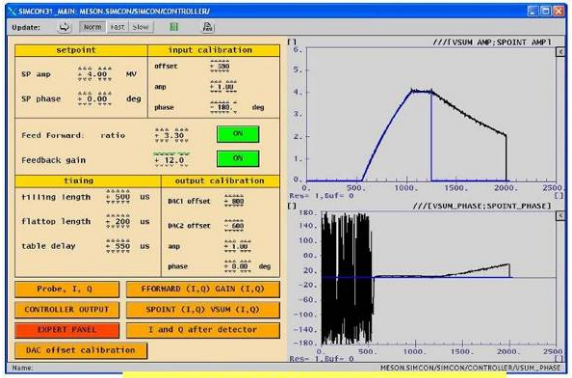
-8-Ch Function Generator board (DESY design)

-Simcon 2.1 FPGA board (DESY design + commercial FPGA board)

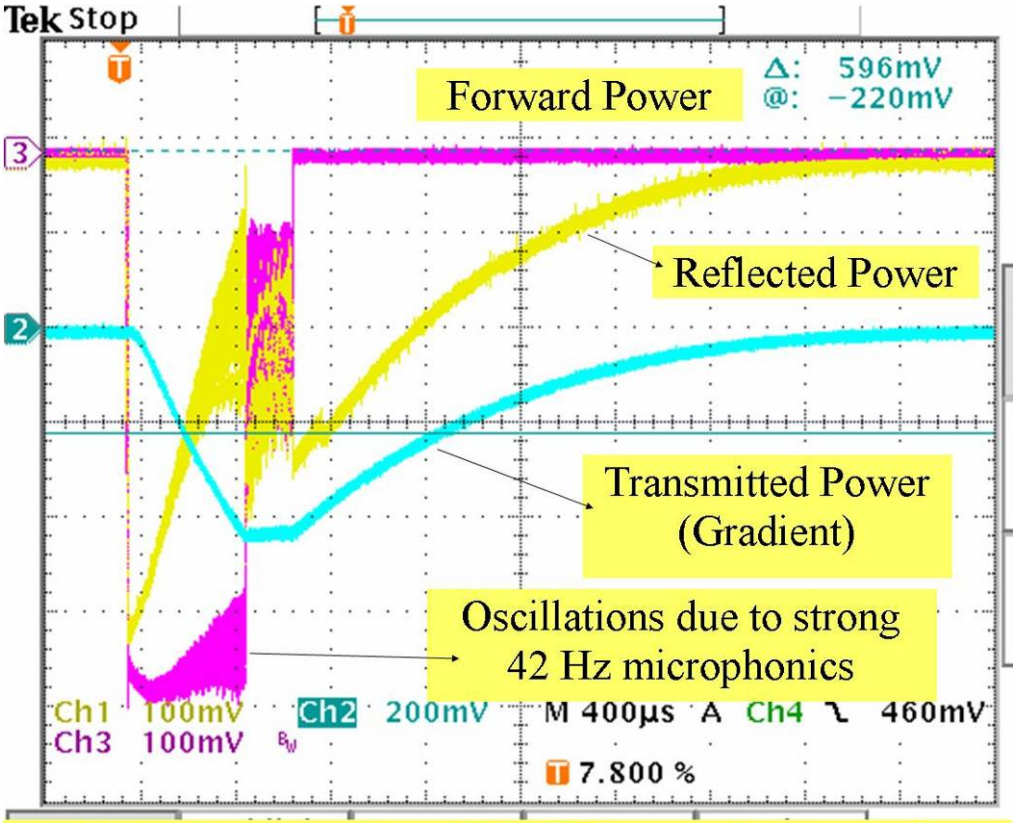
Stand-alone LLRF System

Simcon 3.1 Testing at ILCTA_MDB with CC2 at 4.5 K (3/06)

Simcon 3.1 board



DOOCS Interface

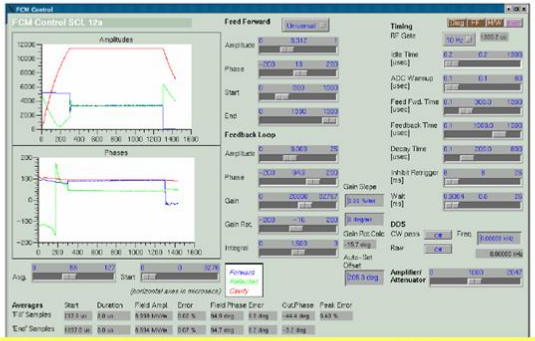


30 RF pulses over plotted: LLRF system keeps gradient steady under presence of strong microphonics

SNS LLRF System Testing at A0 and ILCTA_MDB

An 805 MHz single-cavity SNS LLRF controller unit was modified for 1.3 GHz cavities and shipped to Fermilab. The system was successfully tested with CC1 and CC2.

SNS LLRF board

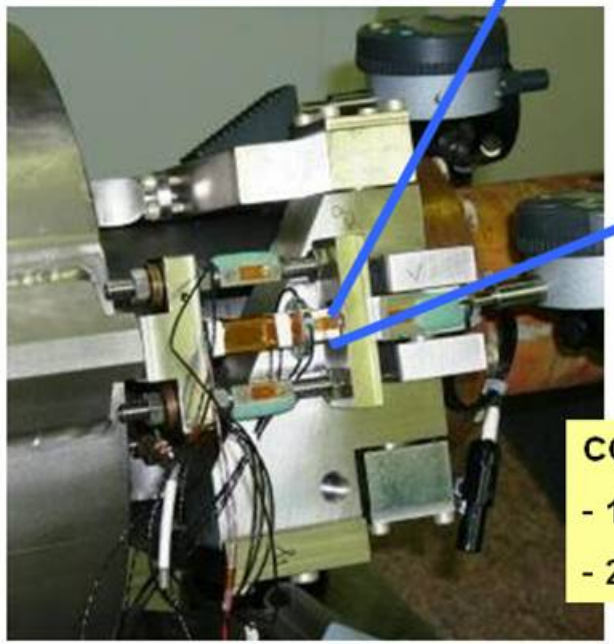


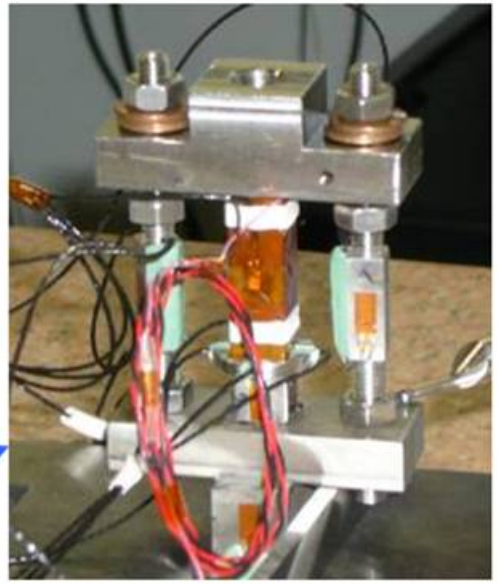
SNS LLRF EPICS-based interface

SNS LLRF System

Piezoelectric Tuner - CC2 Results at 4.5K

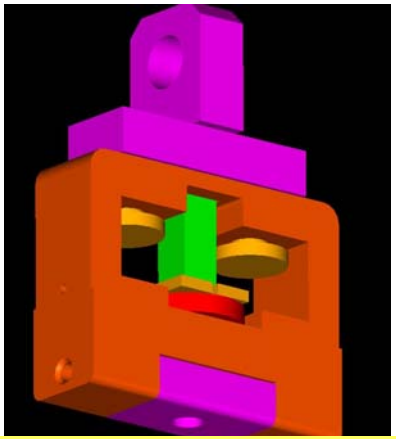
Calibrated "Bullet" Strain Gauge Sensor to measure preload changes during cooldown and stepping motor operation



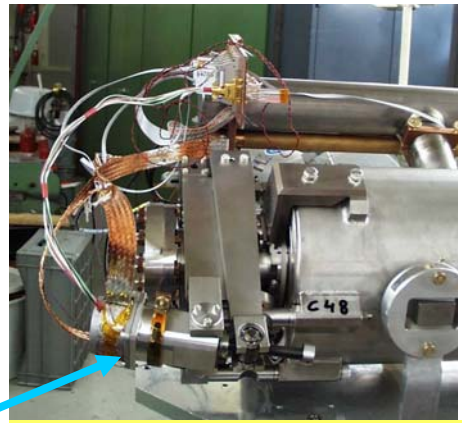


CC2 Piezo assembly instrumentation:

- 11 strain gauges
- 2 RTDs



New Piezo/Magnetostrictive Bracket Design



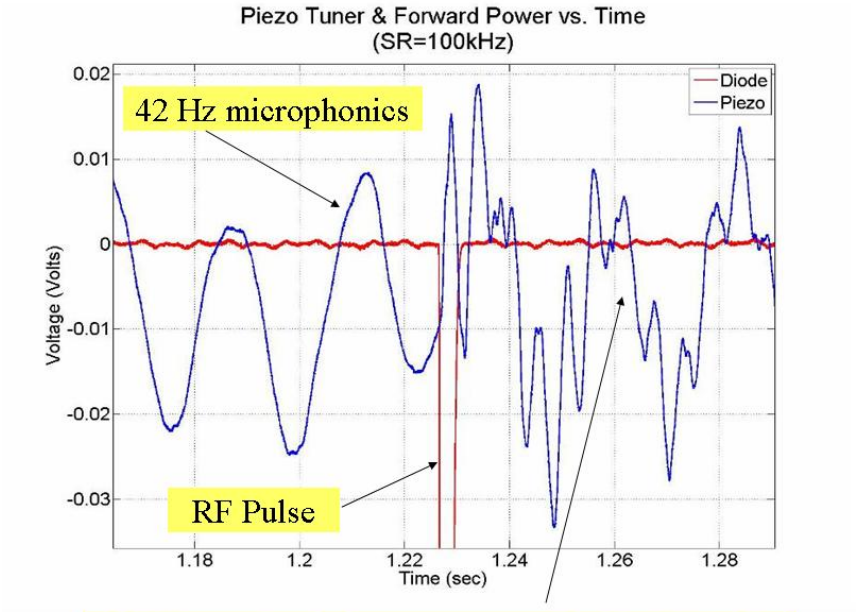
Stepping Motor

CC2 Tuner

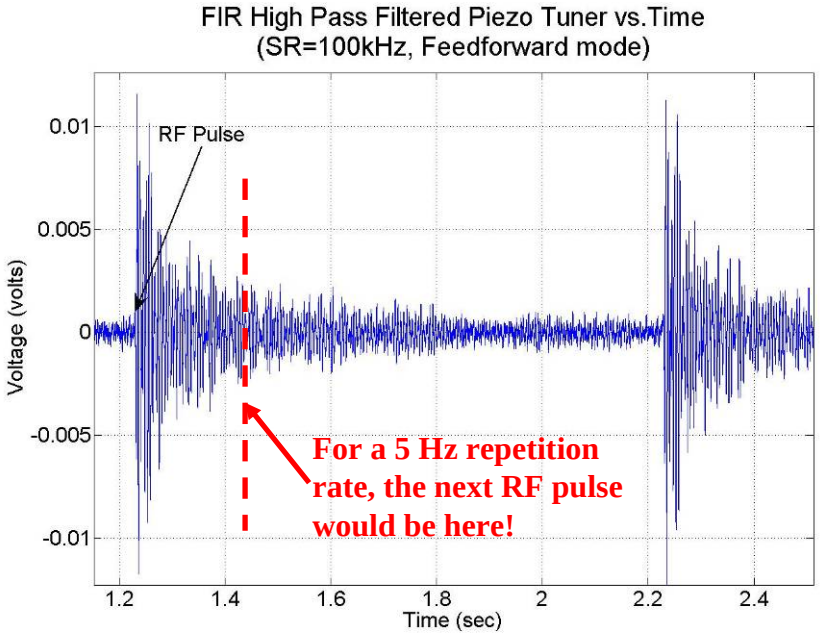
Piezoelectric Tuner - CC2 Results at 4.5K

Piezo as a Vibration Sensor

Piezo as a vibration sensor around an RF Pulse



180 Hz mechanical resonance excited by RF pulse

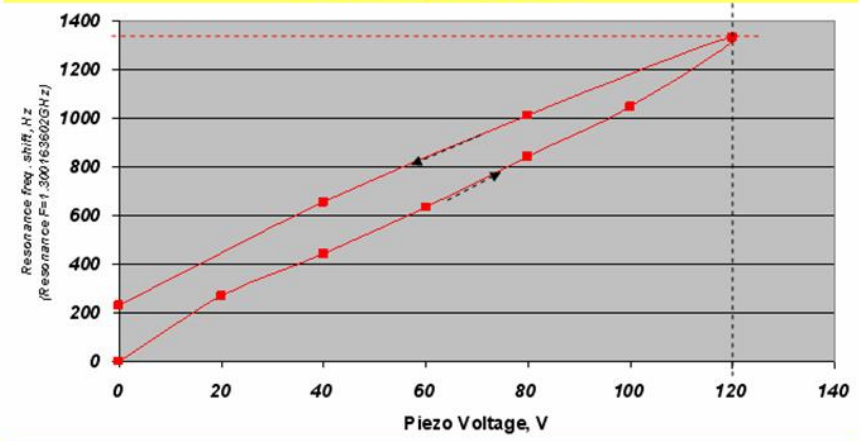


The Piezo Tuner data is filtered with a high pass FIR filter to remove <150Hz noise. The decay of the 180Hz cavity vibration after the RF pulse is ~0.7sec.

Piezoelectric Tuner - CC2 Results at 4.5K

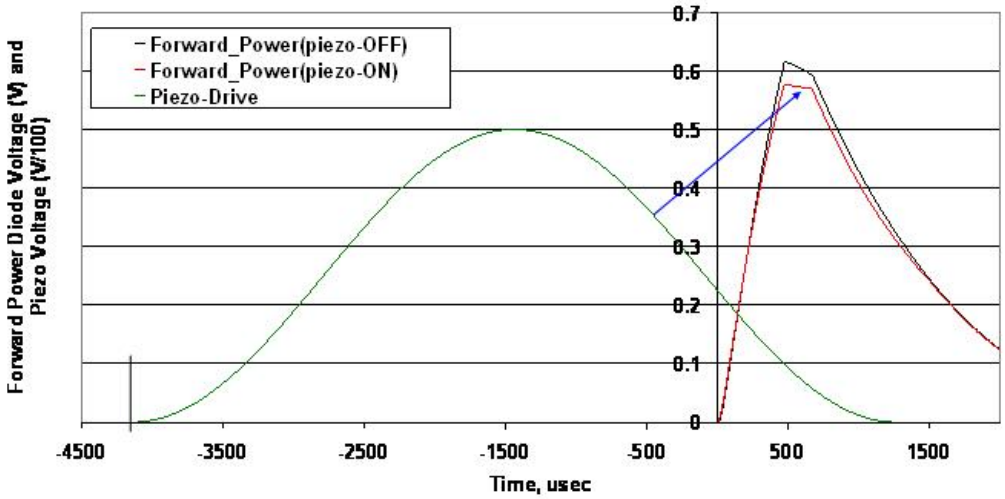
Piezo as an actuator

Static Operation



Static Tuning Range ~ 1.3 KHz

Pulsed Operation

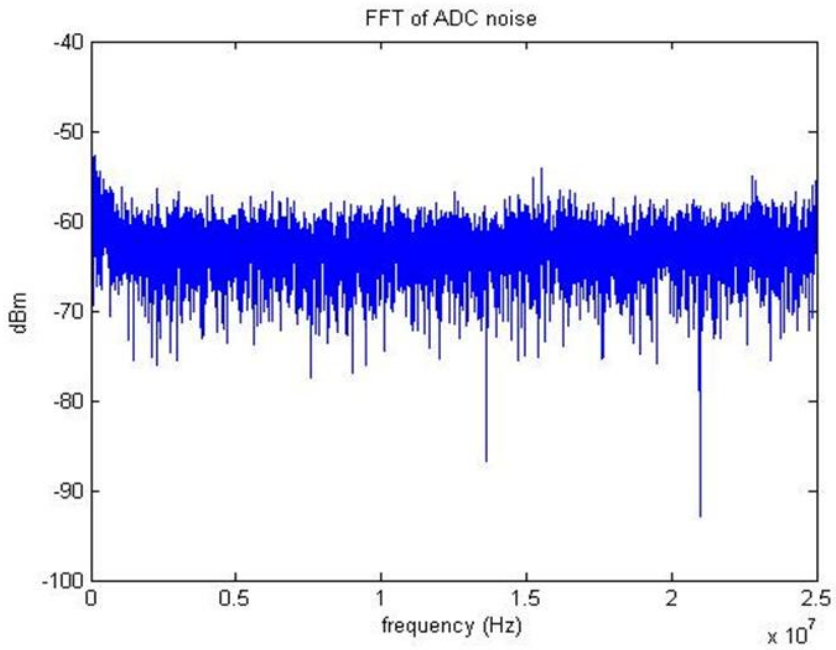


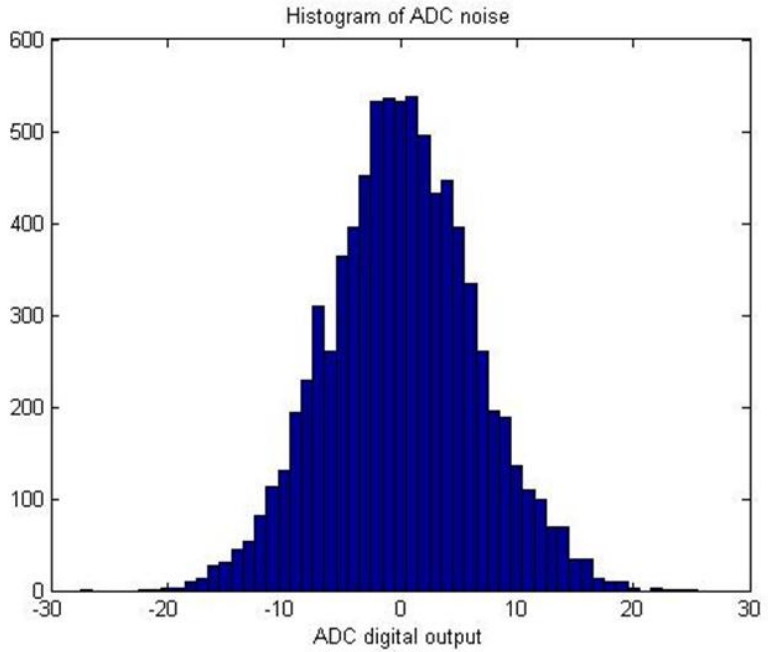
By pulsing the piezo, and manipulating the pulse amplitude, frequency, and phase, it was possible to approximately correct for the artificial flat top detuning

Simcon 3.1 Noise Characterization (Gustavo Cancelo)

Types of noise measurements:

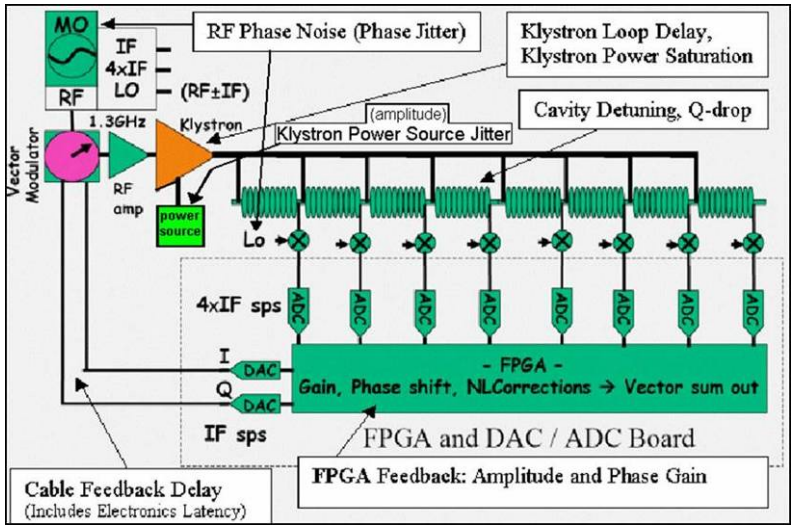
- Environmental noise
- Analog ground plane noise
- Power supply noise
- ADC and associated front-end amplifier noise
- Clock jitter noise
- Phase noise





Example: ADC output noise with a single-tone 15 MHz input. Major source: DC/DC converter ripple powering the ADC front-end amplifiers

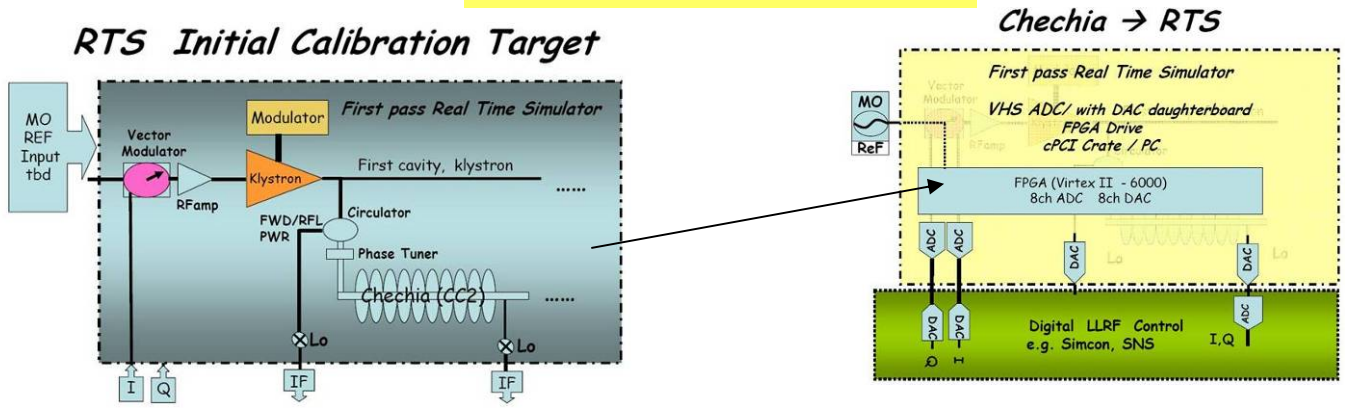
ILC Cryomodule Simulator
(In Collaboration with University of Pennsylvania)



Effects added to the simulation to date

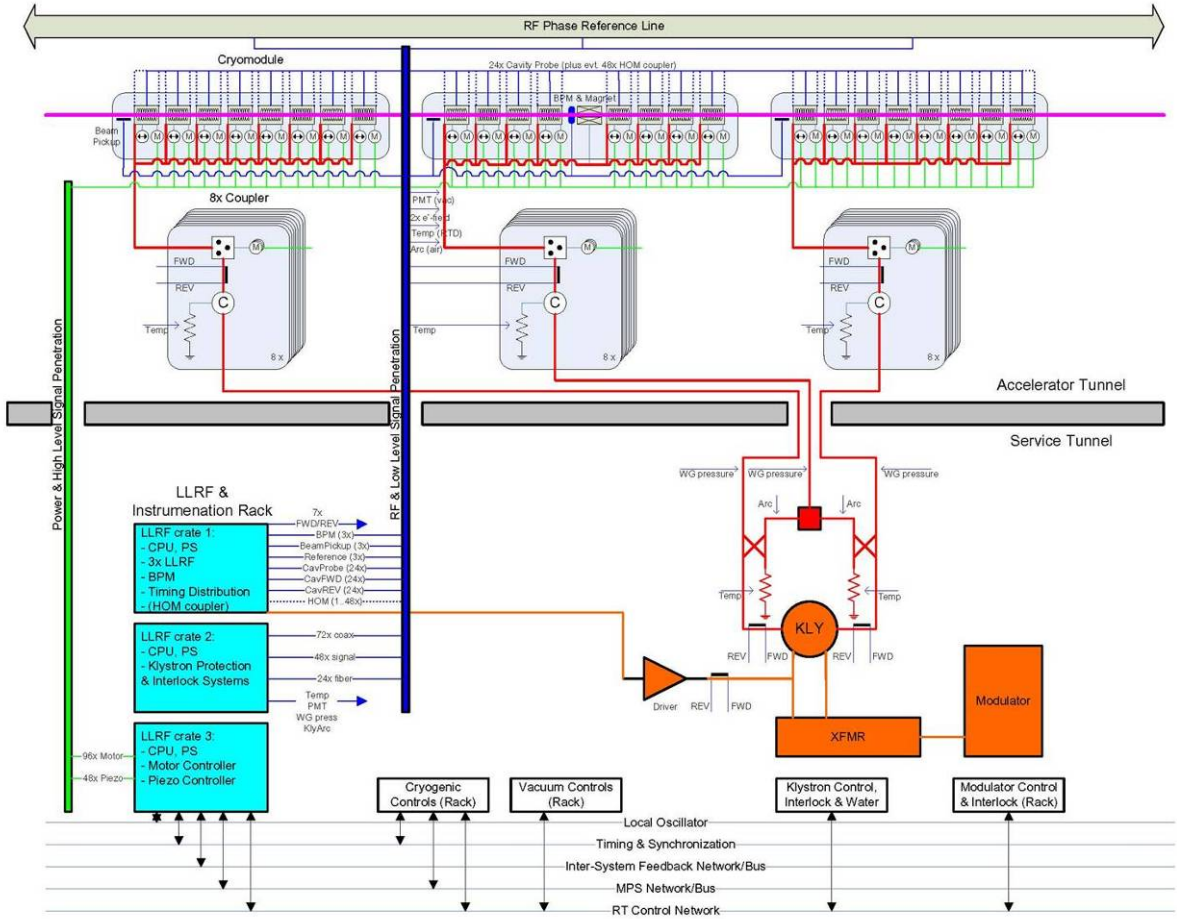
- Q-drop, Q-slope
- Beam Loading (pulsed DC)
- Klystron Power Source Jitter (e.g. Modulator)
- Klystron Power Saturation (no turn on curve)
- Klystron response time
- RF phase noise jitter from MO, fed to LO and cavity
- Feedback Latency (Cable Delay, Electronics Delay)
- Feedback Gain

Real-Time Simulator

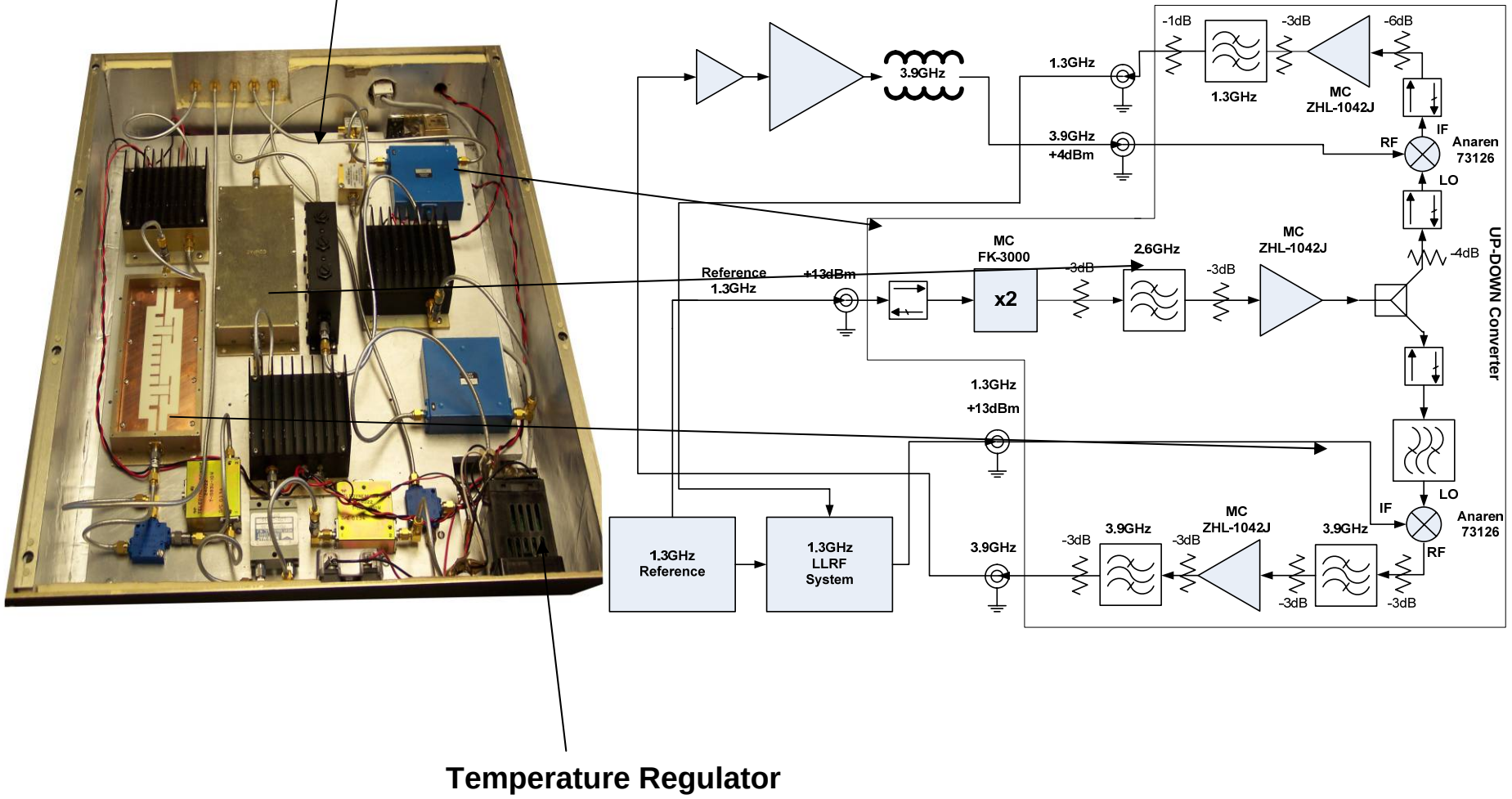


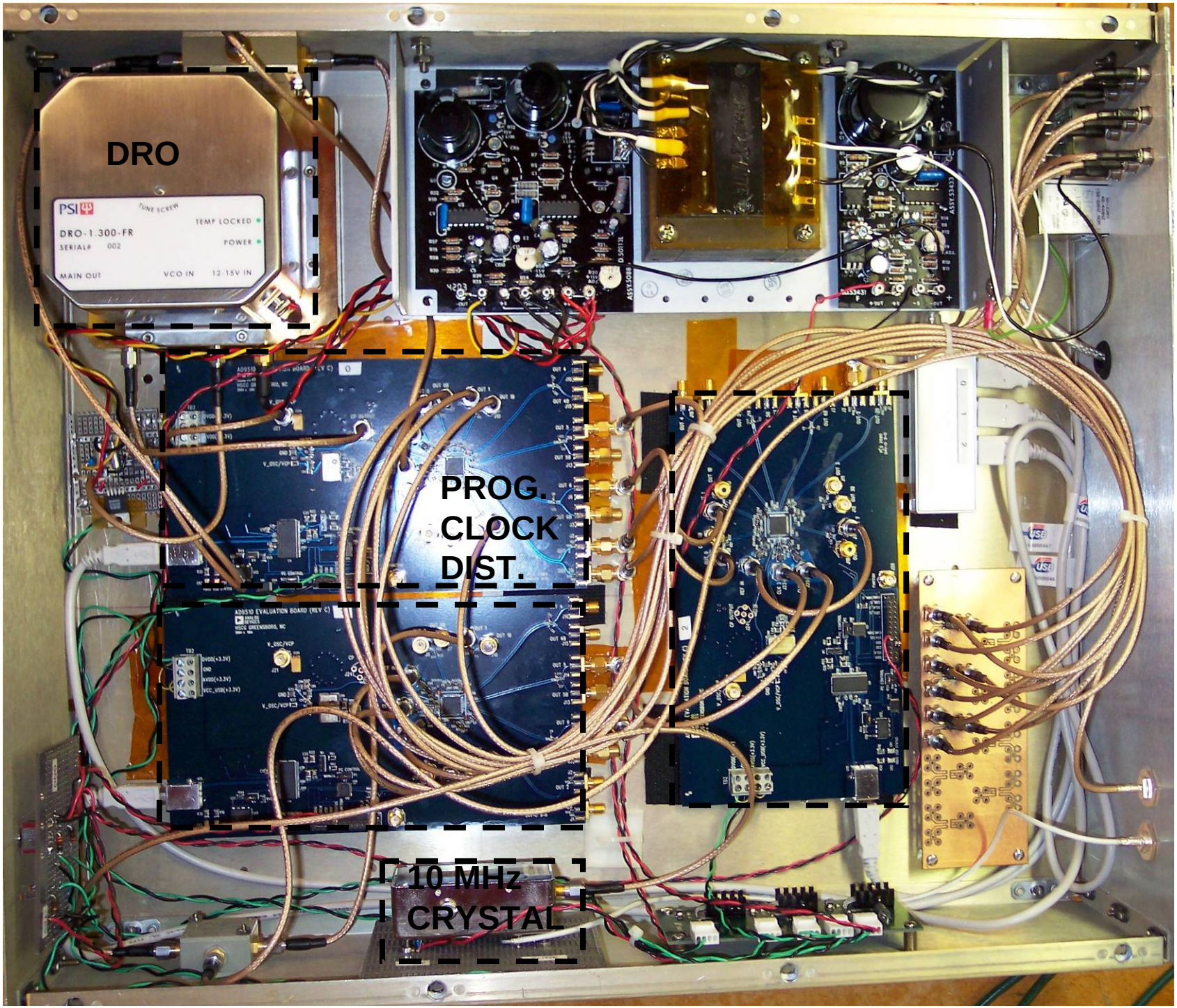
ILC Main Linac RF Unit

Baseline Design Block Diagram

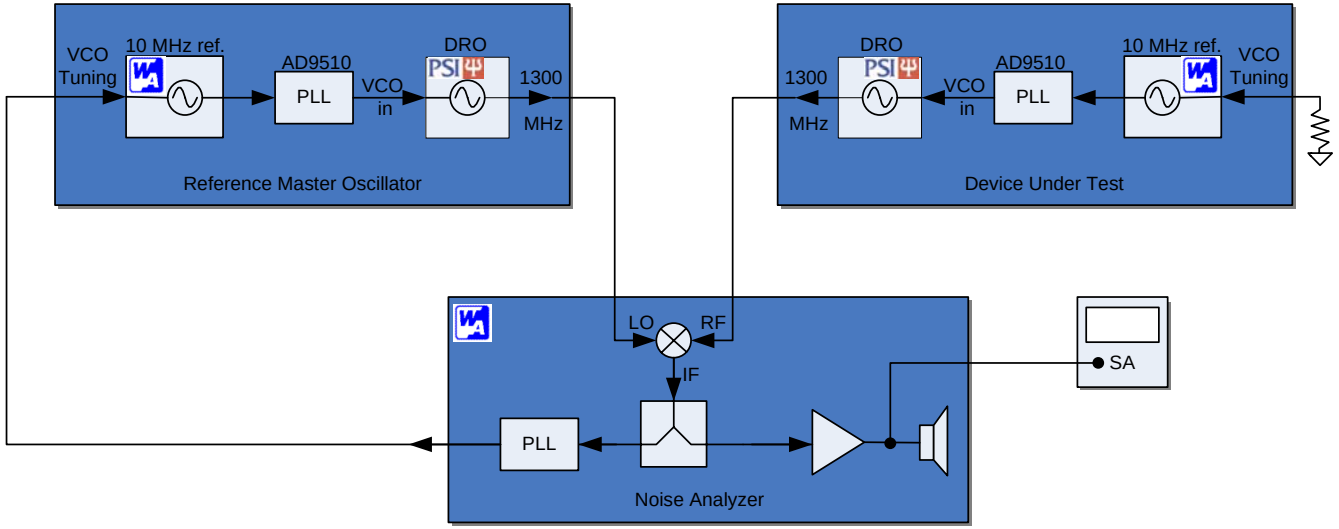


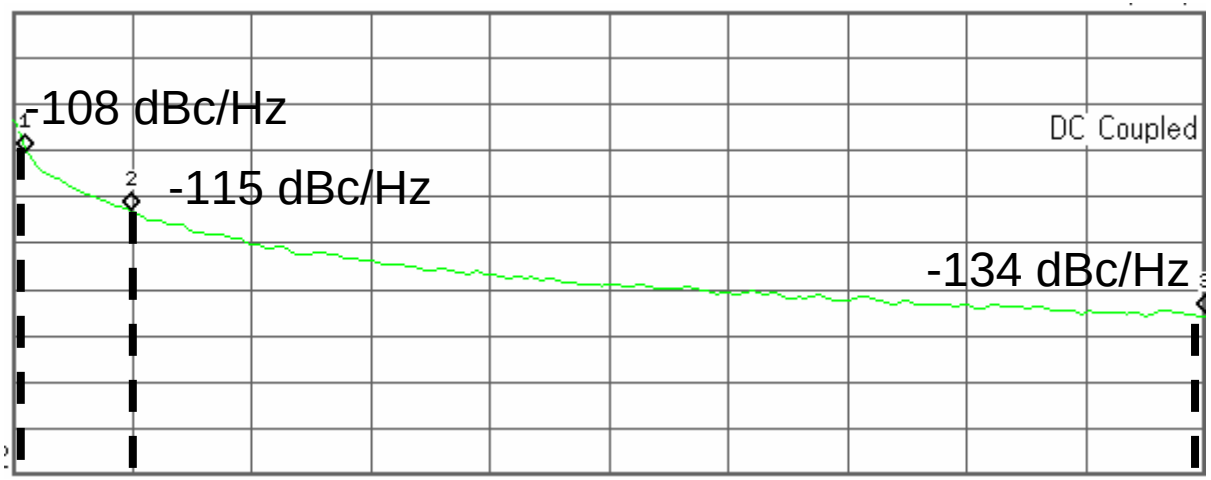
3.9 GHz Up/Down Converter




DRO
PSI
TUNE SCREW
TEMP LOCKED
DRO-1.300-FR
SERIAL# 002
POWER
MAIN OUT
VCO IN
12-15V IN
PROG.
CLOCK
DIST.
10 MHz
CRYSTAL

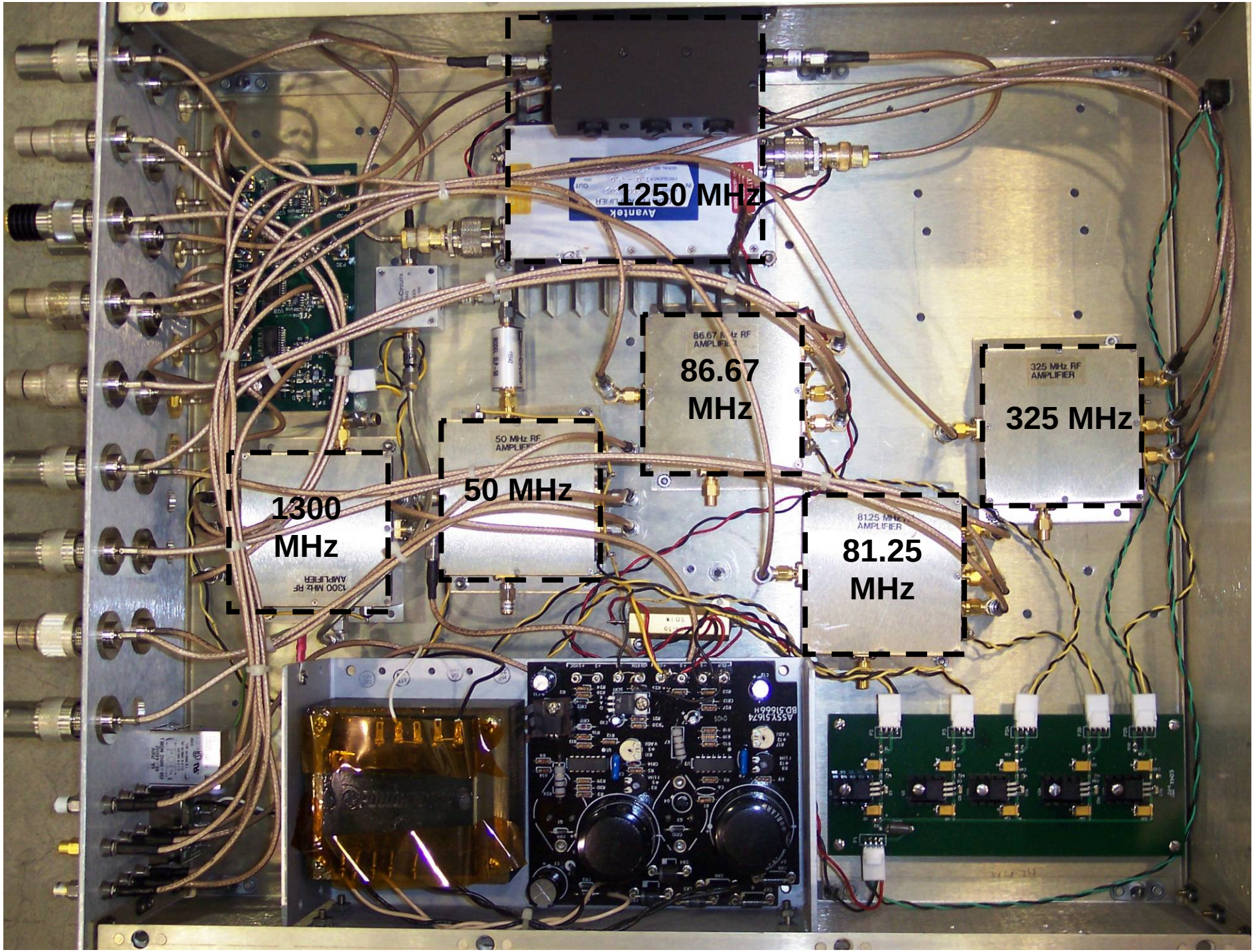
Master Oscillator Phase Noise Measurement





Absolute phase noise:

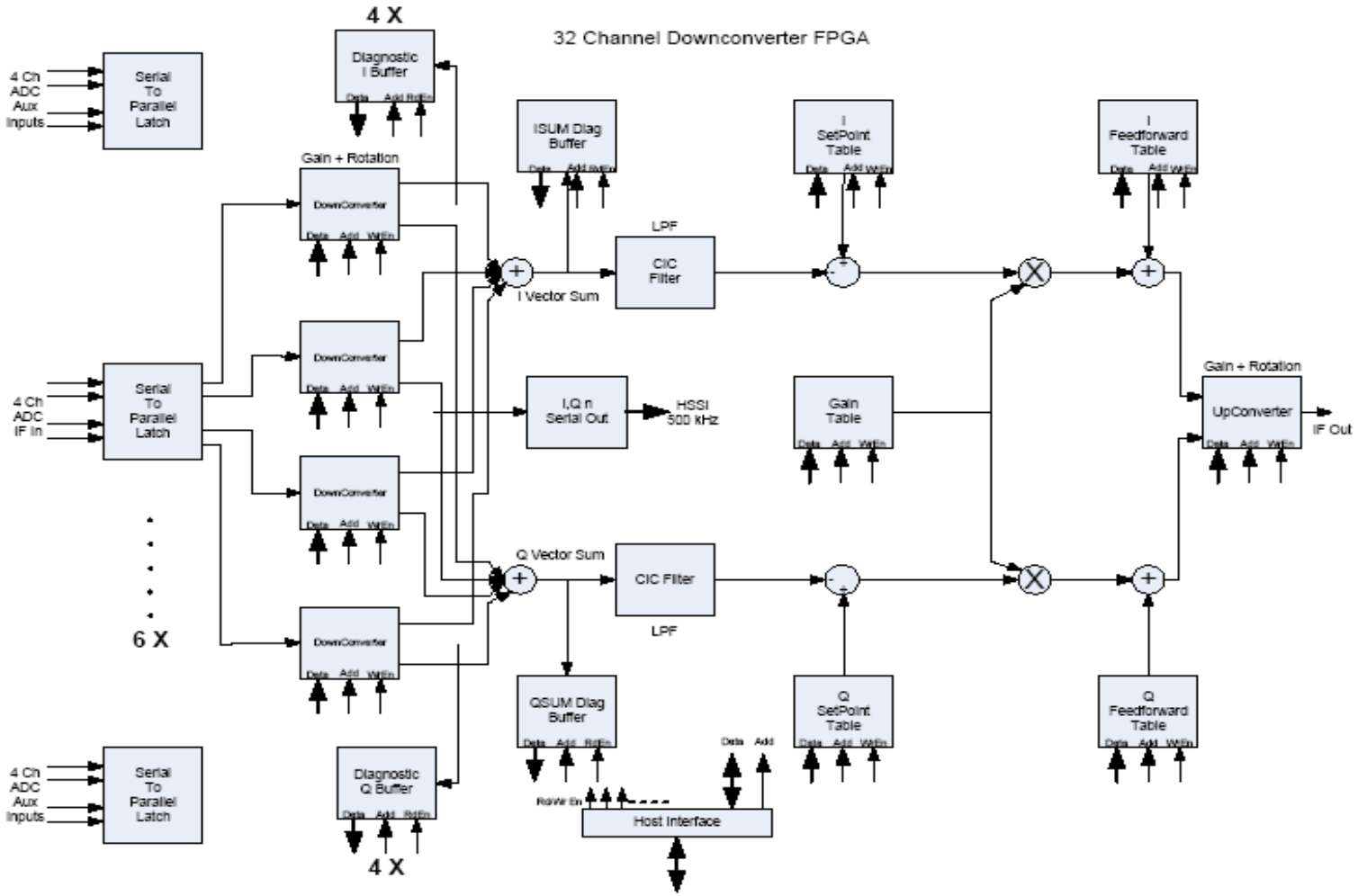
@10 Hz	-90 dBc/Hz
@100Hz	-108 dBc/Hz
@1kHz	-115 dBc/Hz
@10kHz	-134 dBc/Hz
@100kHz	-160 dBc/Hz


1250 MHz
86.67 MHz
50 MHz
1300 MHz
325 MHz
81.25 MHz

ILC Related LLRF Software Effort

- EPICS
  - IOC and GUI Interface to SIMCON 3.1 (Nicklaus)
  - State Notation Language for coupler processing (Nicklaus)
  - Interface for klystron interlock digitizer board (Joireman)
- DOOCS (Rechenmacher)
  - Working DOOCS server for SIMCON crate
  - Working PC/Linux DOOCS client for SIMCON board control
  - Linux VMElib and VME specific DOOCS software
- FPGA
  - Altera code for 32-channel digitizer (Chase/Varghese/Barnes)
  - Modifications to SIMCON FPGA (AD/TD/CD)

32 Channel Field Control Module Process Block Diagram



Next Steps

- Modify Simcon 3.1 firmware for higher Intermediate Frequency (IF). Benefit: reduce latency, improve performance. Develop and demonstrate Fermilab's capability to make substantial firmware changes to this system
- Minor modifications to Simcon 3.1 hardware design to improve Signal to Noise Ration (SNR) Performance
- Develop manufacturing capabilities of Simcon 3.1 improved boards to populate ILCTA
- Provide DOOCS and EPICS control interfaces to Simcon 3.1
- Continue Fast Tuner R&D (piezo, magnetostrictive)
- Continue long-term LLRF controller R&D for an ILC RF unit