Performance study of SPIROC2 chip on FEV 7 board

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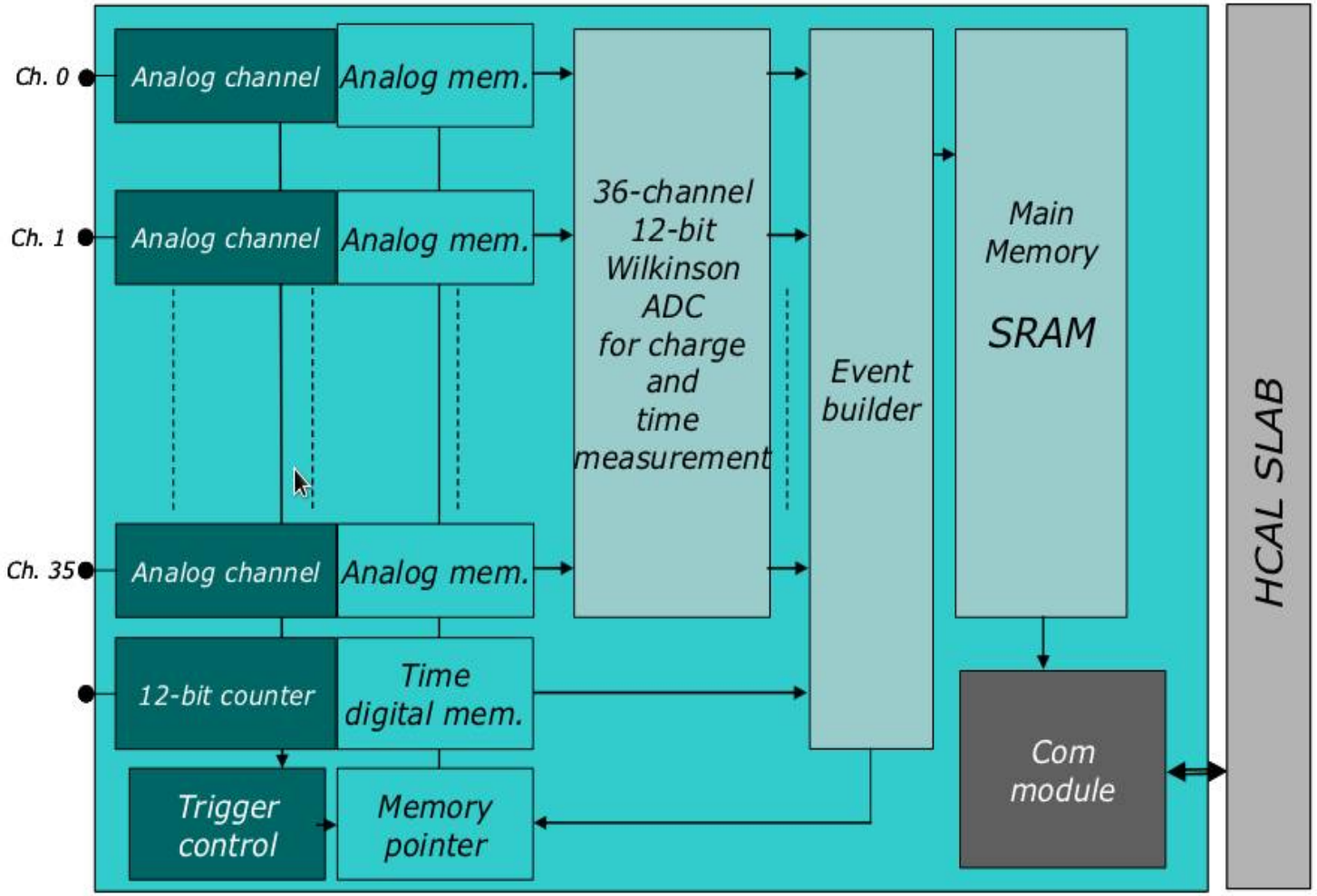
Main view of SPIROC

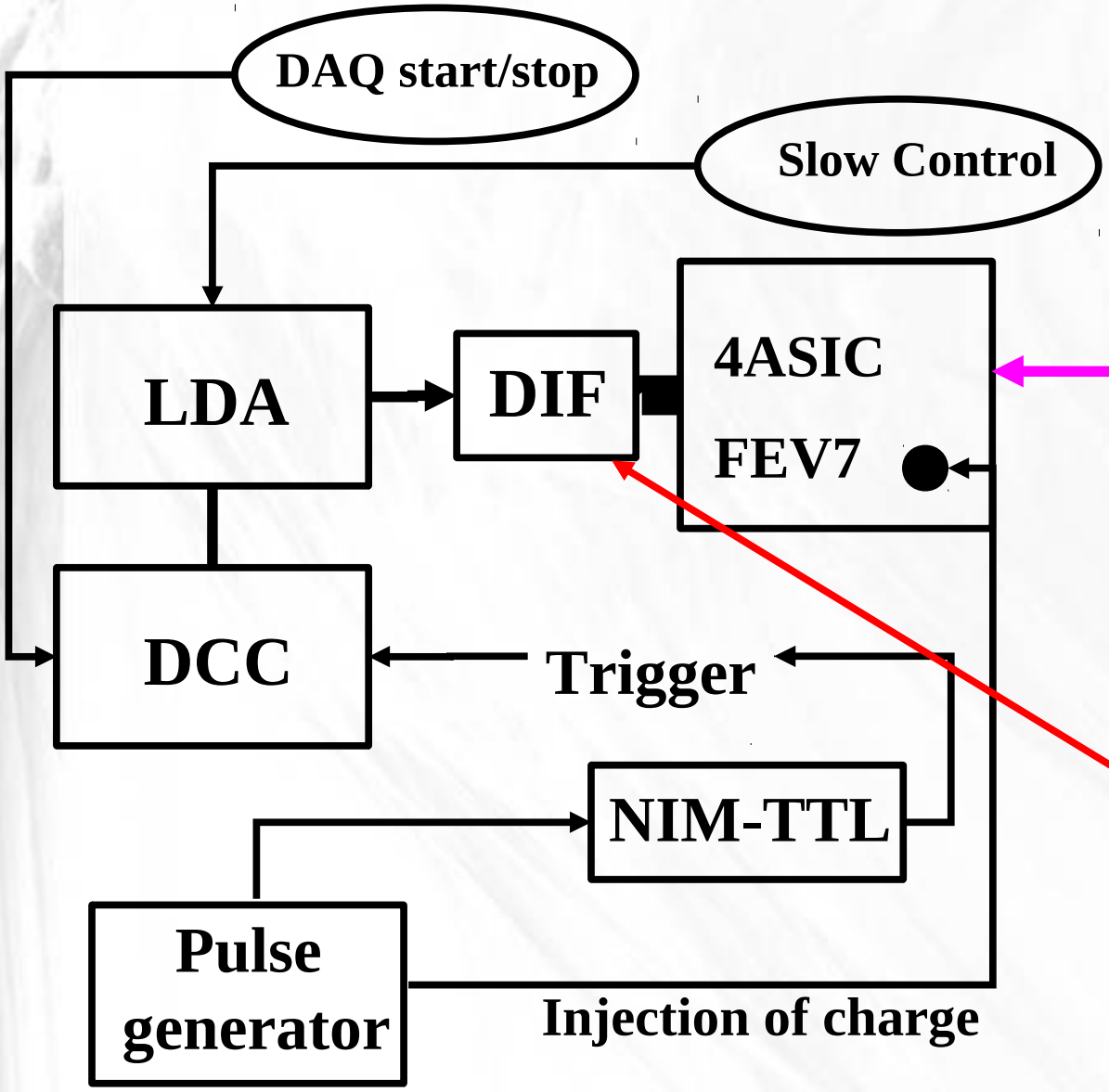
36 channel dual gain

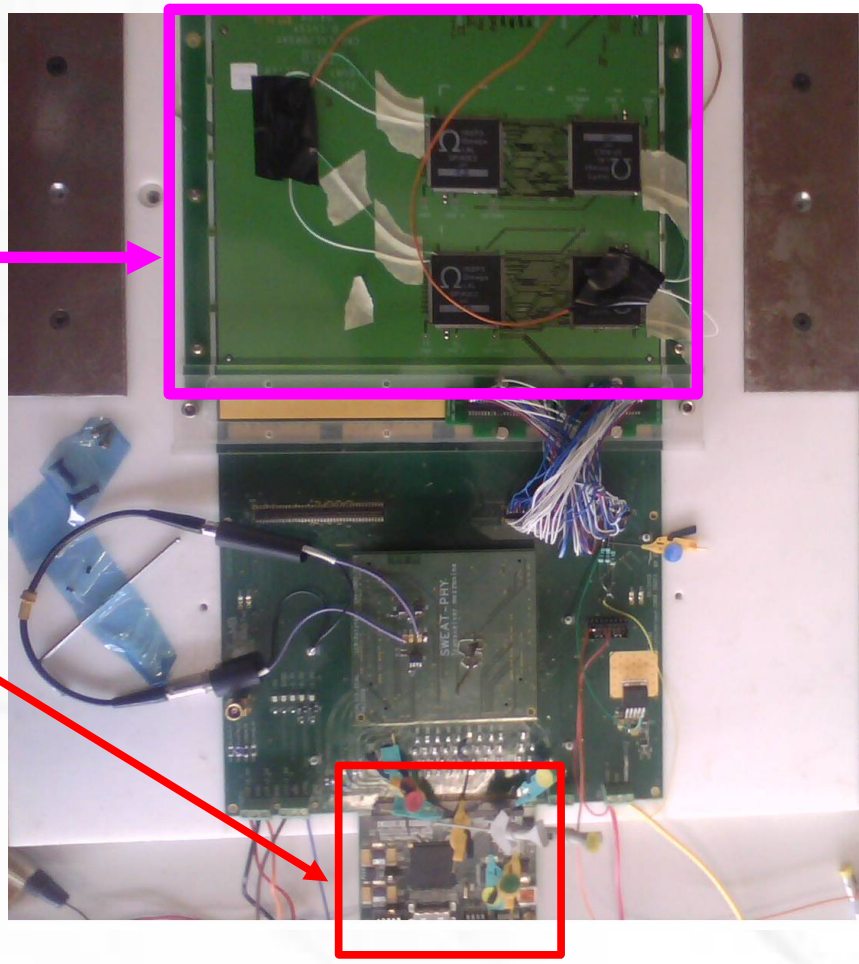
12 bit TDC

12 bit ADC



Test setup with injected charge





SPIROC memory mapping

Charge => 36 channel

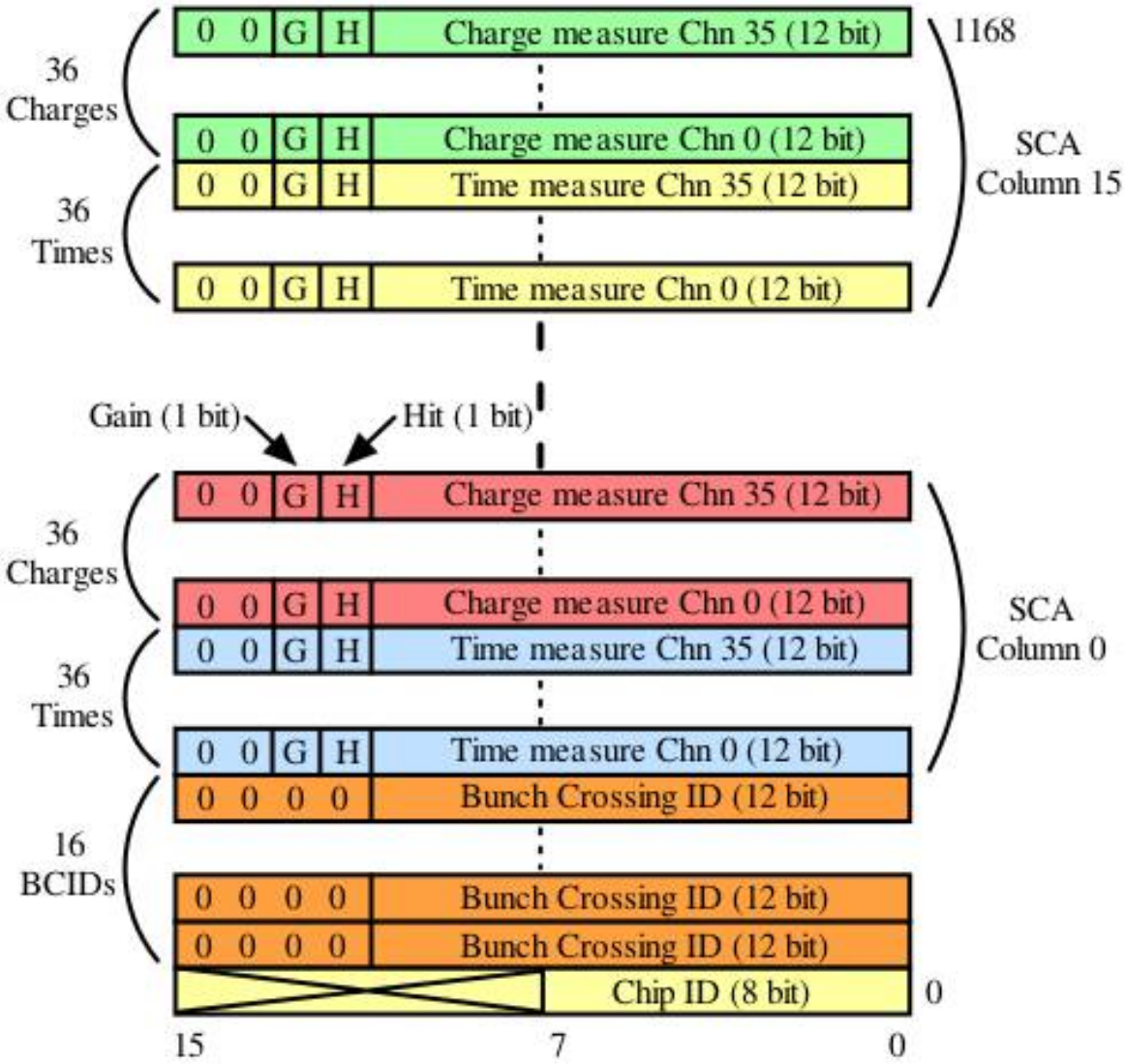
Time => 36 channel

16 bcID

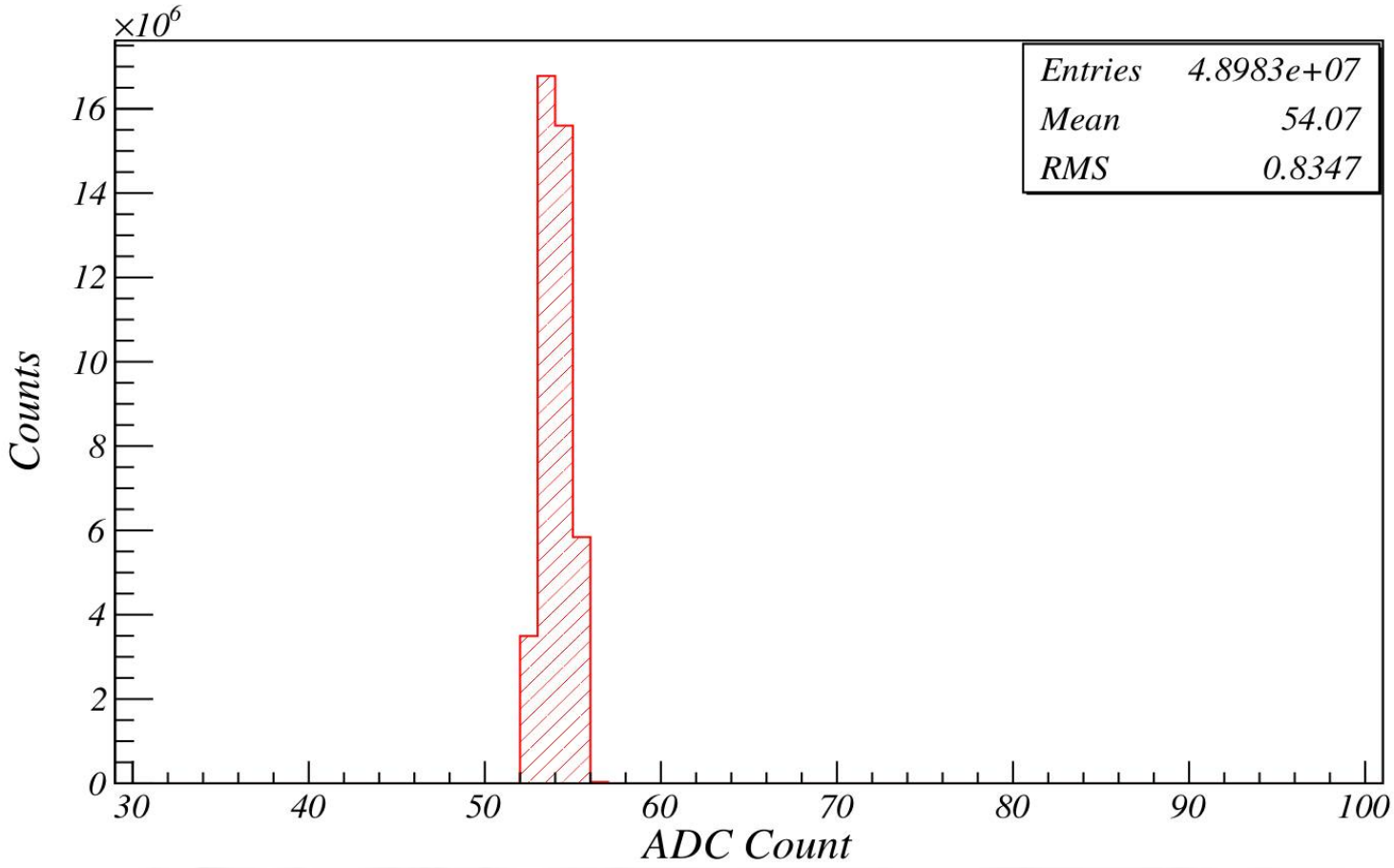
example, 16 bit BCID

0127
0562
0FA0
08A1
0262
0C25
0AEC
01AF
076B
0F28
09F9
02BE
047D
0A34
00F6
07B3
00AA

ChipID

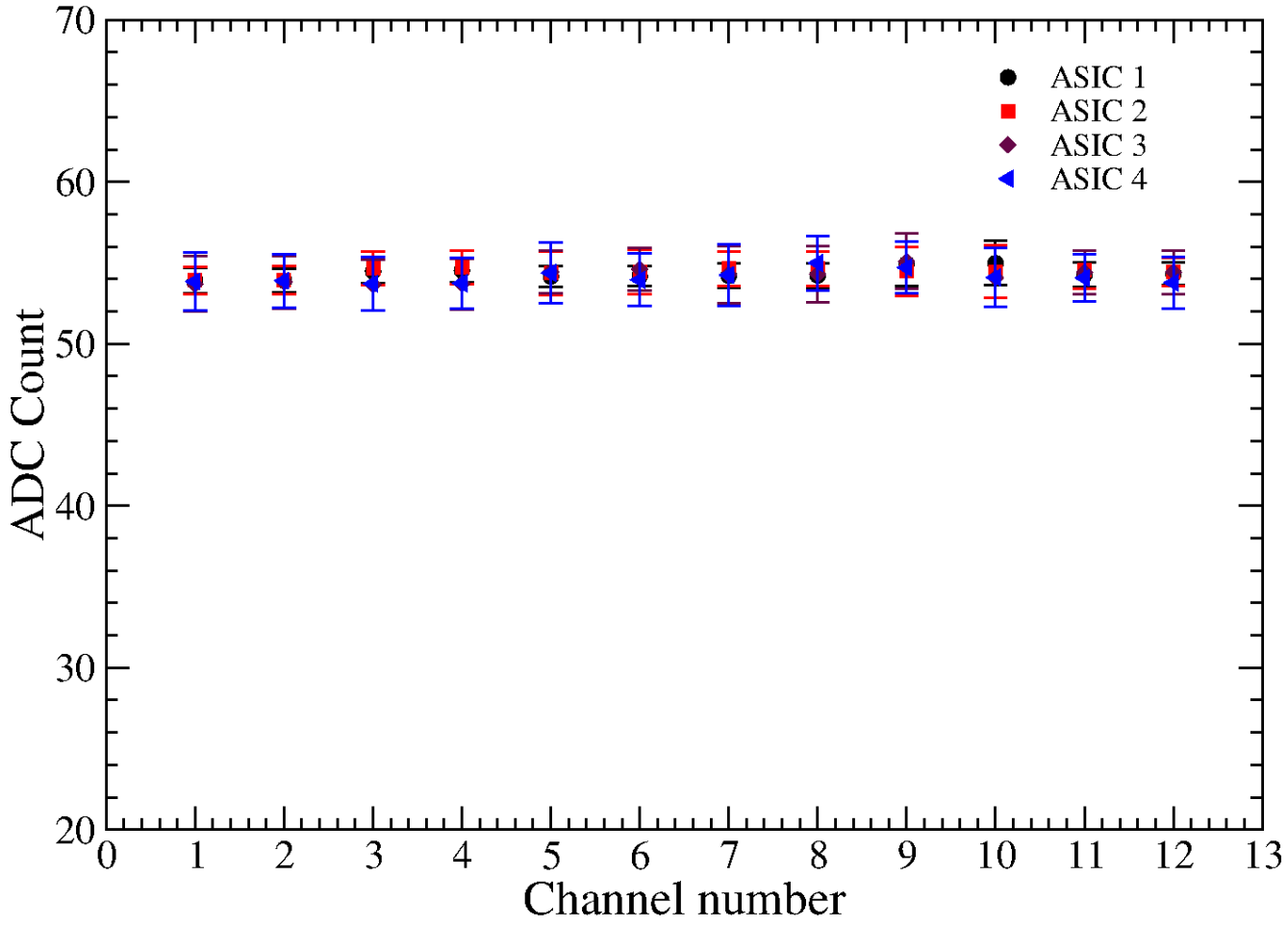


PEDESTAL measurement



Pedestal for 1 channel in one ASIC, the mean value is around 54 ADC Count or 1.2 MIP (1 MIP = 45 ADC Count)

PEDESTAL measurement



Slow Control

12 channel,

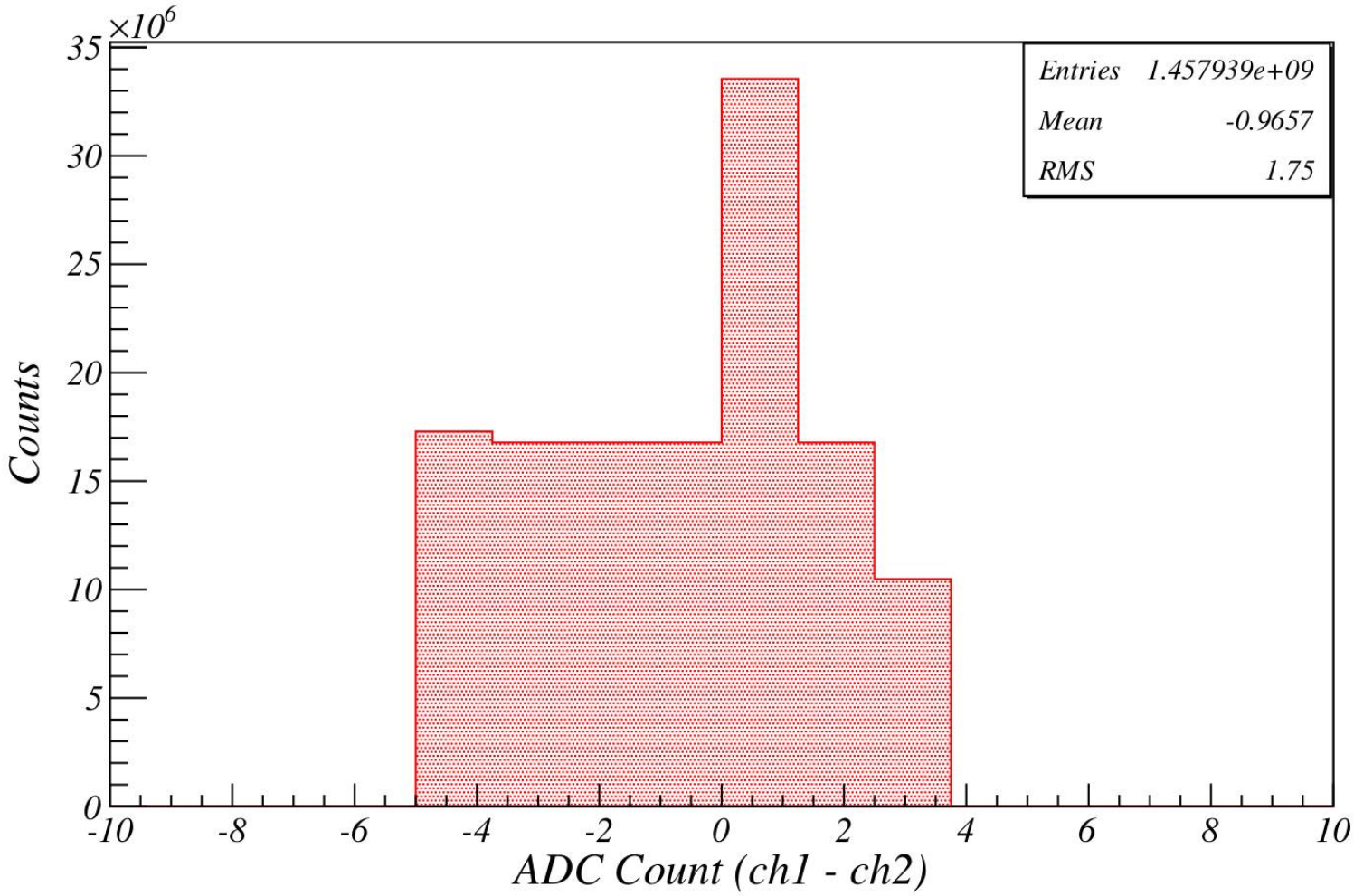
high gain enabled,

only charge

Pedestal for 4 ASIC and each has 12 channel (*example*)

The mean value is the almost same for 12 channel

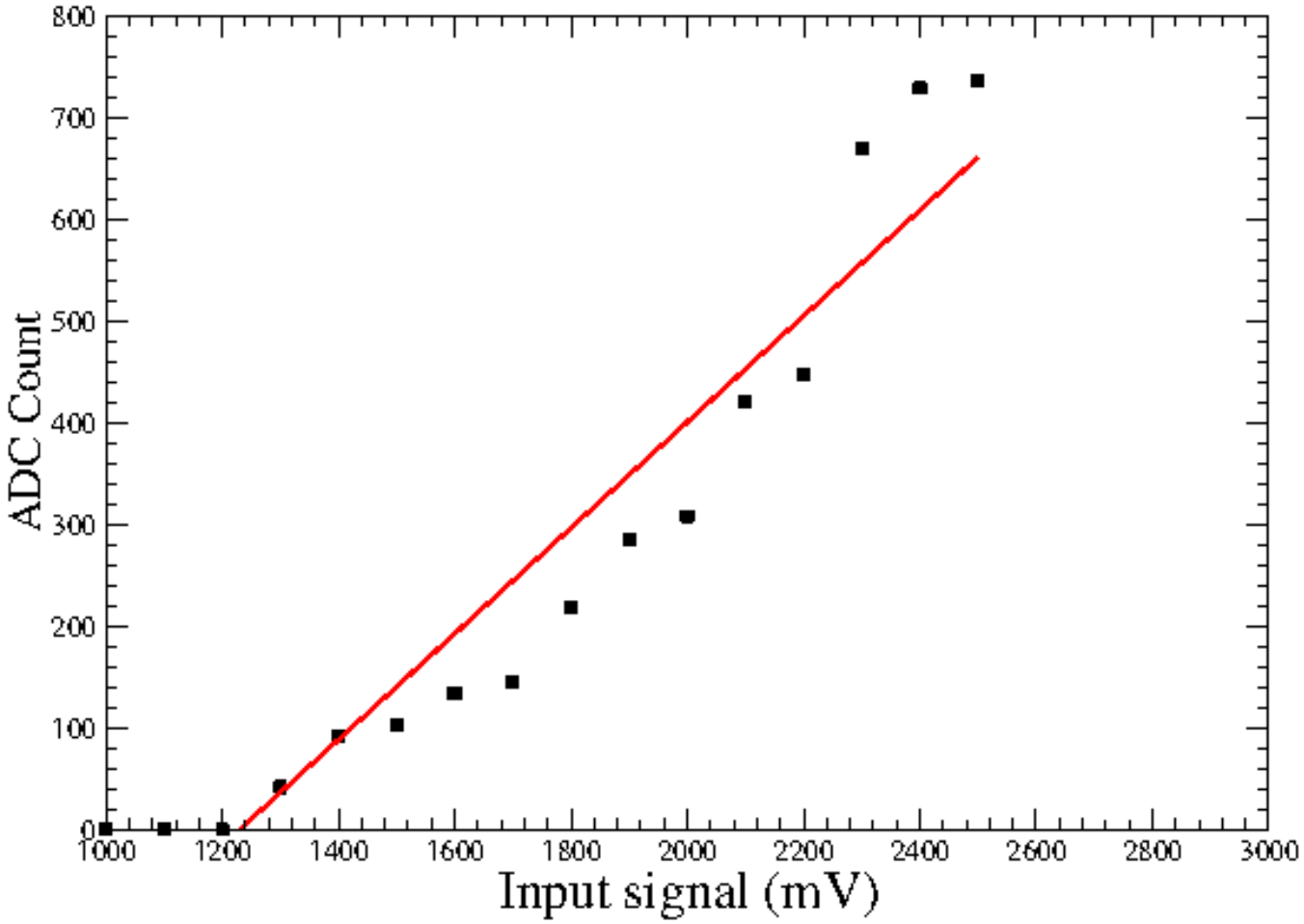
PEDESTAL measurement



Pedestal difference between two channel in one ASIC.

The difference < 10 ADC Count

ADC calibration test

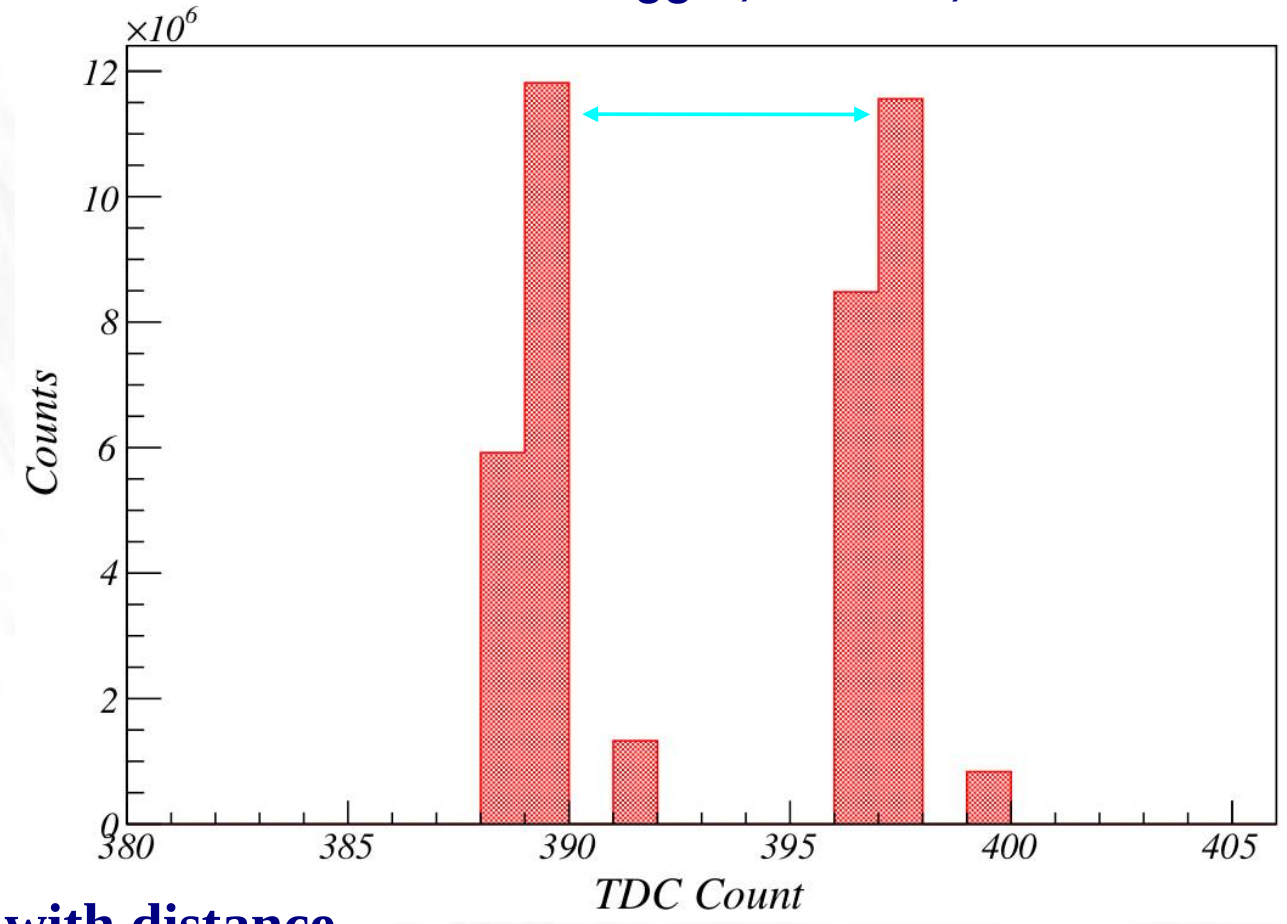


Not ideal linearity, but ADC functional for different injected charge

TDC performance

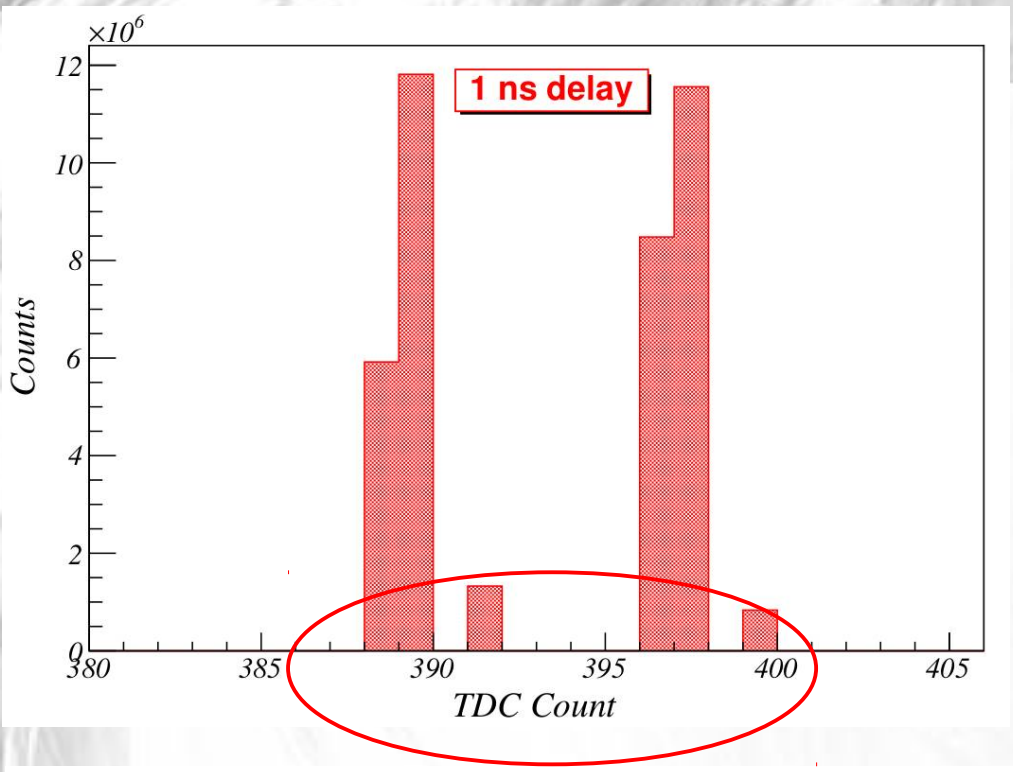
TDC slow control file:

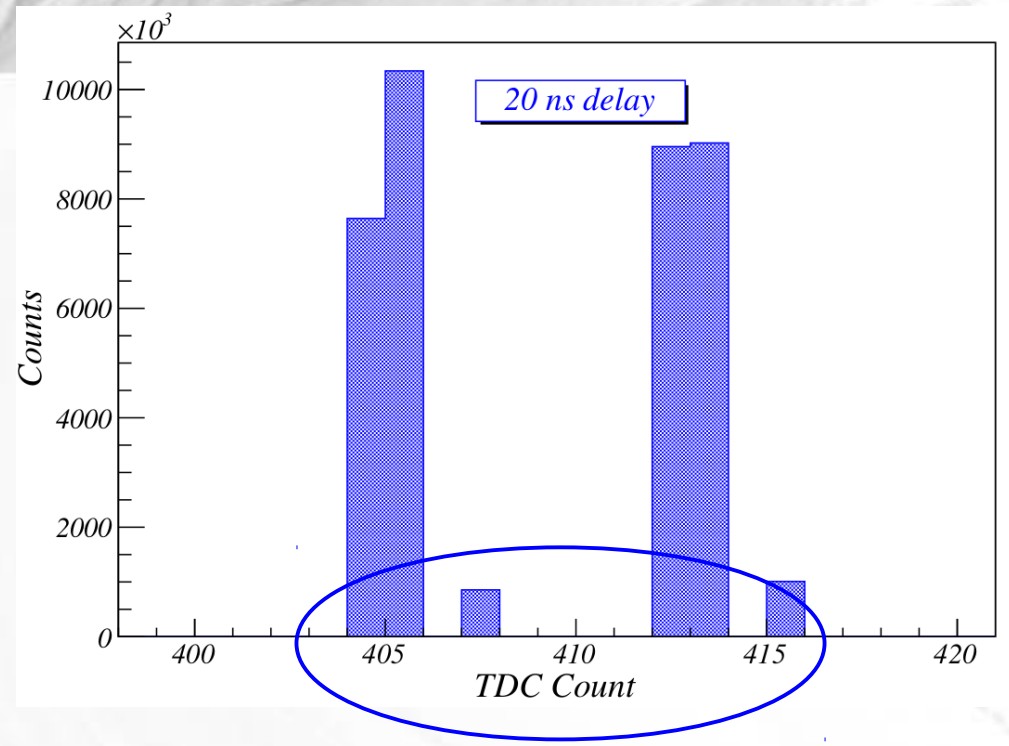
External trigger, hold ext, all channel enabled

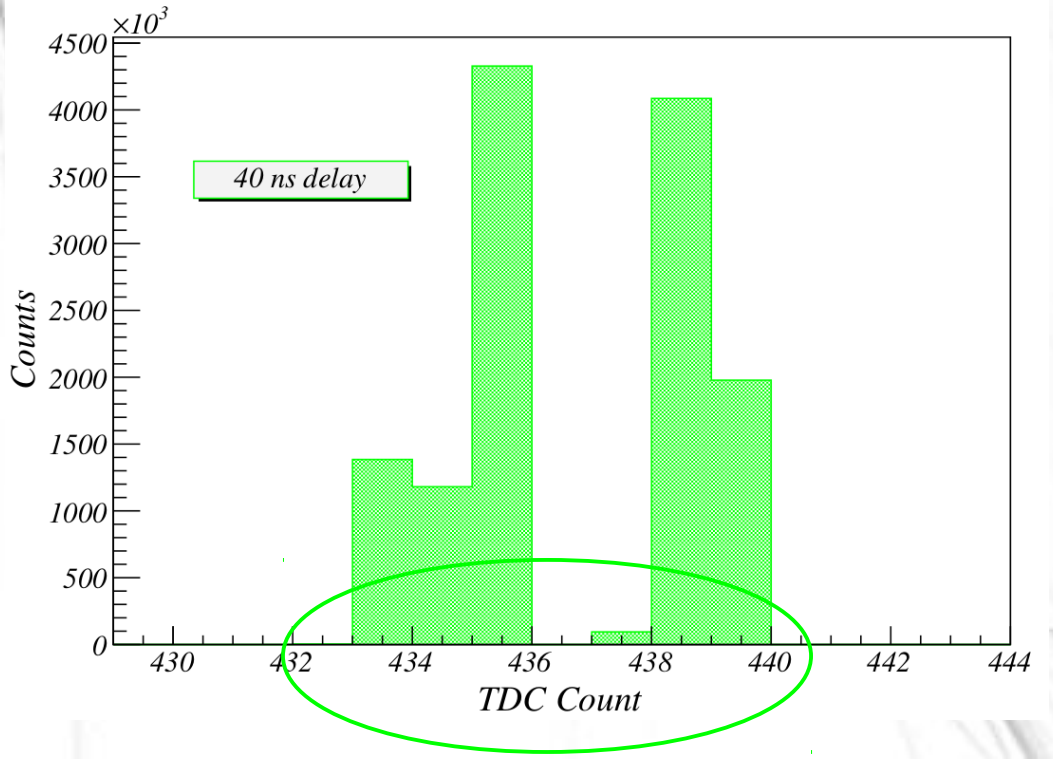


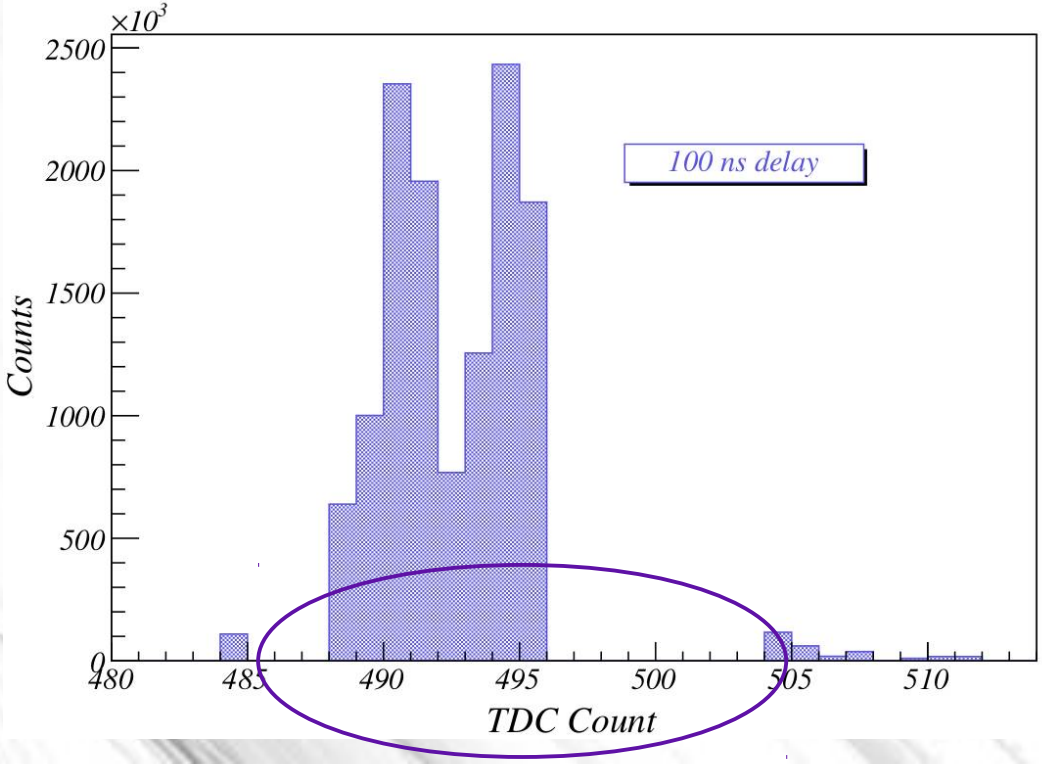
2 peaks with distance,

corresponding to the 2 different slopes in TDC ramp


×10^6
1 ns delay
Counts
TDC Count


×10^3
20 ns delay
Counts
TDC Count


×10^3
40 ns delay
Counts
TDC Count


×10^3
100 ns delay
Counts
TDC Count

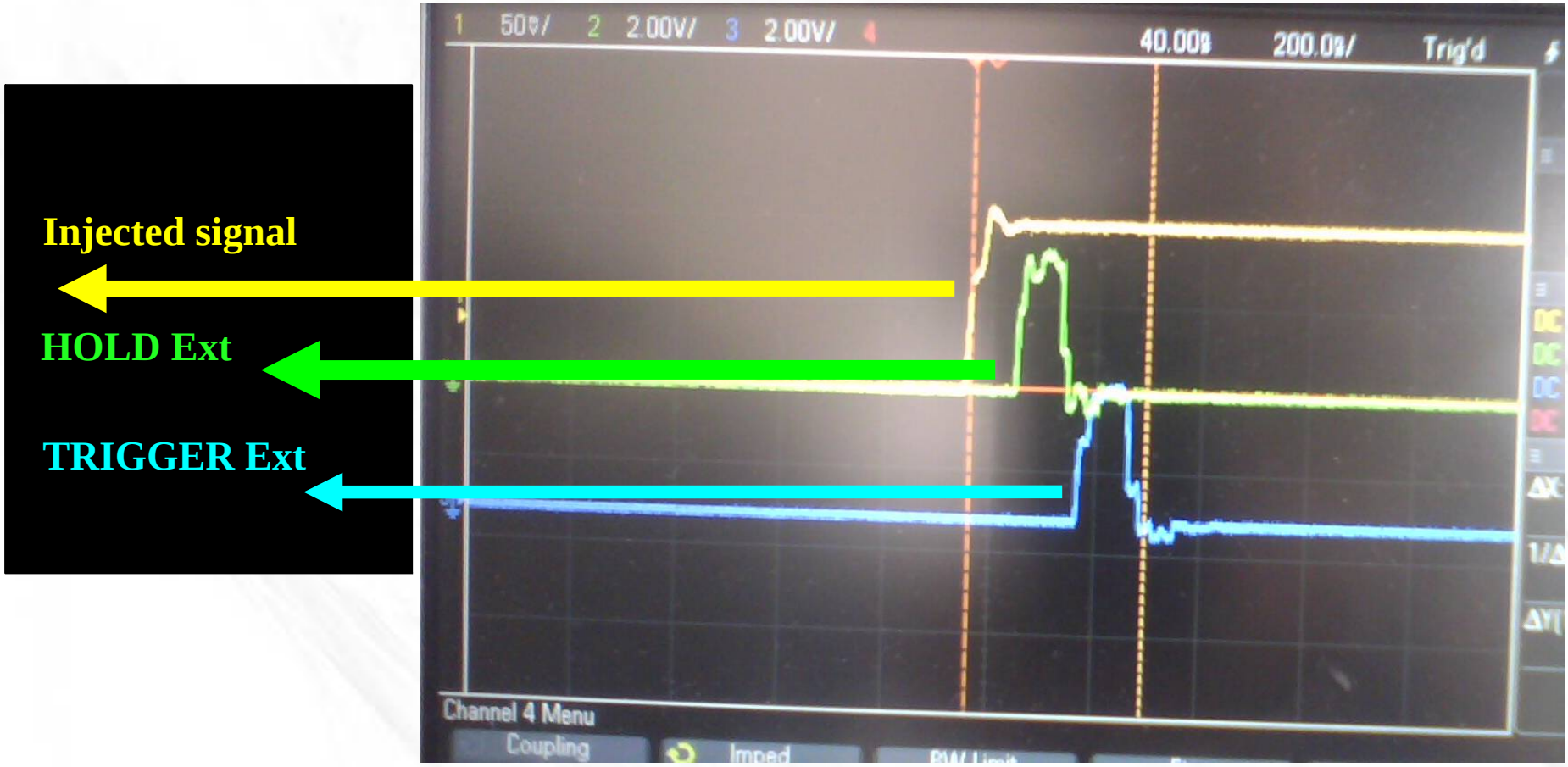
Conclusion

1. The 4 /1 SPIROC ASIC chip are tested with injection of charge.
2. The pedestal value smaller than expected value.
3. The TDC signal position observed differ than pedestal position.
4. For various delayed signal the shift observed in TDC count.

Next step

1. SPIROC 2 – see physical signal with different injected signal within few week!

backUP Slide



backUP slide

FEV 7 board with glued Si wafer