CMOS Pixel Sensors adapted to the ILD VTX

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- Sensor design : coll. with IRFU-Saclay -
- Ladder design : coll. with Bristol - DESY - Oxford -

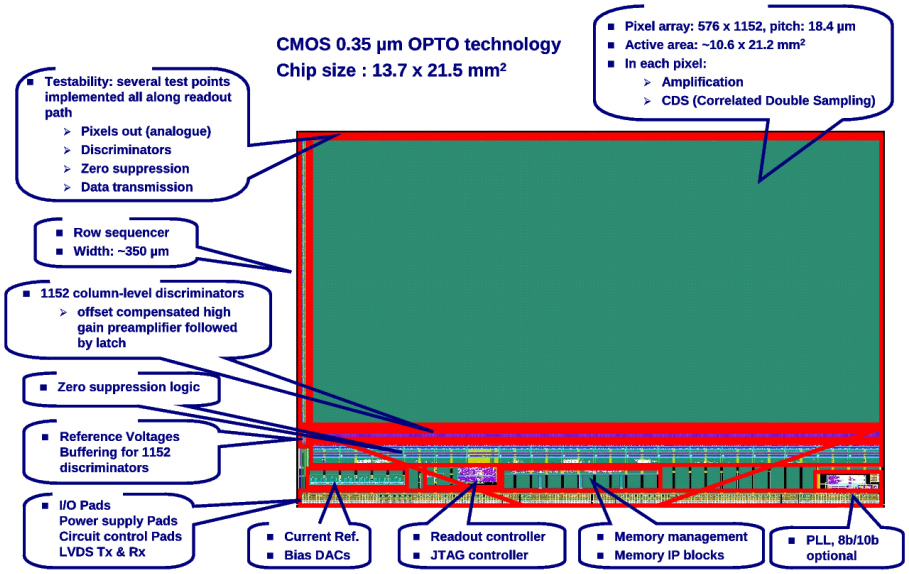
Tokushin Kick-off Meeting – 13 Septembre 2011

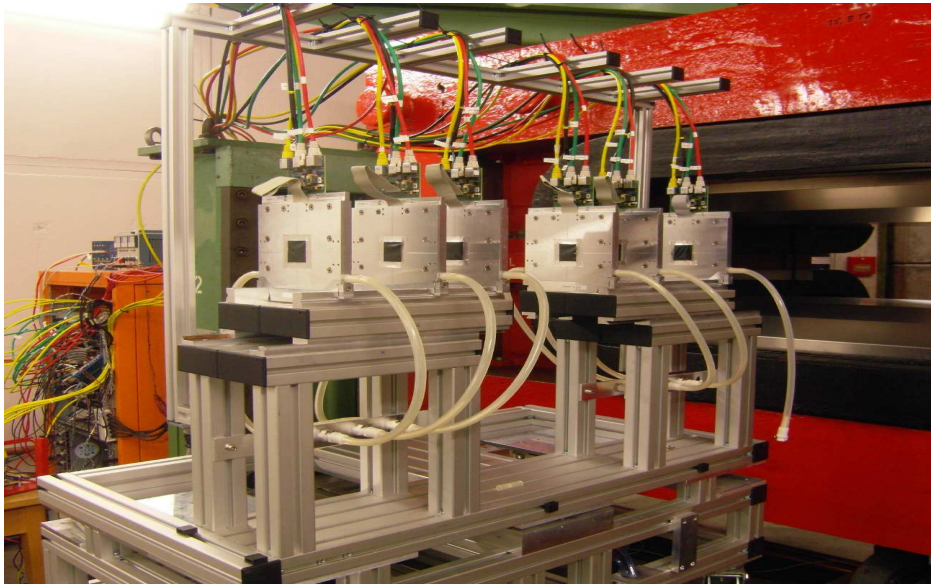
Contents

CMOS Pixel Sensors: Established Architecture

- **Main characteristics of MIMOSA sensor equipping EUDET BT:**

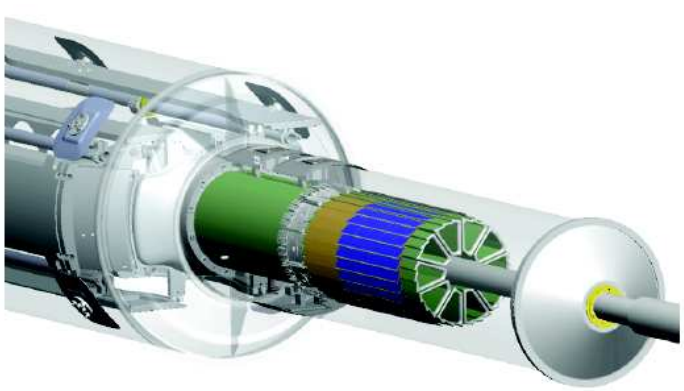
  - ⁕ 0.35 μm process with high-resistivity epitaxial layer
    (coll. with IRFU/Saclay)
  - ⁕ column // architecture with in-pixel amplification (cDS)
    and end-of-column discrimination, followed by $\emptyset$
  - ⁕ active area: 1152 columns of 576 pixels (21.2×10.6 mm^2)
  - ⁕ pitch: 18.4 $\mu m \rightarrowtail$ $\sim$ 0.7 million pixels
    - ▷ charge sharing $\Rrightarrow$ $\sigma_{sp} \lesssim$ 3.5 μm
  - ⁕ $t_{r.o.} \lesssim$ 100 μs ($\sim 10^4$ frames/s)
    suited to $> 10^6$ part./cm^2/s
  - ⁕ JTAG programmable
  - ⁕ rolling shutter architecture
    - $\Rrightarrow$ full sensitive area dissipation $\equiv$ 1 row
      - ▷ $\sim$ 250 mW/cm^2 power consumption (fct of N_{col})
  - ⁕ thinned to 50 μm

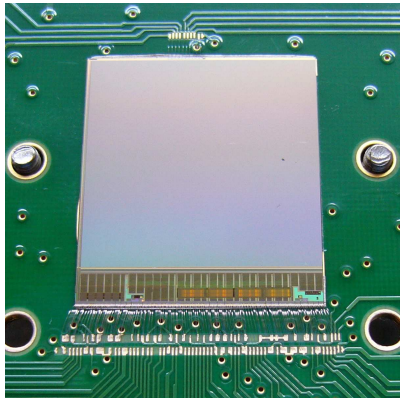


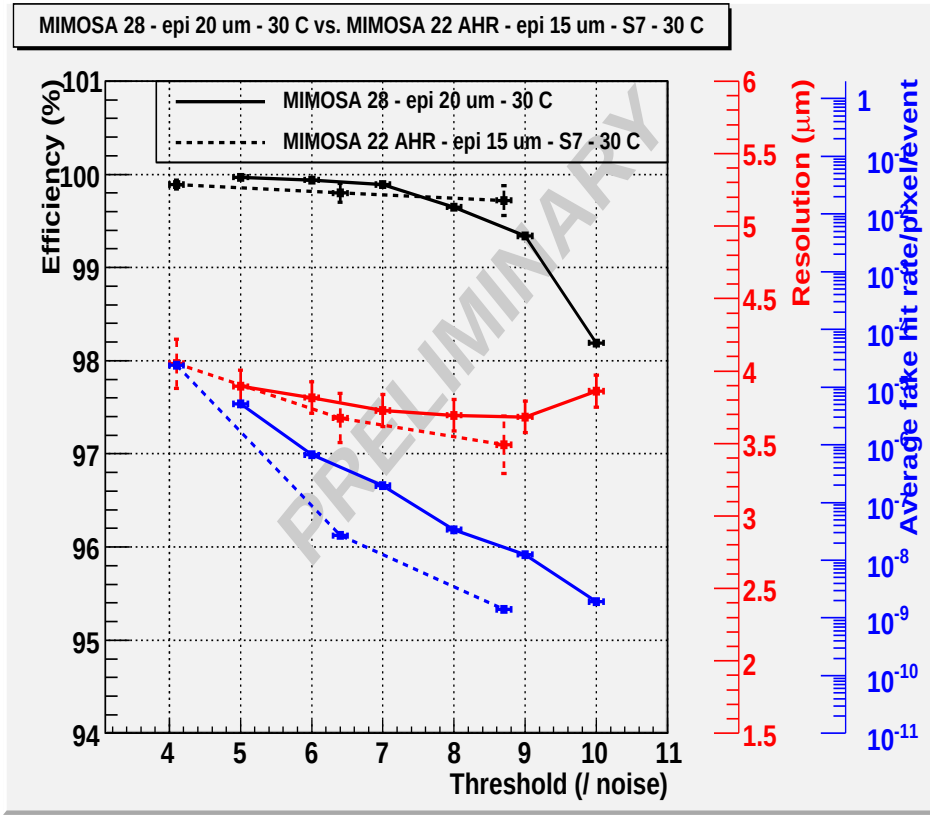


State-of-the-Art: MIMOSA-28 for the STAR-PXL

- **Main characteristics of ULTIMATE ($\equiv$ MIMOSA-28):**
  - ⁕ 0.35 μm process with high-resistivity epitaxial layer
  - ⁕ column // architecture with in-pixel cDS & amplification
  - ⁕ end-of-column discrimination & binary charge encoding
  - ⁕ on-chip zero-suppression
  - ⁕ **active area: 960 colums of 928 pixels (19.9$\times$19.2 mm^2)**
  - ⁕ **pitch: 20.7 μm $\rightarrowtail$ $\sim$ 0.9 million pixels**
    - ↪ **charge sharing $\Rrightarrow$ $\sigma_{sp} \gtrsim$ 3.5 μm** ▷▷▷
  - ⁕ JTAG programmable
  - ⁕ **t$_{r.o.}$ $\lesssim$ 200 μs ($\sim$ 5$\times$10^3 frames/s) $\Rrightarrow$ suited to $>$10^6 part./cm^2/s**
  - ⁕ 2 outputs at 160 MHz
  - ⁕ $\lesssim$ 150 mW/cm^2 power consumption







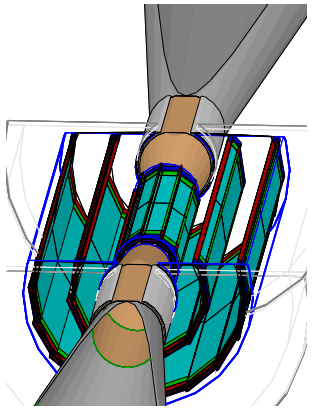
▷▷▷ **Tests under way since early April :** (50 μm thin)

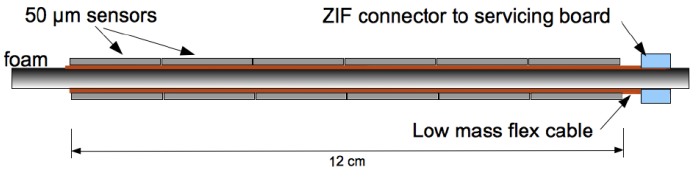
- ⁕ N $\lesssim$ 15 e$^-$ ENC at 30-35°C (as MIMOSA-22AHR)
- ⁕ CCE (^{55}Fe) similar to MIMOSA-22AHR
- —○ Ionising rad. tolerance validated (150 kRad at 30°C)
- —○ NI rad. tolerance validation (3·10^{12} n$_{eq}$/cm^2 at 30°C) in Oct. 2011

▷▷▷ **Start of data taking in FY-2012**

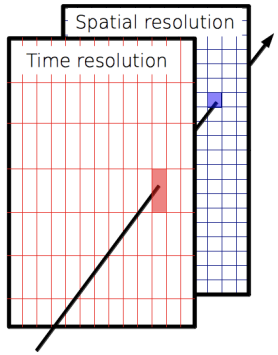
CMOS sensors for the ILD-VTX

- **Two types of sensors :**
  - ⁕ Inner layers ($\lesssim$ 300 cm^2) : priority to read-out speed & spatial resolution
    - ↪ small pixels (16×16 / 80 μm^2) with binary charge encoding
      - ↪ $t_{r.o.} \sim$ 50 / 10 μs; $\sigma_{sp} \lesssim$ 3 / 5 μm
  - ⁕ Outer layers ($\sim$ 3000 cm^2) : priority to power consumption and good resolution
    - ↪ large pixels (35×35 μm^2) with 3-4 bits charge encoding
      - ↪ $t_{r.o.} \sim$ 100 μs; $\sigma_{sp} \lesssim$ 4 μm
  - ⁕ Total VTX instantaneous (average) power $<$ 700 W (20 W)

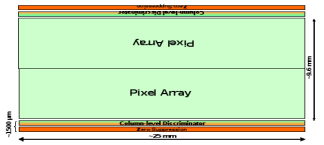


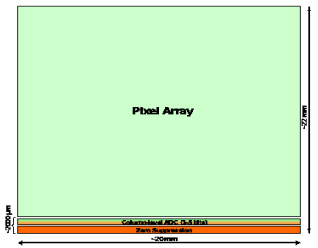


- **2-sided ladder concept for inner layer :**
  - ⁕ Square pixels (16×16 μm^2) on internal ladder face ($\sigma_{sp} < 3\ \mu m$)
    & Elongated pixels (16×80 μm^2) on external ladder face ($t_{r.o.} \sim 10\ \mu s$)



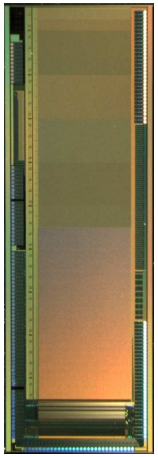
- **Sensor final prototypes :** submitted for fab. Sept. 4th, 2011
  - ⁕ MIMOSA-30: inner layer prototype with 2-sided read-out
    - ↪ one side : 256 pixels (16×16 μm^2)
      other side : 64 pixels (16×64 μm^2)
  - ⁕ MIMOSA-31: outer layer prototype
    - ↪ 48 col. of 64 pixels (35×35 μm^2) ended with 4-bit ADC

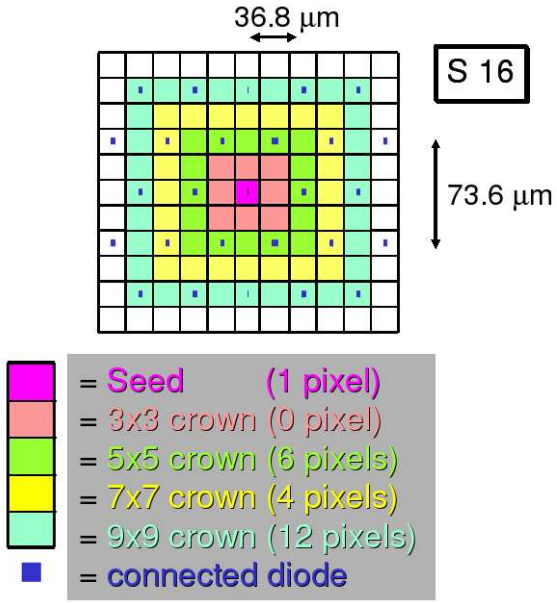




Towards a Large Pitch

- **Large pitch : Motivations**
  - ⁂ elongated pixels allow faster read-out
  - ⁂ trackers (e.g. ILD-SIT) require $\sigma_{sp} \gtrsim 10\ \mu m$
  - ⇛ minimise number of pixels for the sake of power dissipation, integration time and data flow
- **Large pitch : Limitations (besides spatial resolution)**
  - ⁂ DANGER: increasing distance inbetween neighbouring diodes
    - ⇛ particles traversing sensor ”far” from sensing diodes may not be detected because of e^- recombination
  - ⁂ ”fragile” detection efficiency, exposed to losses due to irradiation, high temperature operation & ”slow” read-out
- **Elongated pixels : Test results**
  - ⁂ elongated pixels allow minimising the drawbacks of large pitch
  - ⁂ concept evaluated with MIMOSA-22AHR prototype, composed of a sub-array with 18.4×73.6 μm^2 pixels ▷▷▷
  - ⁂ m.i.p. detection performances assessed at CERN-SPS (T ∼ 15°C)
    - —○ ϵ_{det} ∼ 99.8 %
    - —○ σ_{sp} ∼ 5-6 μm (binary charge encoding)
- **Square pixels : prototype back from foundry**
  - ⁂ MIMOSA-29 being fabricated on high-res epitaxy
  - ⁂ pixels of ≤ 80×80 μm^2

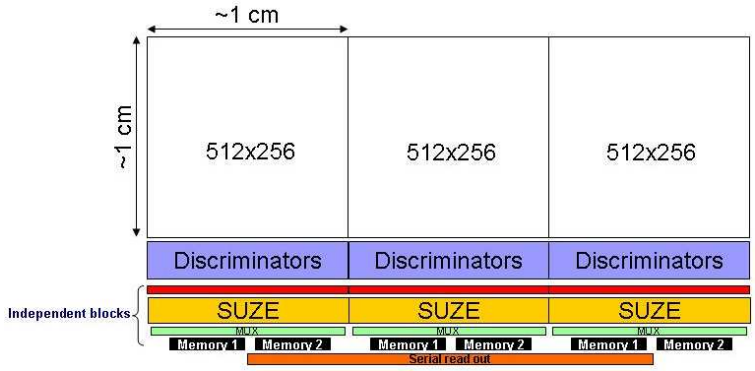




Moving to 0.18 μm CMOS Technology

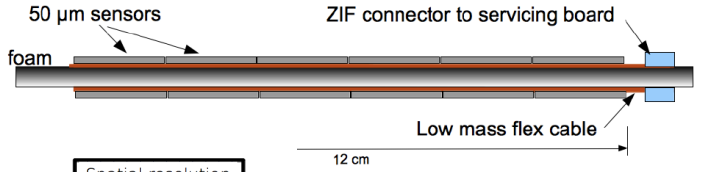
- **Evolve towards feature size $<<$ 0.35 μm :**
  - ⁂ **μcircuits :** smaller transistors, more Metal Layers, ...
  - ⁂ **sensing :** quadruple well, depleted sensitive volume, ...
- **Benefits :**
  - ⁂ higher μcircuit density ⇛ higher data reduction capability
  - ⁂ thinner gates, depletion ⇛ improved radiation tolerance (in particular ionising radiation)
  - ⁂ faster read-out ⇛ improved time resolution
  - ⁂ possibility of stitching ⇛ multireticule sensors
- **Development plans :**
  - ⁂ also motivated by ALICE-ITS/MFT, CMB-MVD, AIDA-SALAT, eRHIC-VD, ...
  - ⁂ step 1 : MIMOSA-32 ▷ submission on 24.10.11
    - —○ exploratory sensor (various sensing systems, amplifiers, discri., ...)
  - ⁂ step 2 : MIMOSA-22THR & SUZE-02 ▷ submission in Spring '12
    - —○ M22-THR : 128 col. of 512 pixels, ended with discri.
    - —○ SUZE-02: zero-suppression μcircuit
  - ⁂ step 3 : Full Scale Basic Block (FSBB) ▷ submission in Spring '13
    - —○ 1x1 cm^2 sensitive area ($\sim$ 20 μm pitch)
    - —○ combination of M22-THR & SUZE-02
    - —○ scalable to various applications ($\geq$ 2014) ▷ ▷ ▷

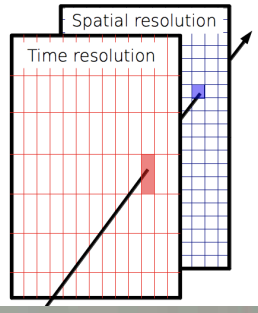
FSBB

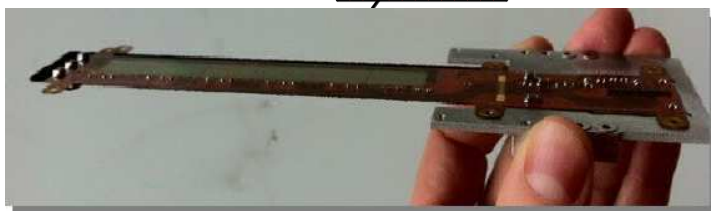


Sensor Integration in Ultra Light Devices

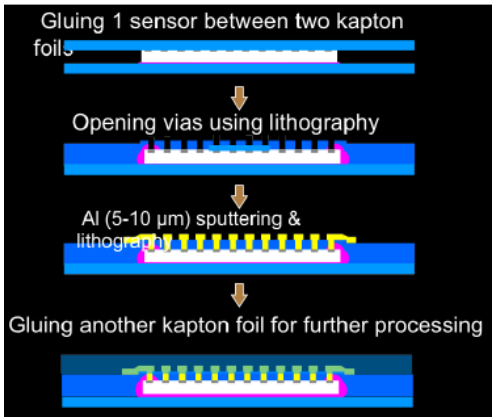
- **Double-sided ladders with time stamping :**
  - ⁂ manyfold bonus expected from 2-sided ladders:
    compactness, alignment, pointing accuracy (shallow angle), redundancy, etc.
  - ⁂ studied by PLUME coll. (Oxford, Bristol, DESY, IPHC) & AIDA (EU)
    ↪ **P**ixelated **L**adder using **U**ltra-light **M**aterial **E**mbedding
  - ⁂ square pixels for single point resolution on beam side
  - ⁂ elongated pixels for 4-5 times shorter r.o. time on other side
  - ⁂ correlate hits generated by traversing particles
  - ⁂ expected total material budget $\sim$ 0.3 % X_0
    ↪ 1st proto. (0.6 % X_0) fabricated & operationnal
    ▷ beam tests at CERN-SPS (traversing m.i.p.) in Nov. '11

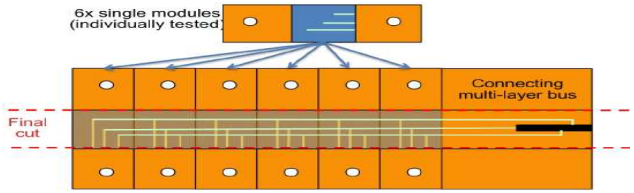






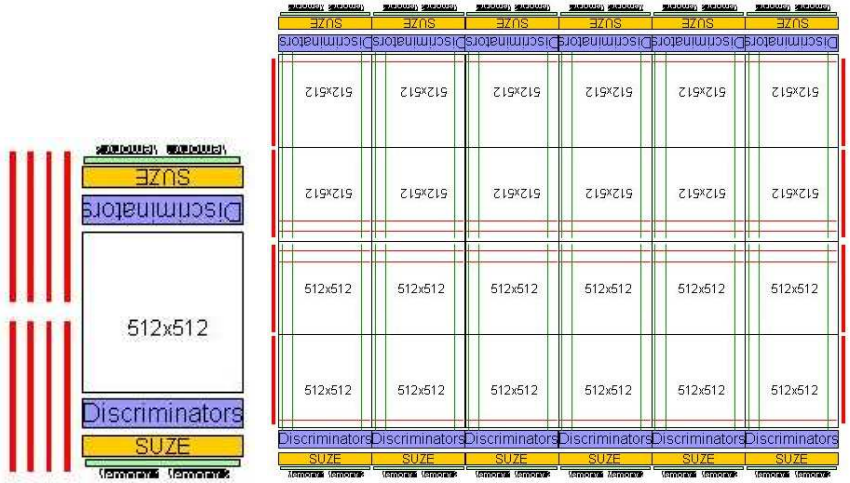
- **Unsupported ladders (Hadron Physics 2 / FP-7)**
  - ⁂ 50 μm thin CMOS sensors embedded in thin kapton and cabled with redistributed connections $\rightarrowtail$ suited to curved surfaces ?
  - ⁂ expected total material budget $\lesssim$ 0.15 % X_0
  - ⁂ 1st single sensor mechanical prototype fabricated
  - ⁂ 1st 2-sensor electrical proto. expected before end of 2011



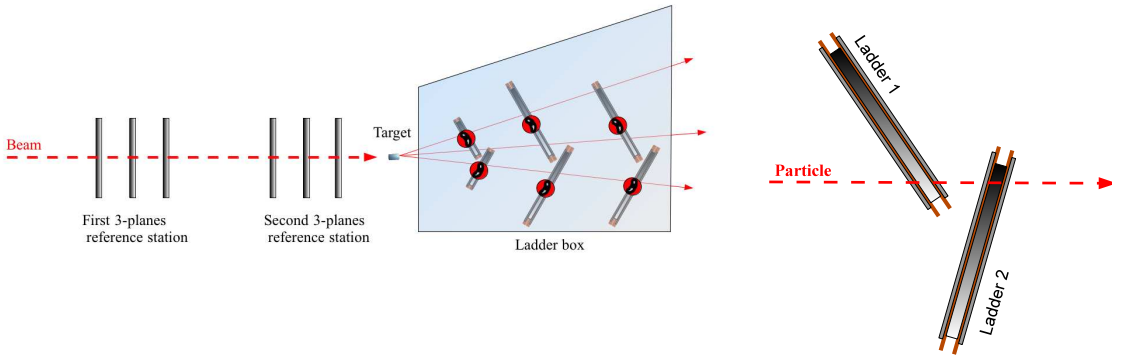


AIDA Project : Assessment of Stitching & 2-Sided Ladder

- **Single Arm Large Area Telescope (SALAT):**
  - ⁂ *2048×3072 pixels (∼ 20 μm pitch)*
    - ⇛ *4×6 cm^2 sensitive area, ∼ 3.5 μm spatial resolution*
  - ⁂ *requires combining several reticules (based on FSBB)*
    - ⇛ *stitching process* ⇛ *establish proof of principle*
  - ⁂ *2-sided read-out of 1024 rows in ∼ 200 μs*
    - ⇛ *3 planes of Large Area Telescope for AIDA project (EU-FP7)*
  - ⁂ *windowing of $\lesssim$ 1×6 cm^2 (collimated beam)*
    - ⇛ *∼ 50 μs r.o. time*
  - ⁂ *50-100 μm pitch variants under consideration (trackers)*



- **Alignment Investigation Device (AID) :**
  - ⁂ *box allowing to mount 3 pairs of ladders*
    arranged in 3 consecutive layers ≡ VTX sector
  - ⁂ *can be equipped with PLUME (2-sided) ladders*
  - ⁂ *ladders are mounted on movable micrometric support*
    - ⇛ *investigate alignment with particles traversing*
      overlapping regions of neighbouring ladders
  - ⁂ *allows developing clustering, tracking & vertexing algo. with particle beams*



SUMMARY

- **Sensor architecture developed in 0.35 μm technology validated :**
  - ▷ complies with specs of σ_{sp}, thickness, rad. tol. (T_{room}), r.o. speed & P_{diss} of VTX
  - ▷ sensors getting implemented in various devices: STAR-PXL, NA-63, CMB-MVD, ALICE-ITS & MFT, ...
- **Translation 0.35 $\mu m \rightarrowtail$ 0.18 μm CMOS under way :**
  - ▷ exploratory chip (MIMOSA-32) to be submitted for fabrication on 24.10.2011
  - ▷ mid-scale prototypes validating architecture in Summer 2012 ▷ DBD
  - ▷ Full Scale Basic Block (FSBB) expected to be validated in 2013
  - ▷ design flexible enough to be adaptable to various designs
- **Long range R&D : 3D sensors for SiD, ILC-1000, CLIC**
- **Ladders development makes progress :**
  - ⁂ 2-sided ladder 1st proto. (0.6 % X_0) fabricated & operationnal ▷ beam tests (SPS) in Nov. 2011
  - ⁂ next 2-sided ladder (2012) expected to feature $<$ 0.4 % X_0
  - ⁂ 2-sided ladder added value will be assessed within AIDA-EU project
  - ⁂ unsupported ladder (0.1 - 0.15 % X_0) concept progressing (1 mechanical proto. successful) ▷ adapted to curved surfaces ?
- **Numerous spin-offs foreseen $\Rrightarrow$ opportunities of combined efforts**