SiW ECAL planning

In ANR project (Rémi), we have several deadlines to meet shapes our project as a whole

STATUS (electronics, system integration)

- have a few partially instrumented FEV7 ASU with packaged SPIROC2(a) ASICs Now being tested with CALICE DAQ2, adapter card, soon with cosmics
- SKIROC2 ASIC is being tested, no major problems identified
- work on design of ChipOnBoard PCB (FEV8) continuing

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PLAN

- first priority, conservative option: a few (~10) layer prototype by next summer with **packaged** SKIROC2 ASICs
 - → implies "U" structure

Test beams:

1 or 2 layer test ~March 2012 (SPIROC2 and/or SKIROC2)

10 layer test June/July 2012

- second stage will be to develop SKIROC2 ChipOnBoard version Work on PCB design continues in parallel with above

FEV8 ASU integration (bonding, gluing) ~ from september 2012

Multi-layer prototype tests mid-2013



