



JOHANNES GUTENBERG  
UNIVERSITÄT MAINZ



# Mainz Electronics Group in CALICE

**Uli Schäfer, Rainer Wanke, André Welker  
(for the Mainz CALICE group)**

**CALICE DAQ Workshop**

**École Polytechnique, Nov 9, 2011**



# The Mainz Electronics Group

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## Who we are:

- **Staff**, working in area of electronics design and programmable logic devices:  
Bruno Bauß, Reinhold Degele, Uli Schäfer
- **Students**, mainly working for programmable logic and system tests:  
Patric Kiese, André Welker, ...
- **Supervisors**, not much working:  
Volker Büscher, Rainer Wanke, ...

## Recent projects:

- **JEM (Jet/Energy module)**

for ATLAS L1 calorimeter trigger:

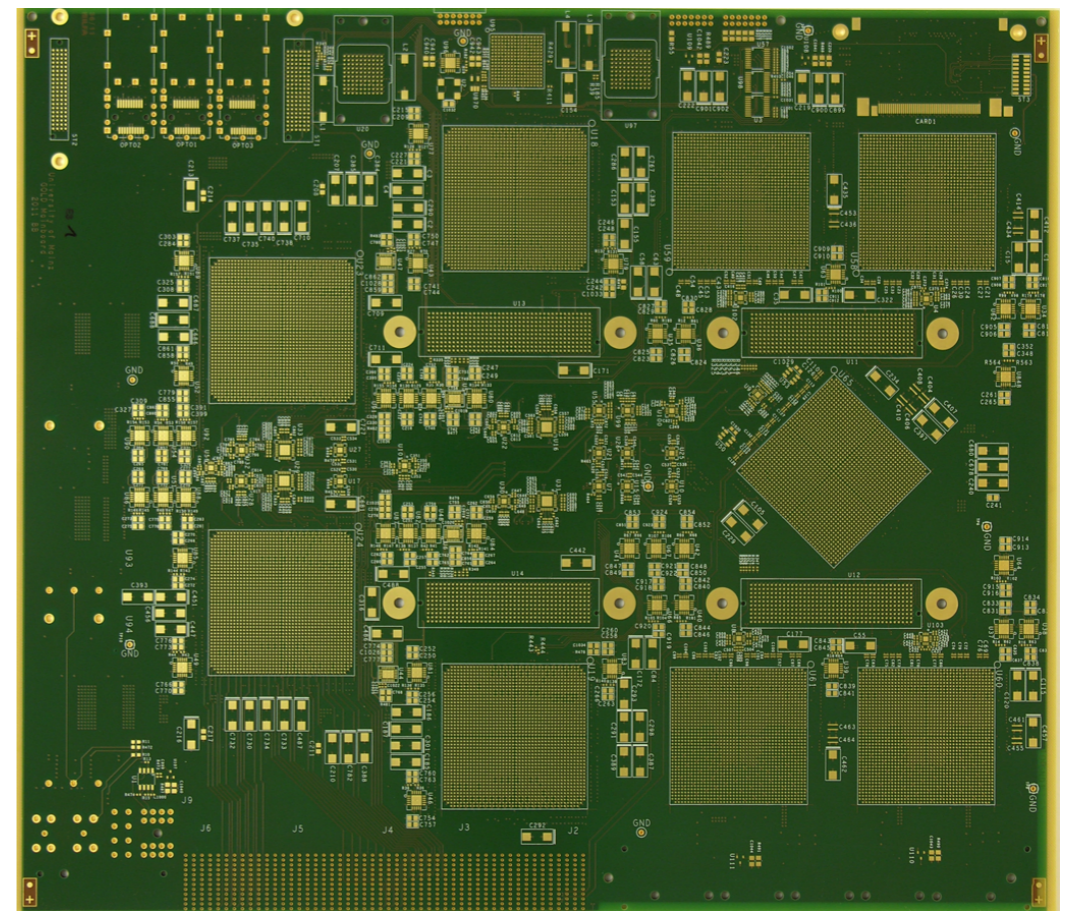
- 9U, 14 layer PCB with VME/Custom backplane.
- 88 x 480 Mb/s energy sum input data.
- Jet finder and energy sum logic in a total of 6 FPGAs (Virtex-2).
- 32 JEM modules running in ATLAS

## ■ ATLAS upgrade:

Various smaller PCB designs, jitter cleaner, Virtex-5 based processor, 6.4 Gb/s optical links.

Currently: **"GOLD" demonstrator** for L1 topology trigger:

- Advanced TCA Module
- 22 layer PCB
- 9 FPGAs (Virtex-6 LXT/HXT)
- through-backplane optical links at 6.4/10 Gb/s (up to 5 MTP connectors, up to 72 fibres each)

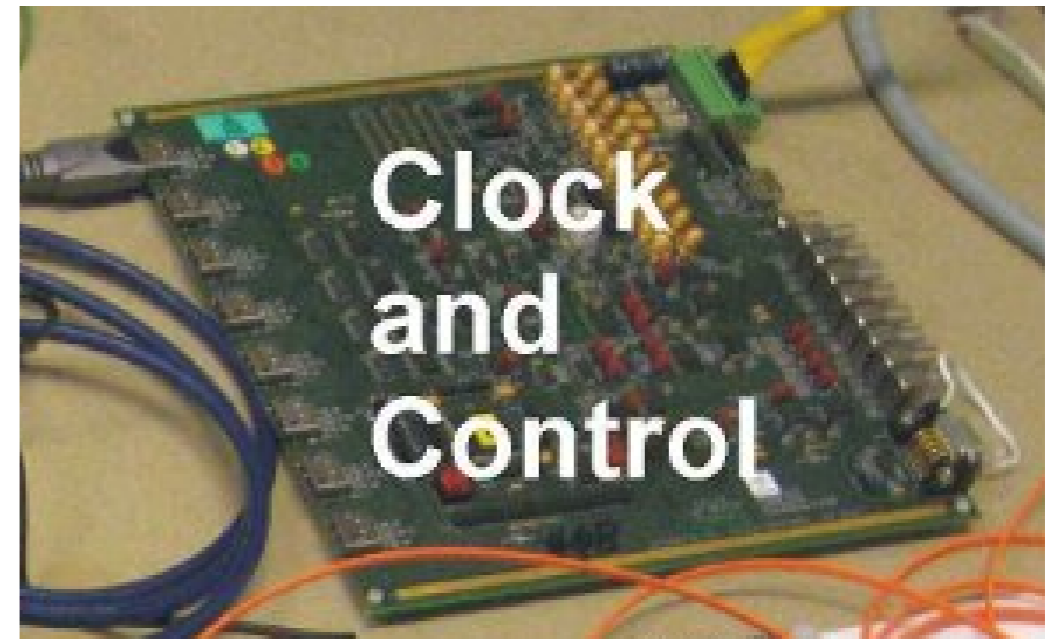


**GOLD PCB**

# Interests in CALICE

Interested in working on improvement of the **Calice CCC**.

- **Assumption so far:**  
improvement needed on
  - Jitter
  - Logic capacity on on-board programmable devices



- **Suggestion:**
  - Add optical fibre links to break ground loop on a multi-subdetector setup

# Interests in CALICE

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- **But still some lack of understanding:**

- How does a setup with a CCC and a TLU look like?
- What is required to make them compatible or to have them talk to one another?

- **Apart from above mentioned issues:**

Is a new CCC meant to be built along the design of the current one?

# Interests in CALICE



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***Hope for many instructive discussions at the meeting and to make a significant contribution to a CALICE success!***