Vertex-Detector R&D for CLIC

KILC12
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for the CLIC Physics and Detector study

Outline

- Requirements
- Machine environment and backgrounds
- Simulation layouts
- Sensor- and readout-technology R&D
- Power delivery / power pulsing and cooling

Requirements

- Integral part of tracking systems (in particular for low p_T)
- Efficient tagging of heavy quarks + tau leptons through precise determination of displaced vertices:

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}$$

$$a \approx 5\mu m \quad b \approx 15\mu m$$

→ Good single point resolution: σ_{SP}~3 μm

→ Low material budget: X ≲ 0.2% X_0 / layer (incl. cooling)

- Full coverage down to low polar angles θ_{min}~7°
- Few % occupancy despite large background rates
- Time stamping with ~10 ns accuracy, to reject background

- To date: no technology option available fulfilling all requirements

→ Simulation studies: impact of layout on performance

→ Integration/Assembly + power-pulsing + cooling studies

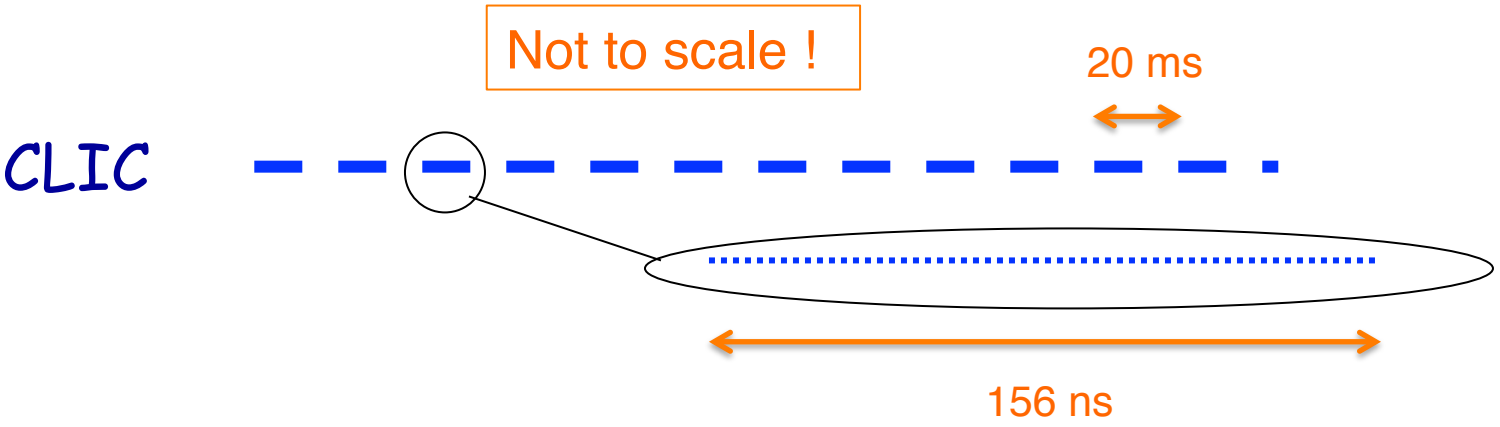
→ R&D on sensors & readout

CLIC machine environment

	CLIC at 3 TeV
L ($cm^{-2}s^{-1}$)	5.9×10^{34}
BX separation	0.5 ns
#BX / train	312
Train duration (ns)	156
Rep. rate	50 Hz
σ_x / σ_y (nm)	≈ 45 / 1
σ_z (μm)	44

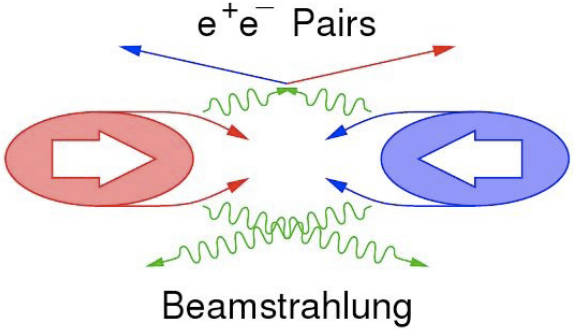
Drives timing requirements for CLIC detector

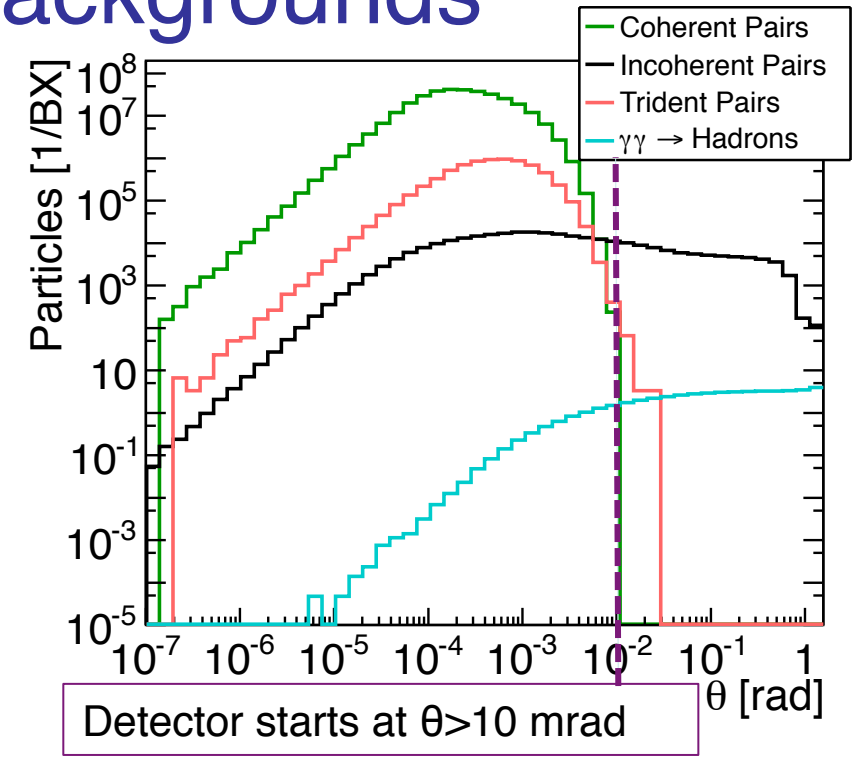
very small beam size

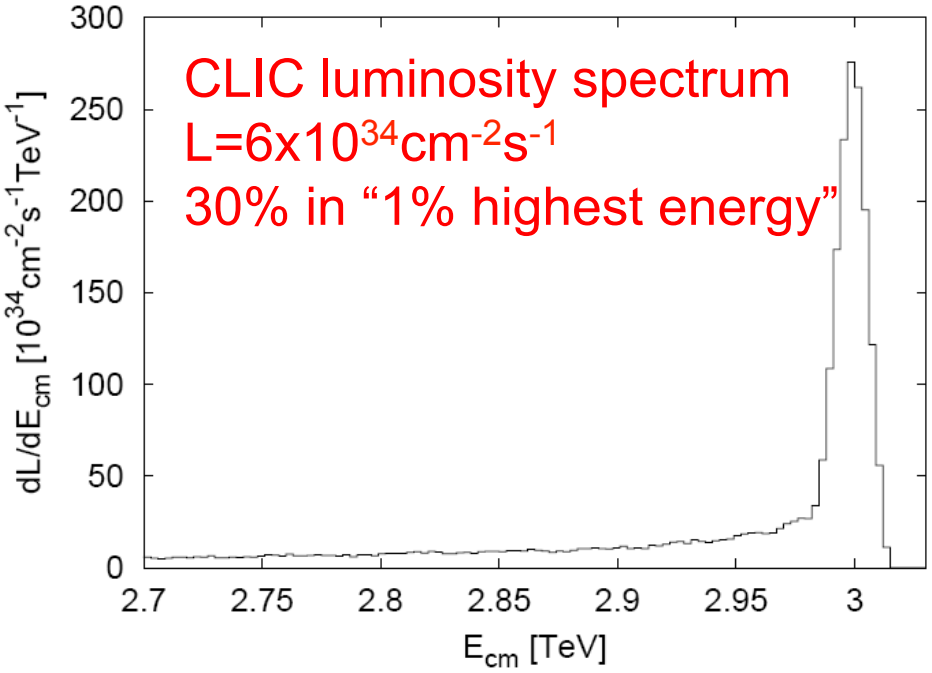


Beam-induced backgrounds

e^+e^- pairs and $\gamma\gamma \rightarrow$ hadrons at $\sqrt{s}$=3 TeV







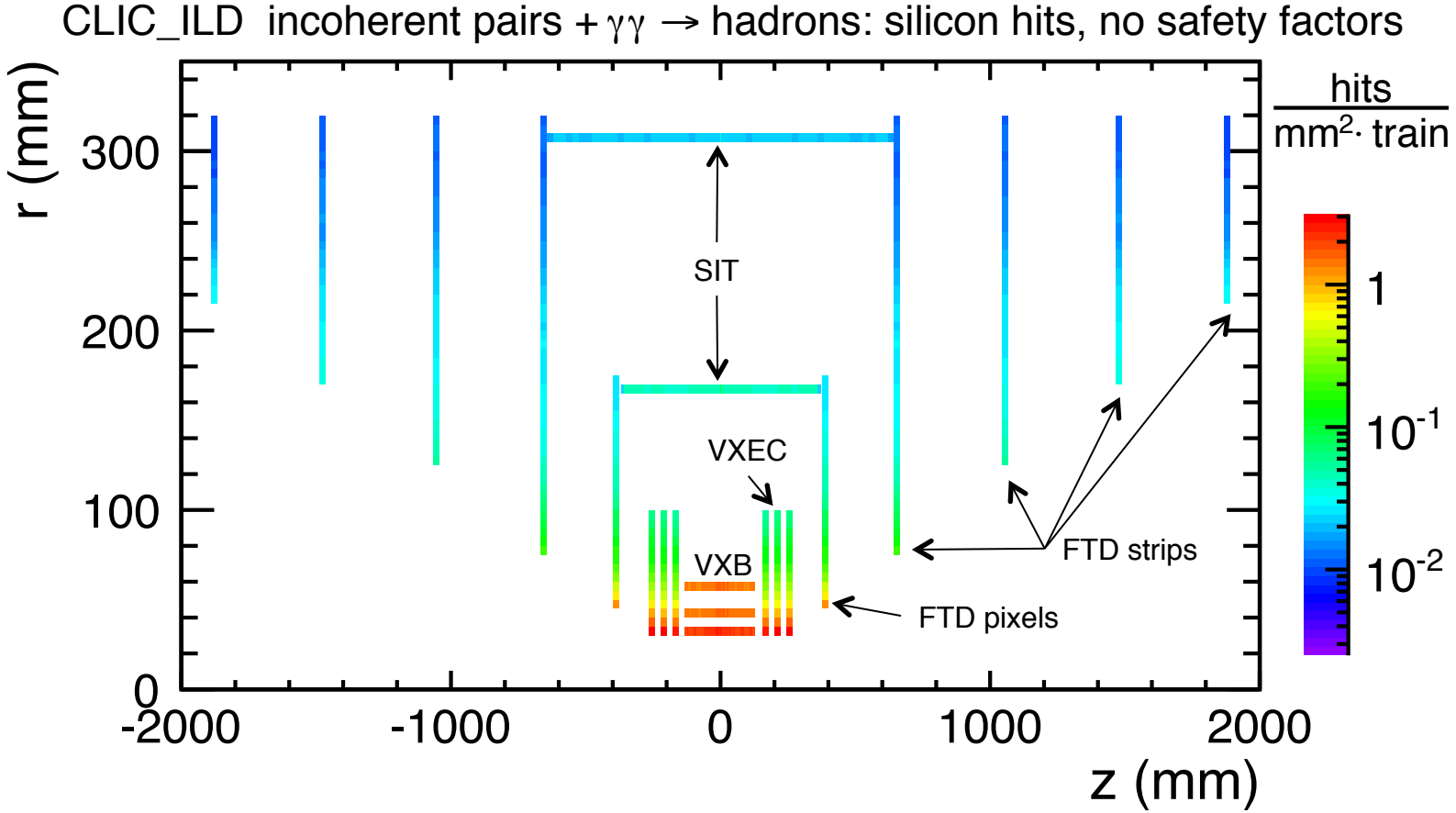
Main backgrounds in detector:

- **Incoherent e^+e^- pairs**: 60 particles / BX
- **$\gamma\gamma \rightarrow$ hadrons**: 54 particles / BX

→ Need **pile-up rejection**

→ Need to include background in **simulation**

Backgrounds in inner tracking region



Occupancies per r/o cell and bunch train and radiation exposure, including clustering and safety factors:

Region	Readout granularity	Max. occup.	NIEL [$n_{eq}/cm^2/y$]	TID [Gy/y]
VXB	20 µm x 20 µm	1.9 %	$4x10^{10}$	200
VXEC	20 µm x 20 µm	2.8 %	$5x10^{10}$	180
FTD pixels	20 µm x 20 µm	0.6%	$2.5x10^{10}$	50
FTD strips	10 cm x 50 µm	290 %	$1x10^{10}$	7
SIT	9 cm x 50 µm	170 %	$2x10^{9}$	2

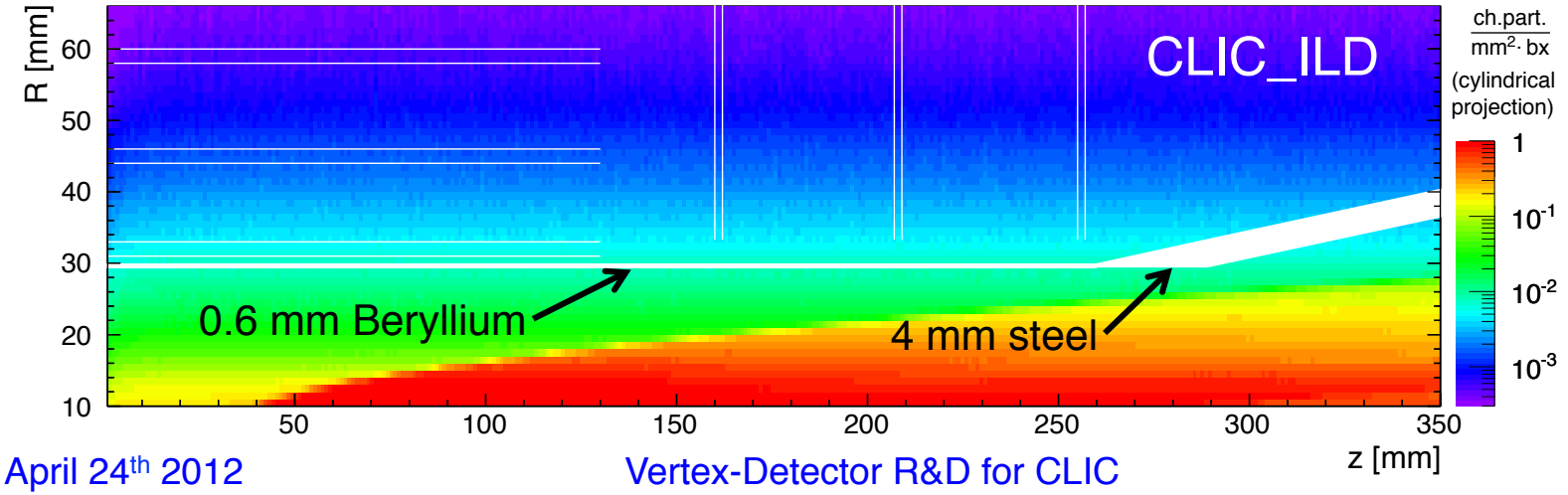
Beam pipe

Requirements for beam pipe:

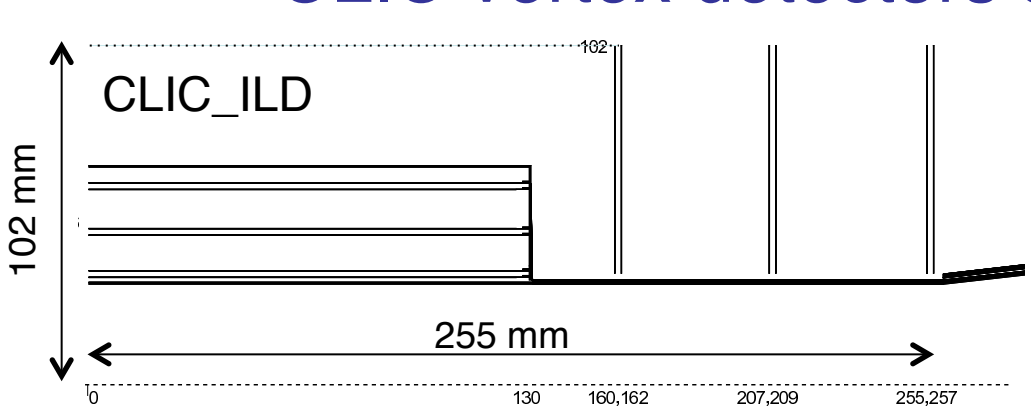
- Provide good vacuum → leak tightness
- Minimise multiple scattering → small amount of material in central part
- Allow for placement of Si layers close to IP → small radius
- Stay outside region of high background occupancy → lower limit on radius
- Shield against back scatters from forward region → thick conical part outside VTX acceptance

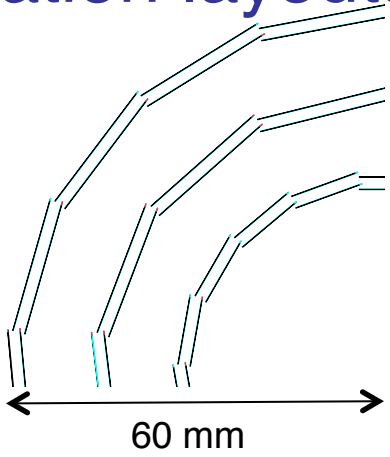
Implementation in simulations:

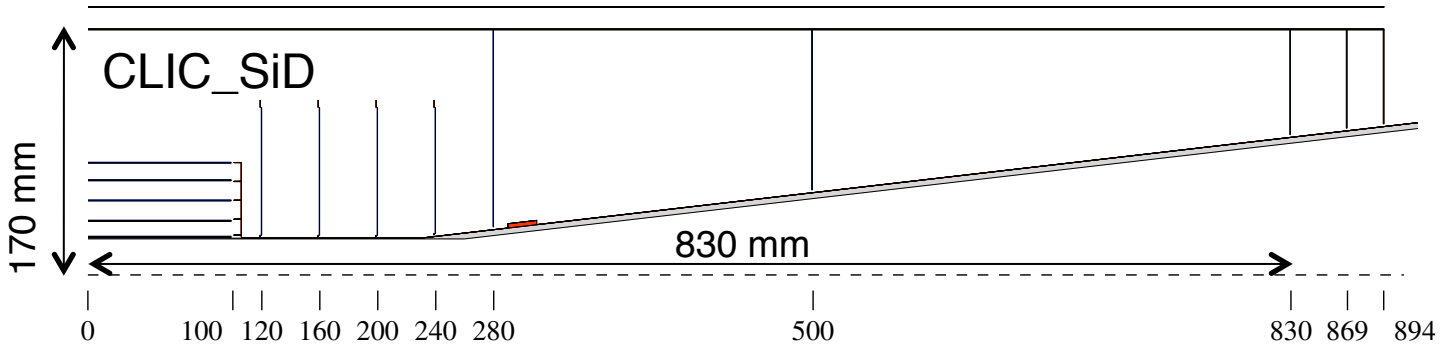
- Central Beryllium part:
  - CLIC_ILD: d=0.6 mm, R=29.4 mm (B=4 T)
  - CLIC_SiD: d=0.5 mm, R=24.5 mm (B=5 T)
  - Safe w.r.t. backgrounds, vacuum collapse, leak tightness (D0, CDF experience in run II)
  - Unlike ILC: no extra shielding, due to low expected levels of incoh. synchrotron radiation (t.b.c.)
- Forward conical part:
  - 4 mm iron, to shield against back scatters from forward region
  - Pointing to interaction point → no extra material inside tracking acceptance

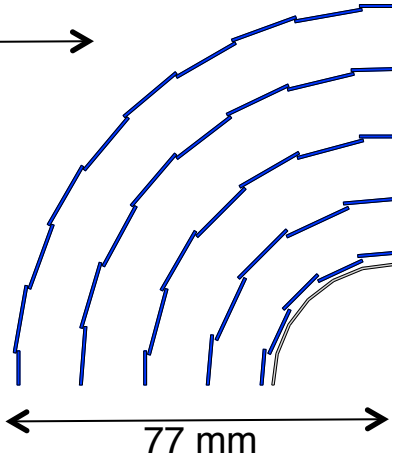


CLIC vertex detectors simulation layouts





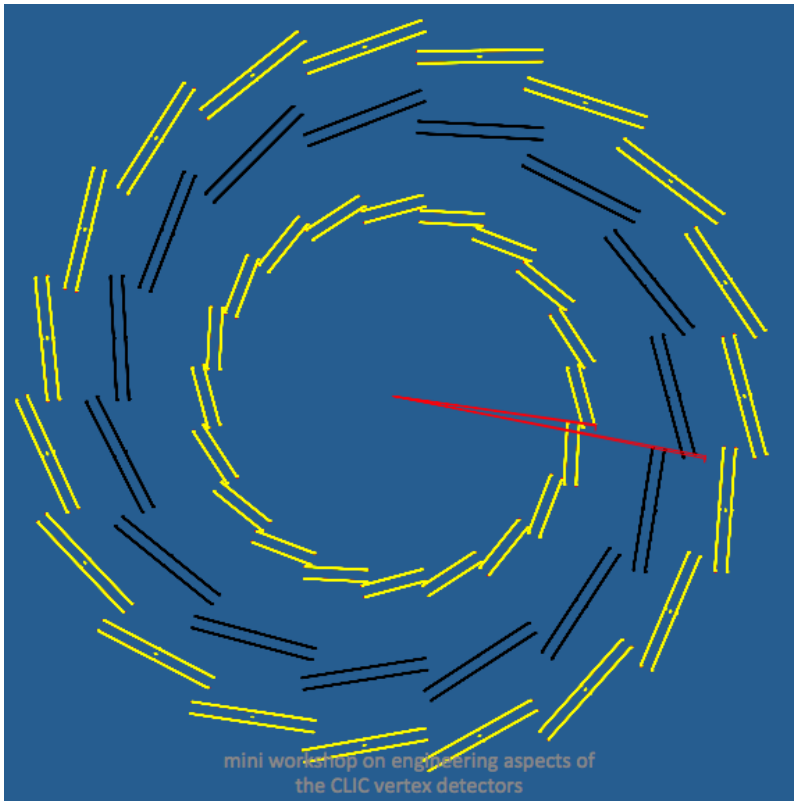


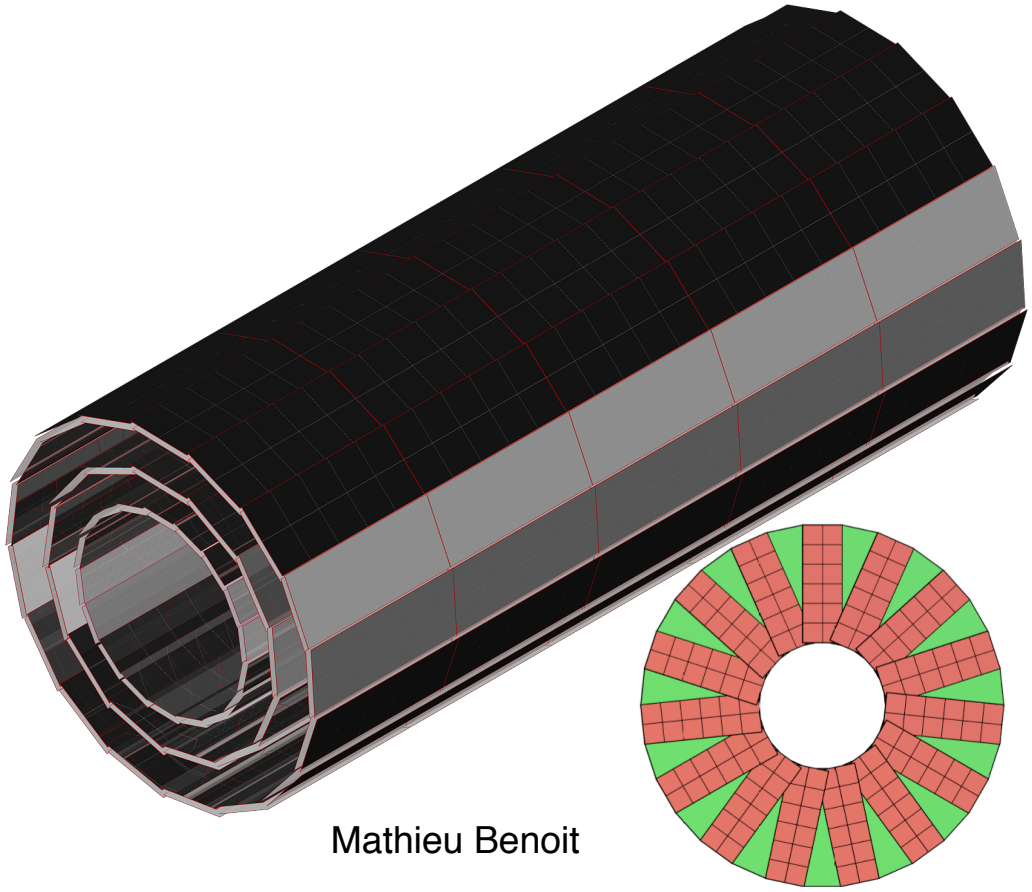


	CLIC_ILD	CLIC_SiD	CMS
Material X/X0 (90°)	~0.9% (3x2 layer)	~1.1% (5 layer)	~10% (3 layer)
Pixel size	20 x 20 μm^2	20 x 20 μm^2	100 x 150 μm^2
# pixels	1.84 G	2.76 G	66 M
Time resolution	~10 ns	~10 ns	<~25 ns
Avg. power/pixel	<~0.2 μW	<~0.2 μW	28 μW

Modules and stave layout (post-CDR)

- First ideas for post-CDR CLIC_ILD module + stave layouts (various options)
- Based on CLIC_ILD_CDR simulation design, taking into account constraints from hybrid sensor + readout concept
- Minimize cabling + active components through vertical integration (TSV) and stitching between neighboring chips
- Design has to take into account inactive regions and Lorentz-angle effect





Mathieu Benoit

Pixel-detector technology options

- <~ 25x25 μm^2 pixel sizes → need small feature sizes
- Time-stamping ~10 ns → need high-resistivity sensor
- ~0.2% material/layer → corresponds to ~200 μm silicon (incl. support + cables)
- 156 ns bunch train every 20 ms → trigger-less readout, power pulsing
- Radiation exposure <10^{11} n_{eq}/cm^2/yr → radiation hardness not a major concern

Possible technology development paths:

1) **Hybrid or multi-tier technologies**

- Thinned high-resistivity fully depleted sensors, ~50 μm thick
- Fast, low-power highly integrated readout chip, ~50 μm thick
- Low mass interconnects
- Pros: factorization of sensor + readout R&D;
  r/o chips profit fully from advancing industry standards
- Cons: interconnect difficult/expensive; harder to reduce material

2) **Integrated technologies**

- Sensor and readout combined in one chip or 3D integration of multiple tiers
- Charge collection in epitaxial layer (typically < 1 μm)
- Pros: allows for very low material solutions; synergy with R&D for ILC detectors
- Cons: harder to achieve good time resolution and sufficient S/N

Hybrid approach: R&D examples

- Thinned high-resistivity fully depleted sensors
  - Several producers can make ~50 µm thick silicon sensors (e.g. IZM, Micron, CNM)
  - Handling + flip-chip bonding is a concern, in particular for larger structures

- Fast, low-power readout ASICs in Very-Deep-Sub-Micron (VDSM) technology
  - Timepix3 ~2013: 130 nm IBM CMOS, 55 µm^2 pitch
  - SmallPix ~2013: 130 nm IBM CMOS, ~40 µm^2 pitch (medical applications)
  - CLICPix ~2015: 65 nm, 25 µm^2 pitch

  → CLICPix demonstrator prototypes ~2013: 64x64 pixel array

- Low-mass interconnects and pixel connectivity
  - Through Silicon Vias (TSV):
    - fan out ASIC contacts to backside through vertical conducting channel
    - avoids dead areas from wire-bonding pads around the chips
    - Example: CEA-Leti via-last process with Medipix 3, prototypes under test
  - Lateral interconnectivity
    - Edgeless sensors
    - Stitching of neighboring chips

Silicon device simulation with TCAD

- Thin sensors (~50 µm) + small pitch (20-25 µm^2) + fast shaping + digitization

→ Need to investigate:

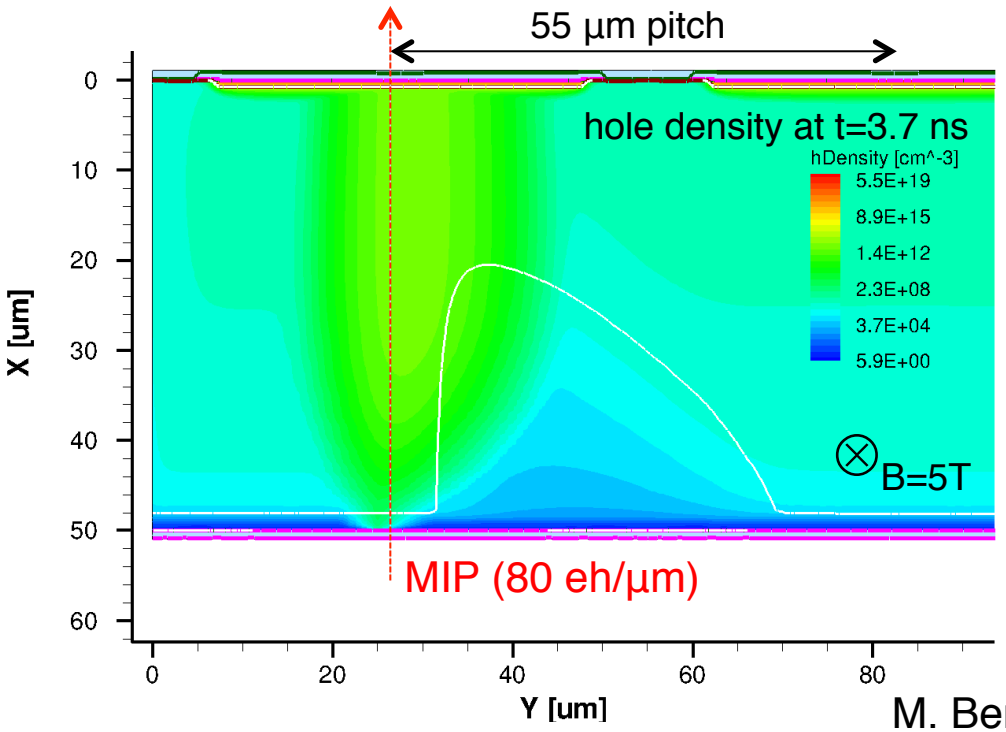
  - Charge rise time, collection efficiency, sharing between pixels, signal/noise
  - Dependence on momentum, angle, electric field
  - Lorentz-angle effects from magnetic field

- Use TCAD process and device simulation
- Results to be validated with prototypes in test beam

Example:
Hybrid detector with Timepix readout

p-in-n sensor (10 kOhm cm)
50 µm thickness
55 µm readout pitch
V_{bias}=10 V
Magnetic field: 5 T

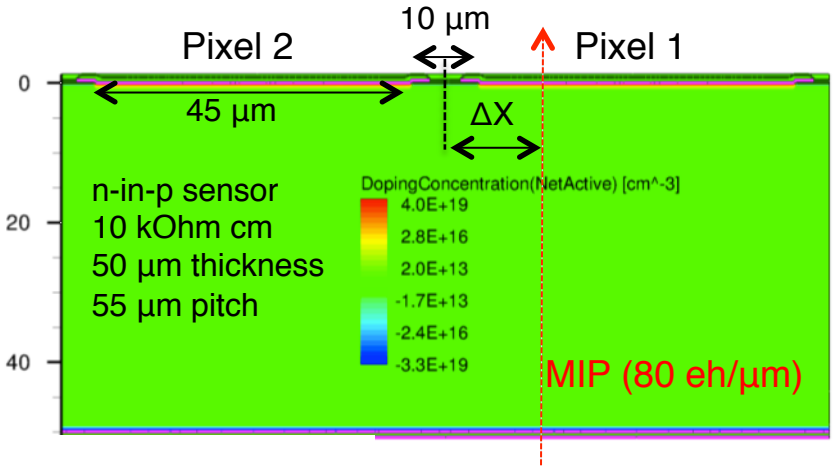
- Spread of charge cloud due to Lorentz-angle effect
- Effect more pronounced for electrons
- Can be partially compensated by rotation of sensors with Lorentz angle
- Over-depletion reduces effect

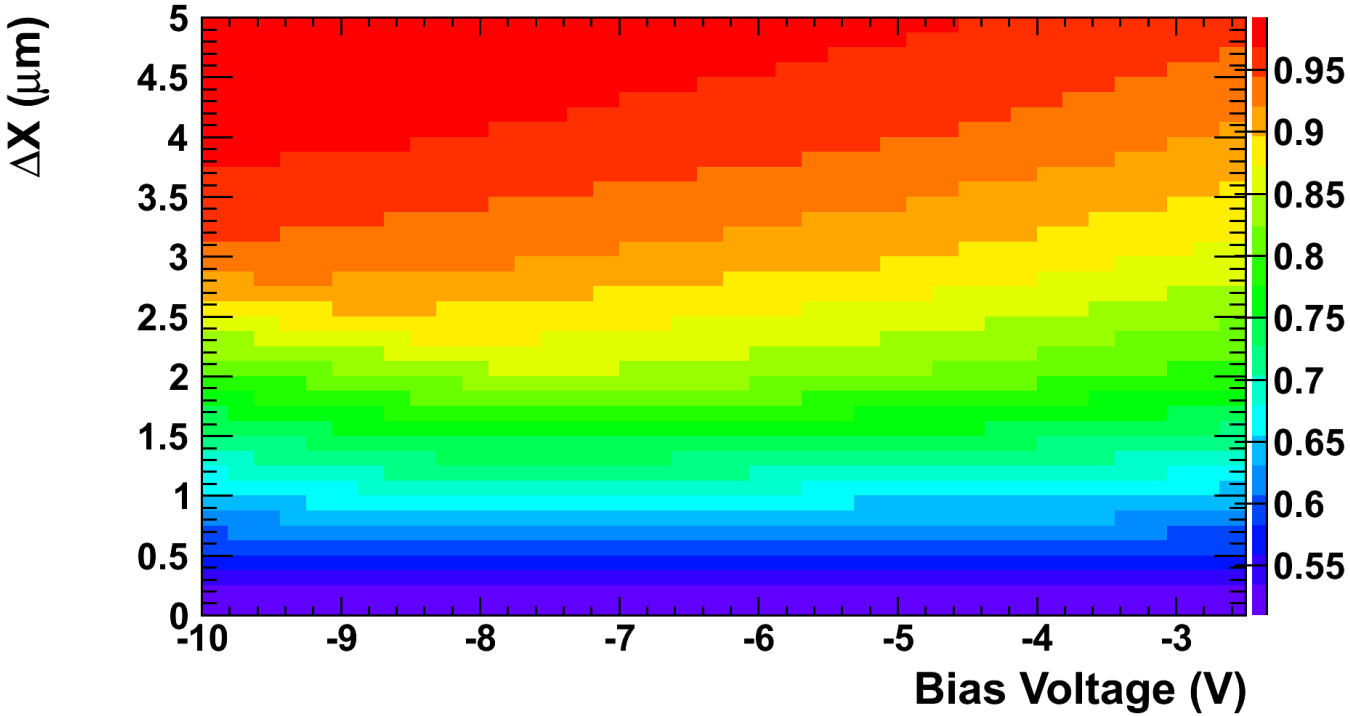


M. Benoit

Charge sharing

- Charge spread in sensor leads to sharing of charge between neighboring pixels
- Over-depletion increases E-field, thereby reduces charge spread and charge sharing
- Charge sharing can improve resolution through interpolation (with analog readout)
- However: signals below threshold are lost





Fraction of total signal collected in pixel 1

Signal rise time

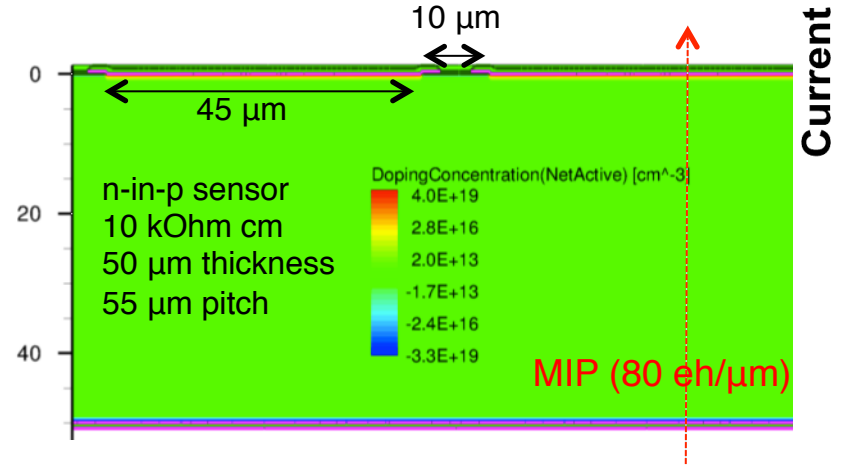
- Need time-stamping precision of ~10 ns, to suppress beam-induced backgrounds

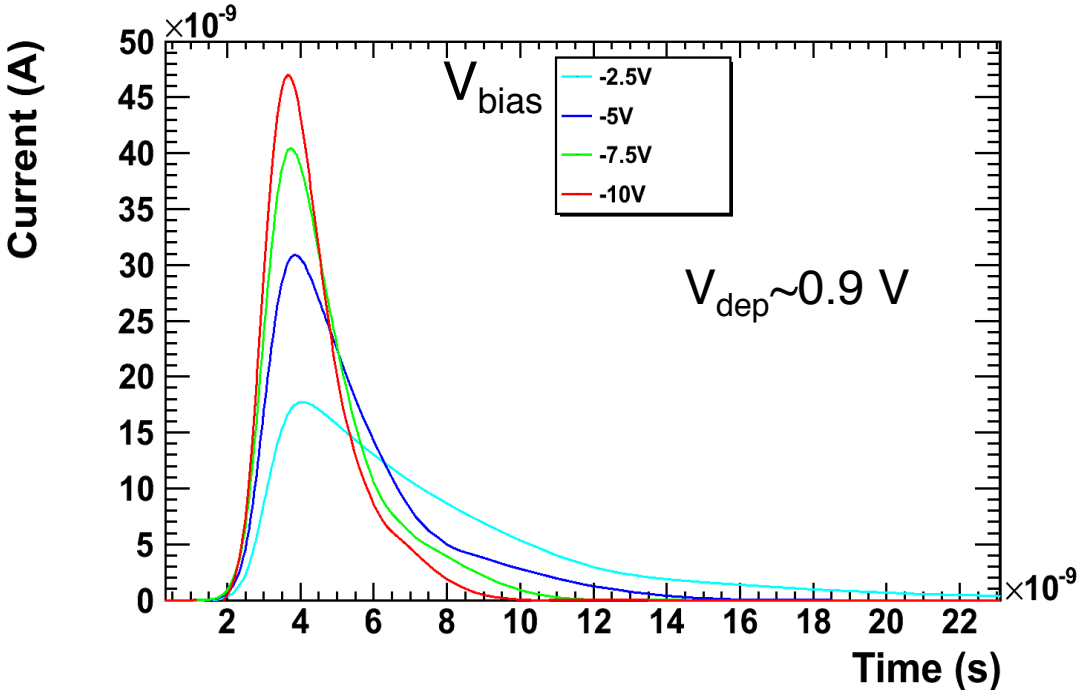
→ Peaking time in sensor should be <<10 ns, to optimize S/N and reduce effect of time walk

- electron collection faster than holes → favors n-in-p sensors

Example:

- 55 x 55 µm^2 pixels
- 50 µm thinned n-in-p sensor, ρ=10 kOhm cm
- ~2 ns peaking time with weak dependence on V_{bias}
- For higher V_{bias} better S/N expected after shaping, due to higher peak value; also less time walk due to reduced dispersion





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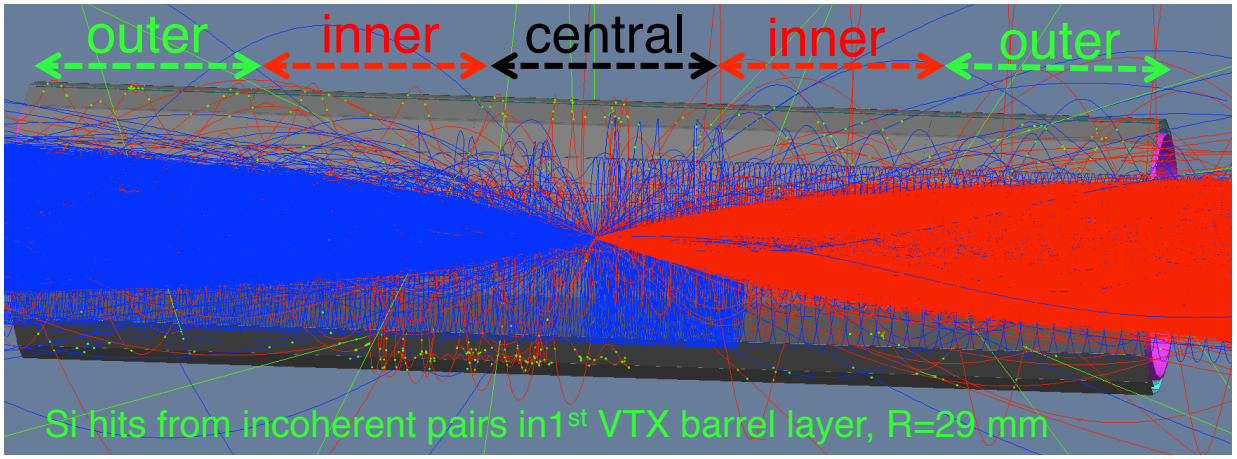
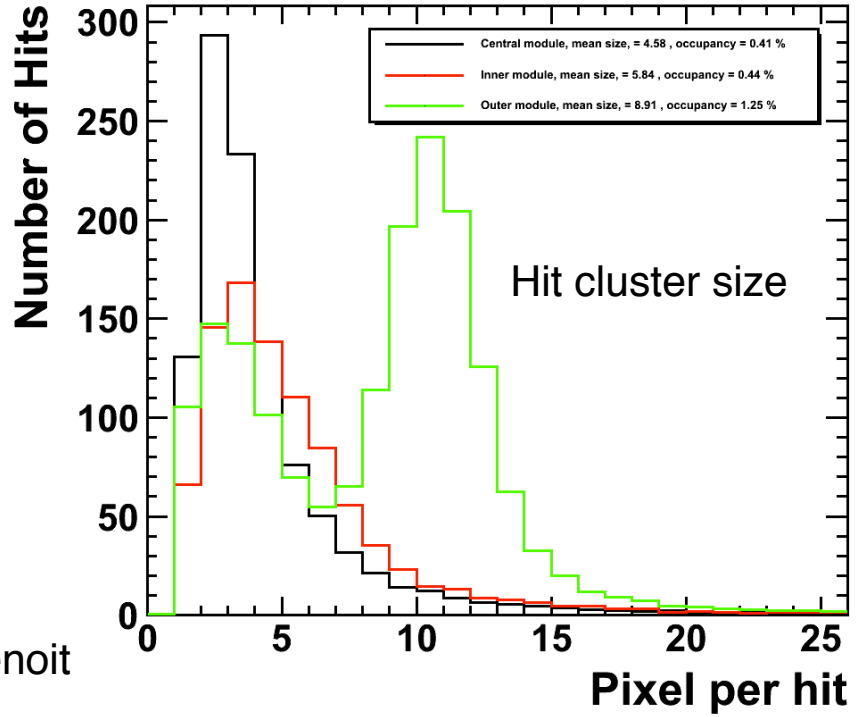
Background simulation with realistic clustering

- Incoherent pairs in post-CDR CLIC_ILD vertex detector model
- 50 µm sensor n-in-p
- Timepix-like readout
- AllPix + MAFALDA framework for digitization + reconstruction
- EM Liverpool physics list, for low-energy, delta rays
- Uses parameterized input from TCAD + Testbeam results



- Observed cluster sizes for 20x20 µm pixels in innermost vertex barrel layer:
  - 5-10 hits per cluster, depending on theta (for CDR studies: assumed 5 hits)
  - Resulting train occupancies ~ 0.5%-1% (excluding safety factors)
- Next step: include γγ→hadrons

- Results can be used to improve full-detector simulation with overlay of backgrounds



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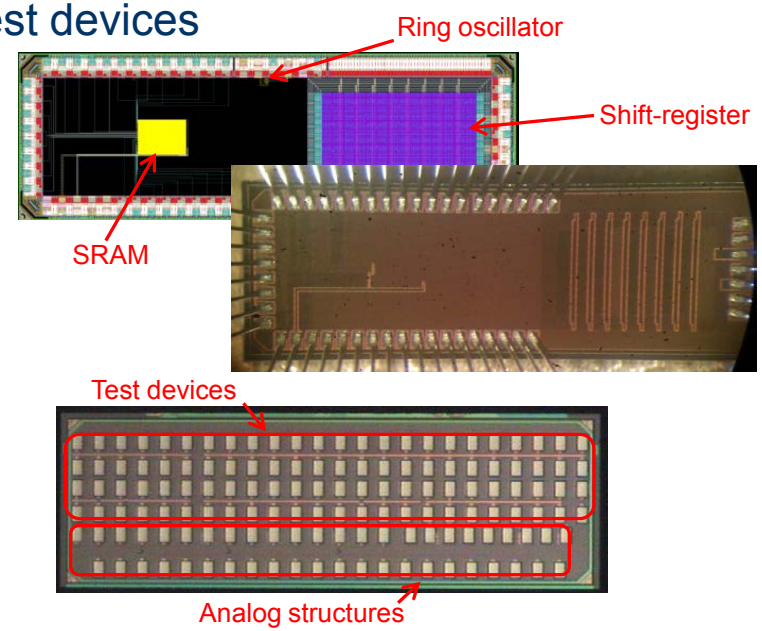
CLICPix 65 nm test structures

- 65 nm technology allows for performance improvements w.r.t. 130 nm:
  - Smaller pixel sizes (10-30% less area for analog part, 60% less for digital part)
  - More functionality in each pixel
  - Lower noise (due to lower capacitances)
- Test structures produced in 65 nm multi-project wafer run:

  - Radiation and functional tests
  - Total size: 3x4 mm
  - Divided in three sub-chips:
  - 1 chip for analog structures and test devices
    - 1 pad per multiple gates
    - Analog structures
  - 1 chip w/ test structure/devices
    - 1 pad per gate
    - 142 total pins
  - 1 chip for digital logic
    - 64 kbit Shift-register
    - 56kbit Memory
    - Ring oscillator (1025 gates)



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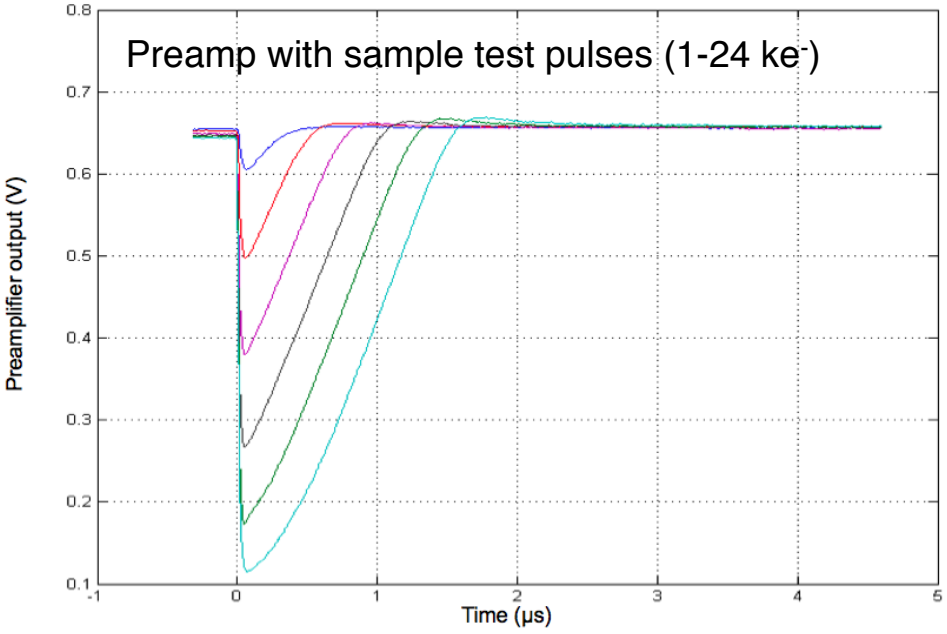
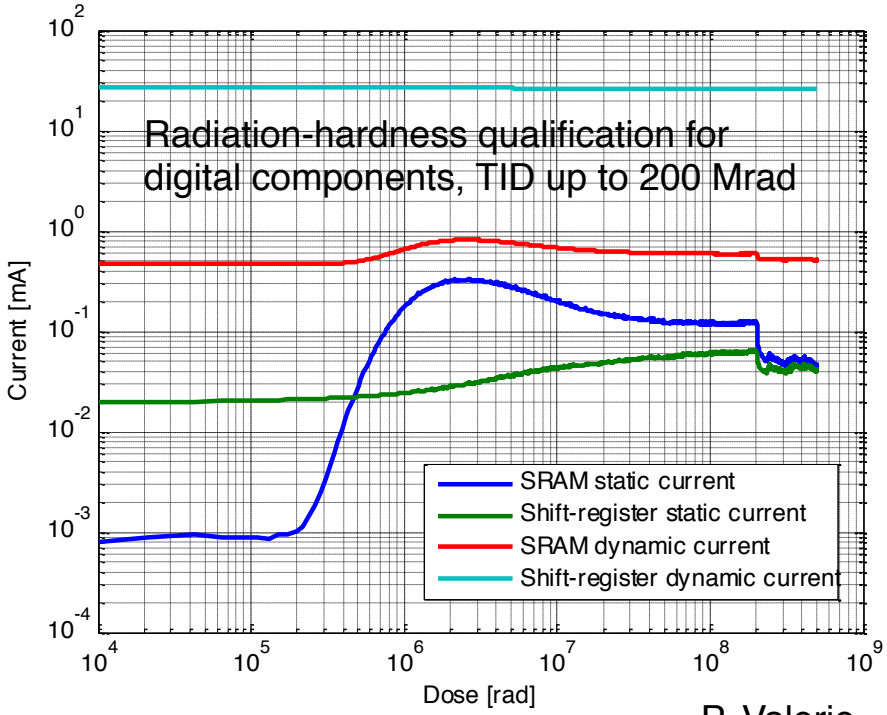
CLICPix 65 nm test structures: results

- Measurements on Test pixels
- Results according to simulations
- Improved radiation tolerance w.r.t. 130 nm observed (TID up 200 Mrad and SEU)
- Results allow for projections to CLICPix performance (e.g. power consumption digital part)

Preamp measurements:

	Simulations	Measurements
Rise time	50ns	65ns
Gain	30mV/ke$^-$	29.1mV/ke$^-$
Linearity	5% at 16ke-	5% at 15ke$^-$
Noise	55e$^-$	60e$^-$ (70e$^-$ for ELT channel)





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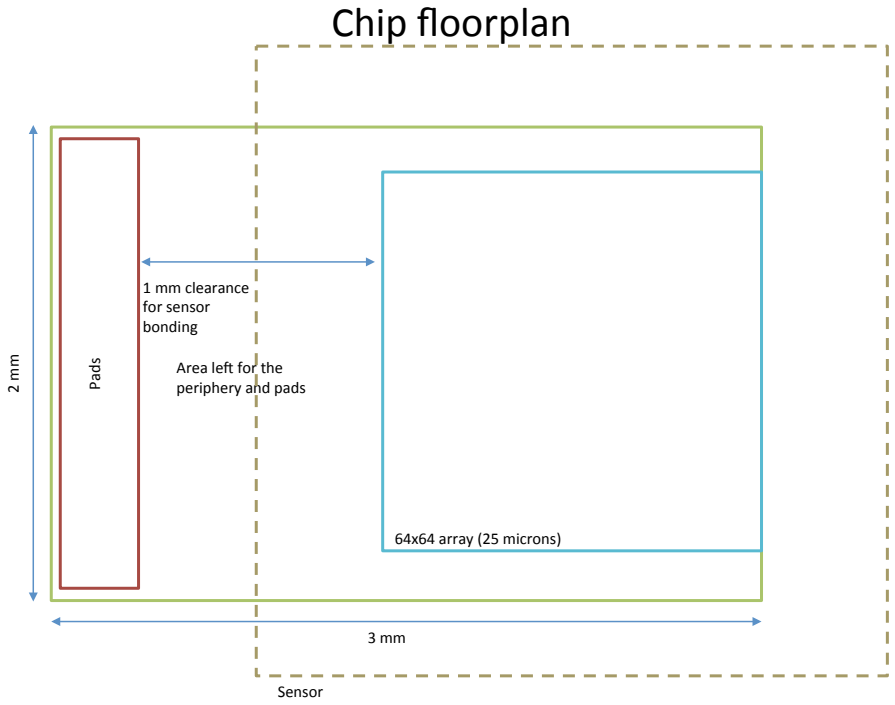
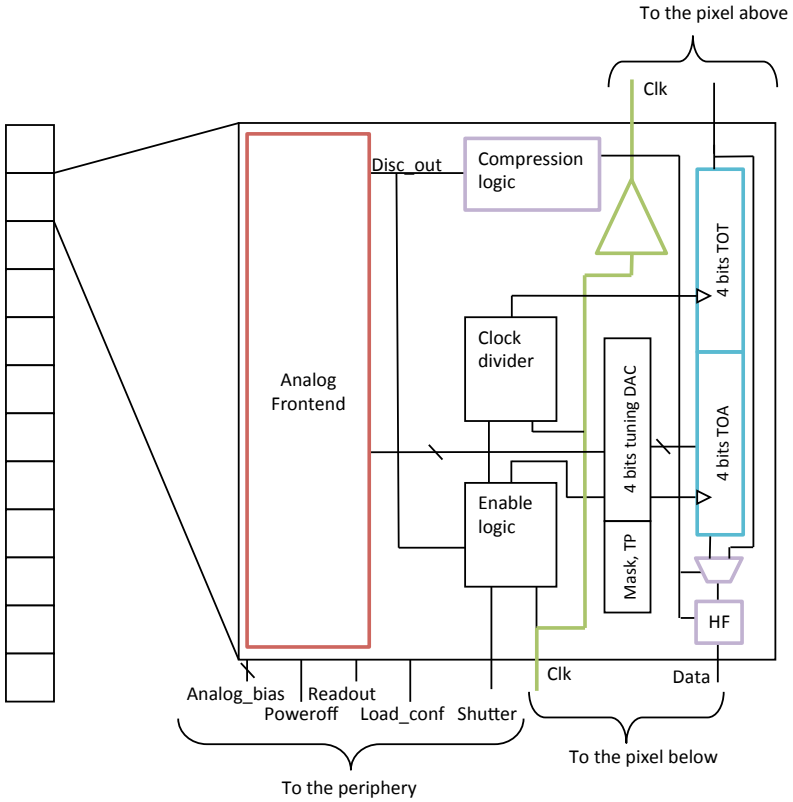
CLICPix 65 nm demonstrator chip

Demonstrator chip for next 65 nm MPWR

- First prototype with full pixel-readout functionality
- Submission 2nd half of 2012
- Includes 64 x 64 pixel array with 25 µm pitch
- Will try to bond to sensor





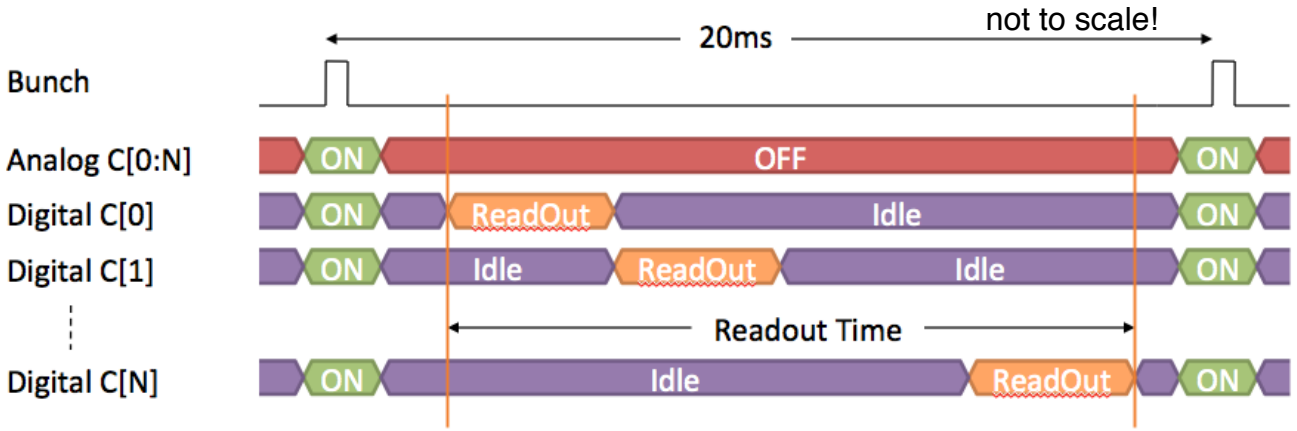
- simultaneous 4-bits TOA and 4-bits TOT measurements per pixel (100 MHz reference clock)
- Compression logic allows for sparse readout; Cluster-based compression is being evaluated
- Power saving techniques include clock gating when the pixel is not being read out and power gating (with an external signal) for the analog part when the chip is not acquiring data

P. Valerio, X. Llopart

CLICPix power-pulsing requirements

- Overall power budget (driven by air-flow cooling): $P_{avg} \sim 50$ mW / cm^2
- Estimation of power consumption for analog and digital blocks of CLICPix readout chip
- Based on measurements with 65 nm test-chip and projections from current TimePix
- Power pulsing with On/Idle/Off states, to reduce average power consumption
- Very small duty cycle for analog power is major challenge for design of power delivery/pulsing

→ Requires local energy storage



Bunch Train (3.0 W/cm²)	
Pixel Analog	ON
Pixel Digital	ON
Periphery Analog	ON
Periphery Digital	ON
IO LVDS Pads	OFF

Chip Readout (360 mW/cm²)	
Pixel Analog	OFF
Pixel Digital	ON
Periphery Analog	OFF
Periphery Digital	ON
IO LVDS Pads	ON

Idle (7.8 mW/cm²)	
Pixel Analog	OFF
Pixel Digital	Idle
Periphery Analog	OFF
Periphery Digital	ON
IO LVDS Pads	OFF

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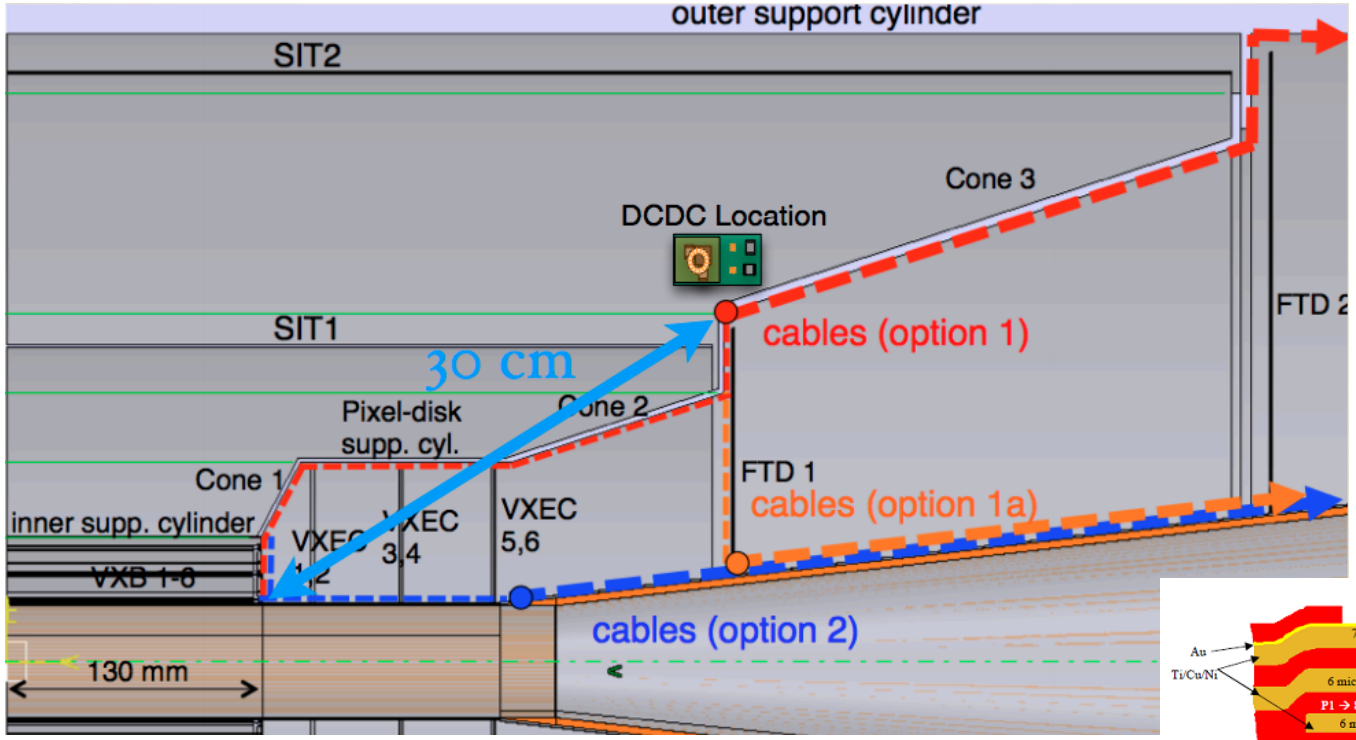
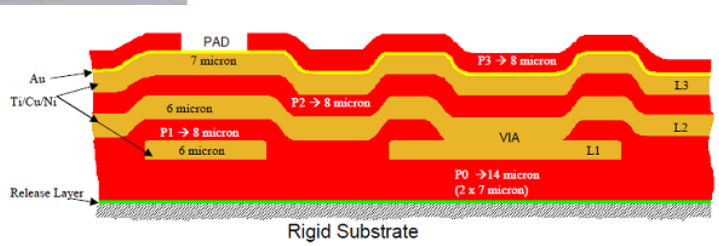
Power delivery concept

- DC/DC converters outside pixel-sensor area
- Power pulsing, to reduce average power consumption
- Flexible Kapton cables for power delivery, controls, readout
- Cabling along ladders integrated in chips (stitching across modules)



HighTec™ flex Kapton

- Cu on Polyimide
- ~20-50 µm total thickness
- Aim: replace Cu with Al
  → x3.7 less rad. length
  for same conductivity

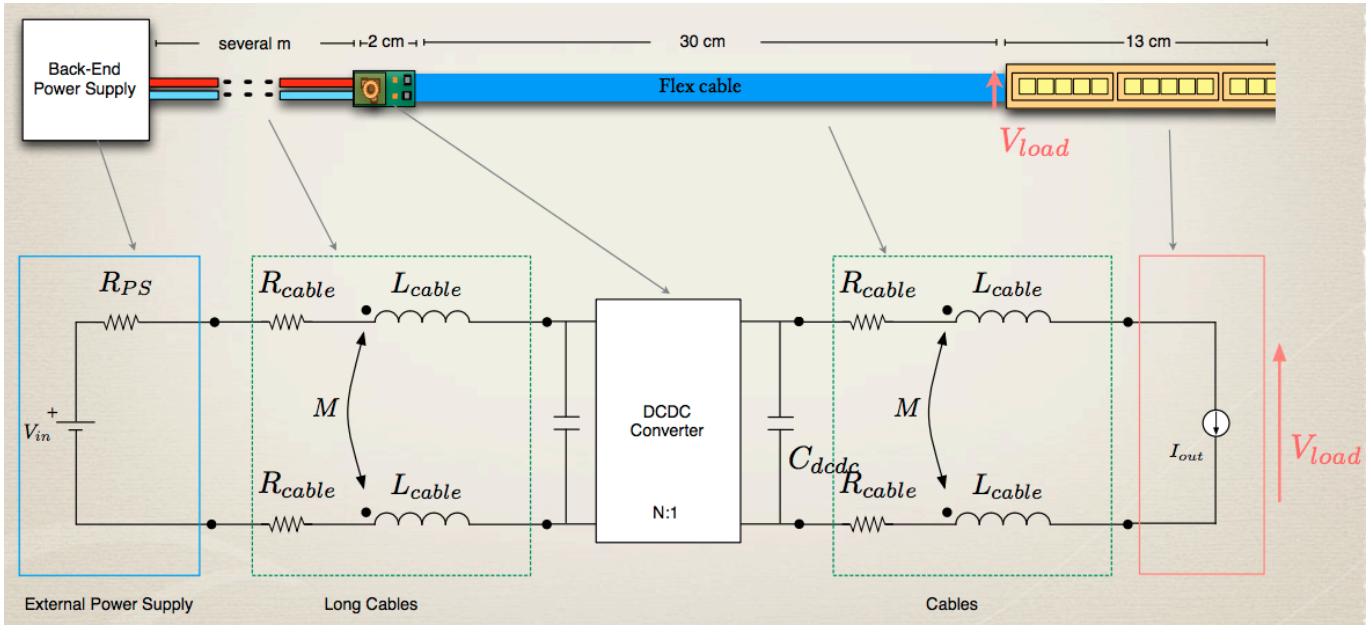


Main challenges:

- Cabling has to cope with large and short current peaks in chips (small duty cycle of CLIC machine)
- Combine DC/DC with power pulsing (possibly including local energy storage on the staves)
- Has to work in magnetic field: B = 4-5 T
- Large currents along ladders: stitching technology not established yet

C. Fuentes
G. Blanchot

Power delivery simulations



Spice simulation of powering for analog components of CLIC_ILD barrel pixel ½ ladder

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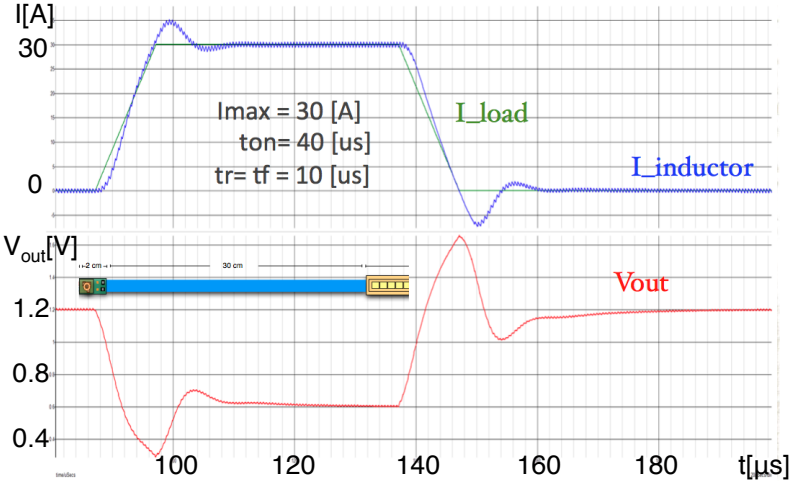
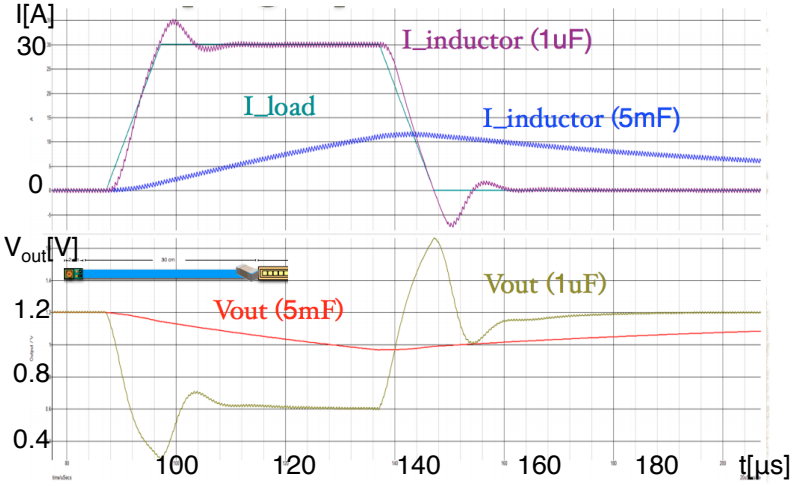
G. Blanchot





- Decoupling capacitor close to load helps to reduce spikes + drop in load voltage and to level cable currents
- Realistic simulation of transient behavior needs to take into account details of chip response

Cooling

- P~500 W in vertex detectors (50 mW/cm^2)
- Need efficient cooling, meeting material budget requirements
- Several options considered:

Forced (dry) air flow

- baseline for barrel region
- no extra material

→ following talk by Hubert Gerwig in this session:
http://ilcagenda.linearcollider.org/contributionDisplay.py?sessionId=20&contribId=57&confId=5414

Evaporative CO_2 cooling

- Option for supplementary cooling in forward disks
- High pressure up to ~70 bar, requires rather thick tubing
- ~2.7 % X_0 per tube (incl. coolant)

Water cooling

- Option for supplementary cooling in forward disks
- Sub-atmospheric pressure
- Can use thin PEEK pipes → lower material budget than CO_2, ~0.4% X_0 per tube

Micro-channel cooling

- Ongoing R&D (e.g. NA62 Gigatracker upgrade)
- Integrate cooling channels in Silicon
- Connectors pose major challenge

Summary / conclusions

- CLIC environment + physics requirements pose challenging demands on vertex-detector systems

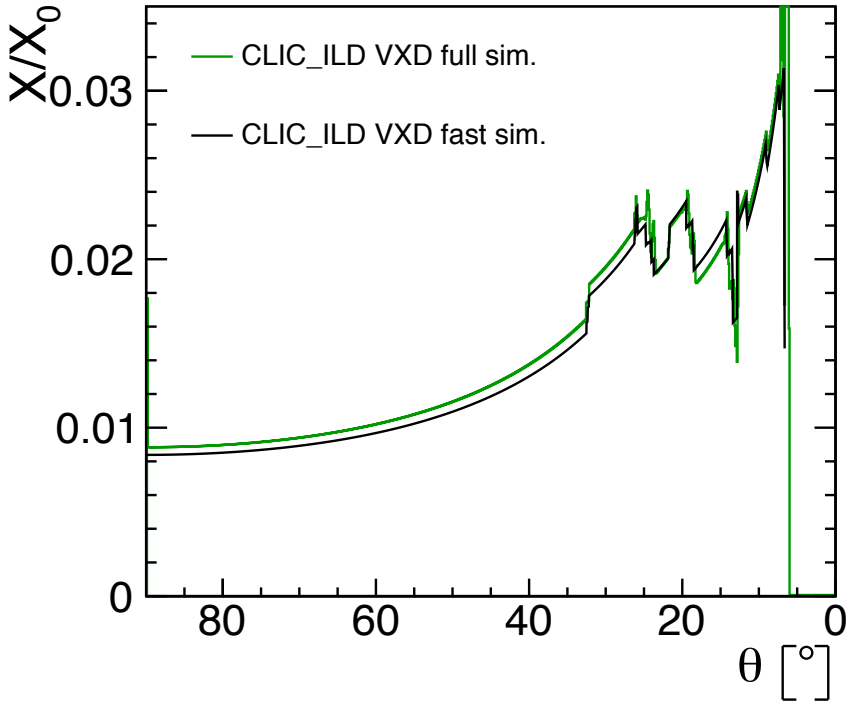
- Presented initial layout proposals meeting those demands

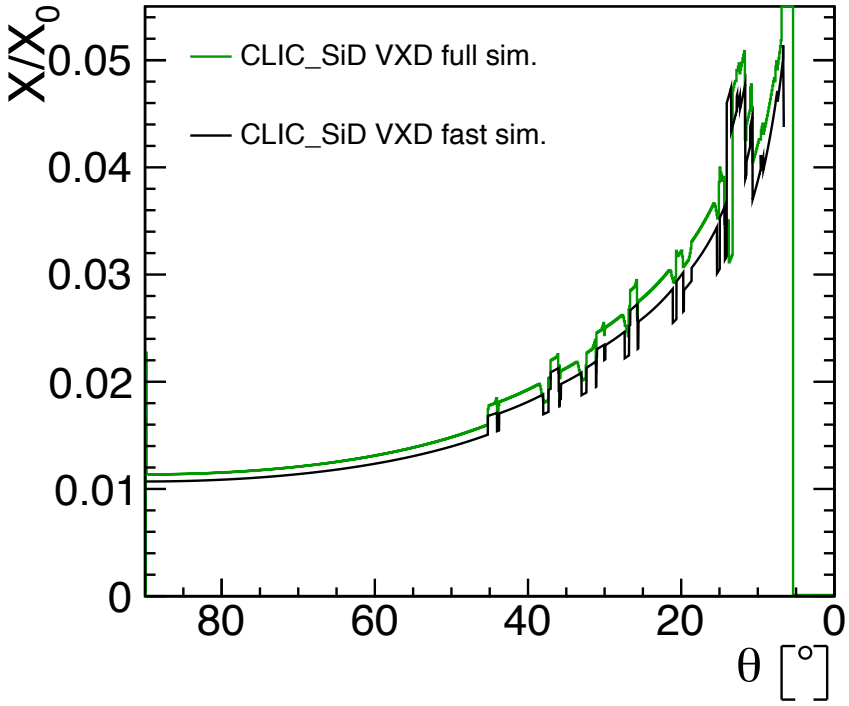
- Examples for active R&D on:
  - sensor + readout technologies
  - Mechanics, cooling
  - Power-delivery and power pulsing

- More details in CLIC vertex-detector working group presentations: http://indico.cern.ch/categoryDisplay.py?categId=2843 and in CDR: http://lcd.web.cern.ch/LCD/CDR/CDR.html

Backup slides

Material budget vertex region





- Integrated amount of material seen by particles originating from the IP:
  $X/X_0 \sim 1\%$ (at $\theta=90^o$, averaged over ϕ)
- Good agreement full / fast simulation
  (fast simulation has only ideal cylinders and disks, no module overlaps)

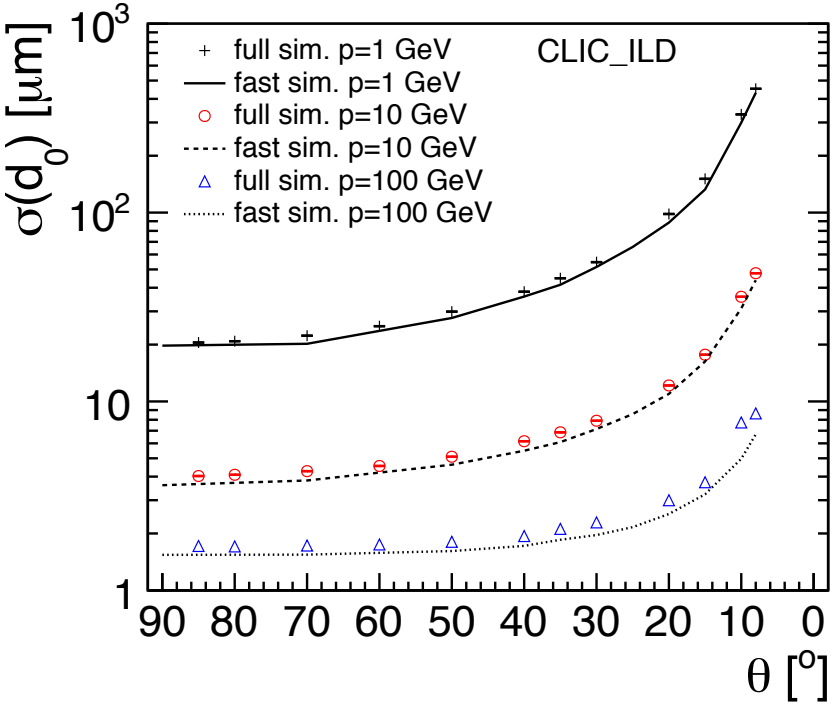
Transverse impact-parameter resolution

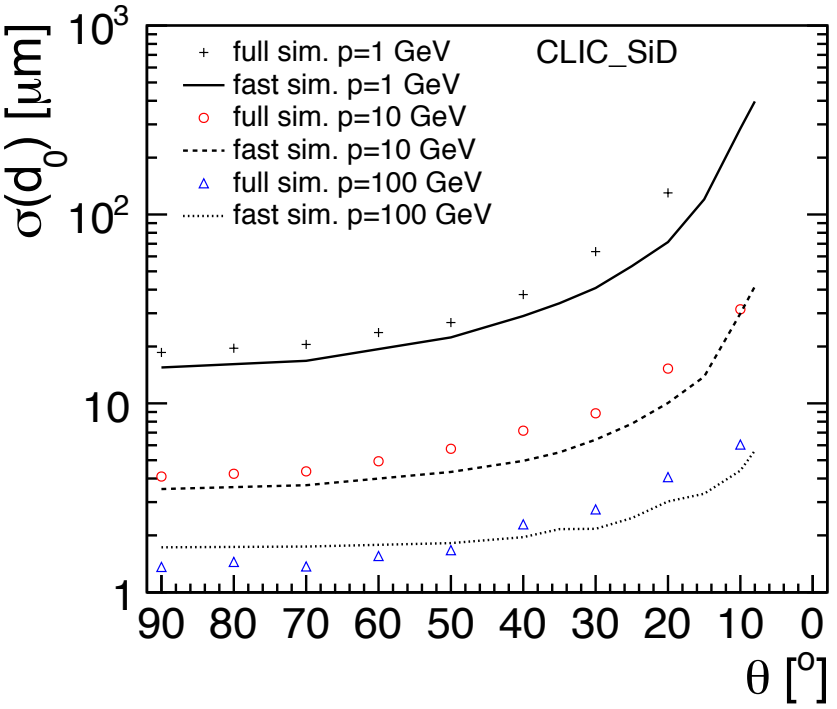
d_0: distance of closest approach to interaction point in R-phi plane

→ main benchmark parameter for vertex detector performance

Fast simulation: LiC detector toy tool, used for design optimization

Full simulation: Geant4-based ILD/SiD frameworks, used for physics studies





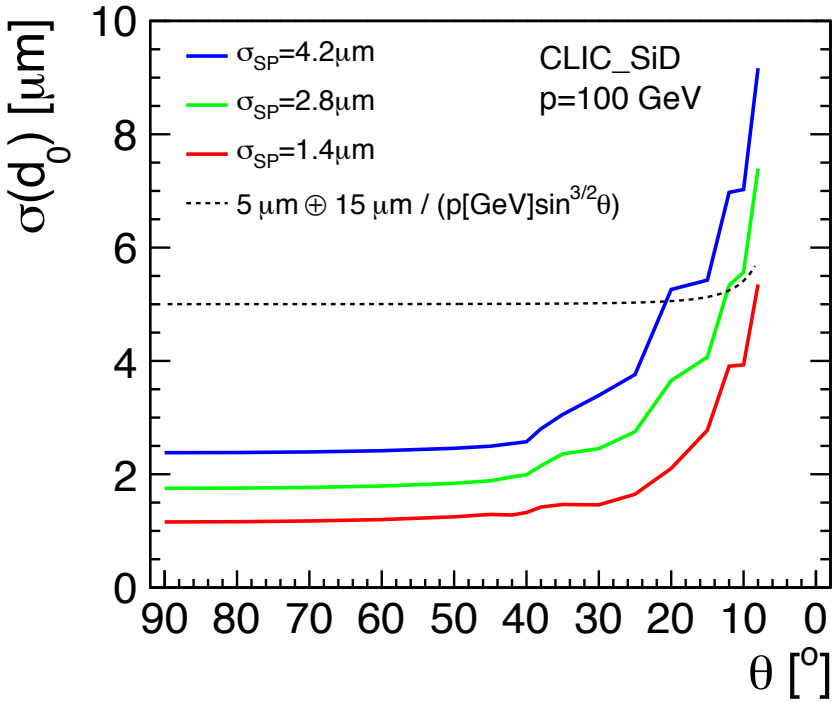
CLIC_ILD:

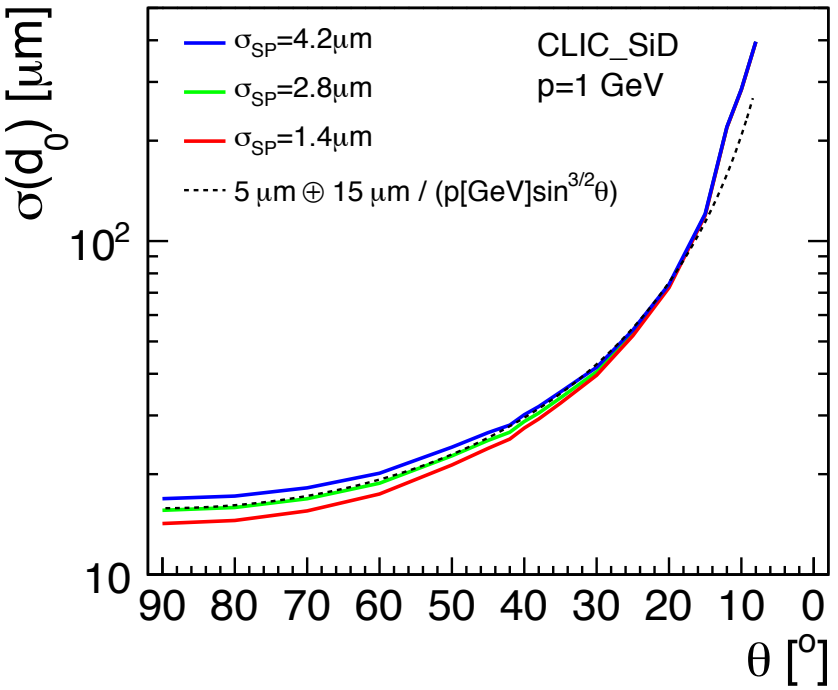
- Both full and fast simulation perform simple Gaussian hit smearing
- Very good agreement between full/fast simulations

CLIC_SiD:

- Full simulation models clustering according to parametrization of KPiX readout chip → added realism leads to worse resolution in full simulation, as expected

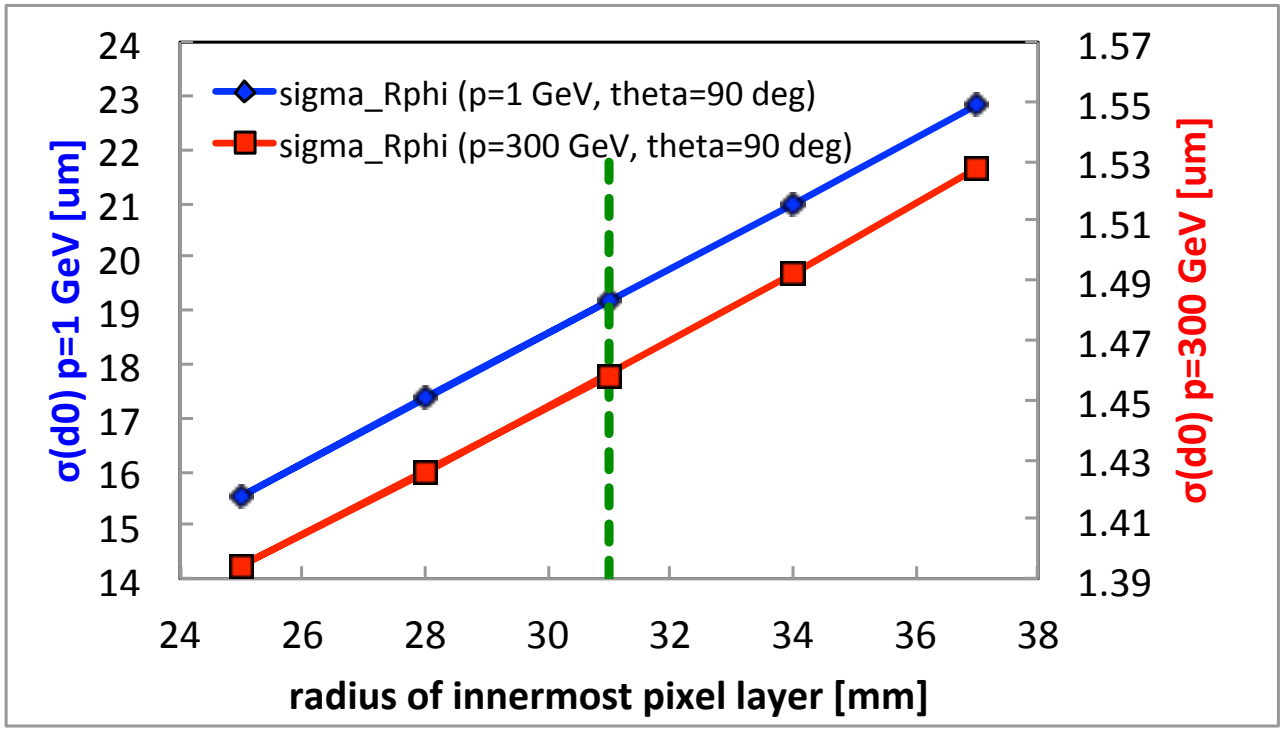
Dependence on single-point resolution





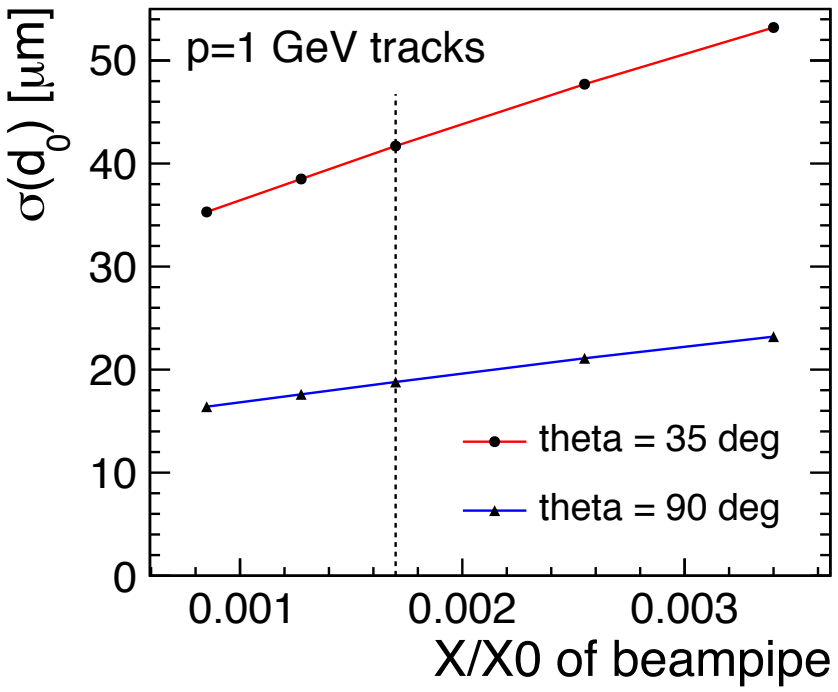
- Varied single-point resolution by +- 50% (~ pixel sizes 10x10, 20x20, 30x30 μm²)
- Observed change in d_0-resolution:
  - +- 40% for p = 100 GeV
  - +- 15% for p = 1 GeV
- Resolution close to or better than target values for all cases
- Pixel size is also constrained by:
  - Expected background occupancy
  - Ability to separate adjacent tracks in dense jets

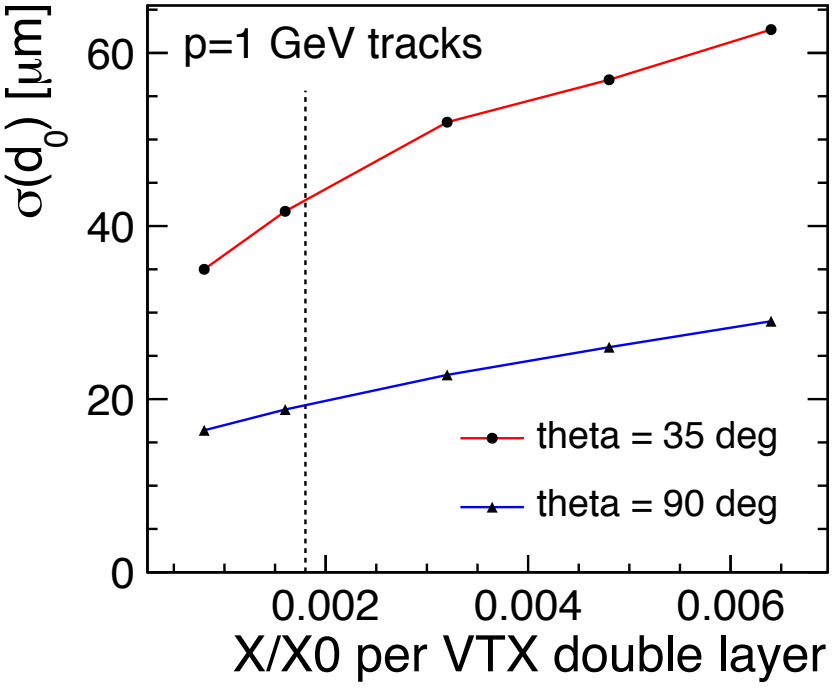
Dependence on distance to IP



- Varied distance to interaction point, by changing radii of beam pipe and barrel vertex layers in CLIC_ILD model
- Observed change in d_0-resolution:
  - 3.2% / mm for high momenta (parameter 'a')
  - 0.8% / mm for low momenta (parameter 'b')
- Distance to interaction point is constrained by direct hits from incoherent pairs

Dependence on material





- Very small amount of material in baseline designs
- Realistic models for supports, cabling, cooling not available yet
- Studied sensitivity of d_0 resolution for low momenta on material in beampipe and silicon pixel layers of CLIC_ILD
- Doubling beam-pipe thickness → ~20% worse resolution at 90°
- Doubling material in silicon layers → ~20% worse resolution at 90°
- Steeper slope in forward region

Examples for Integrated Approach

- Active R&D programs for integrated technologies, targeted to ILC requirements
- Attempts to reach faster signal collection and ~ns time-stamping capability, compatible with CLIC requirements:
  - MIMOSA CMOS chip family (currently 350 nm) in STAR, EUDET Telescope
    → developing high-resistivity epitaxial layers, smaller feature sizes
  - Chronopixel CMOS sensors with fully depleted epitaxial layer
  - INMAPS technology: deep p-well barrier protects n-well charge collector, improves charge collection, allows for high-resistivity epitaxial layer and full-featured CMOS MAPS technology
  - High-voltage CMOS: CMOS signal processing electronics embedded in reverse-biased deep n-well that acts as signal collecting electrode
  - Silicon-On-Insulator (SOI): ~200 nm SiO_2 isolation layer separates charge collection and readout functionality
  - Full 3D-integrated pixel solutions: Thinned high-resistivity sensitive tier coupled to additional tiers with advanced analog+digital functionality

- Concerns for CLIC:
  - Long-term availability of processes
  - Suitability for large-scale systems

  → prefer staged developments and synergy with industrial trends