High resolution vertexing based on CMOS sensors with microsecond time stamping

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- Sensor design : coll. with IRFU-Saclay -

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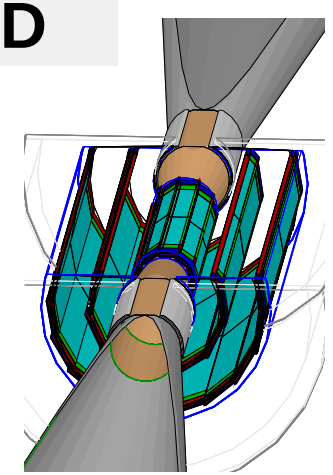
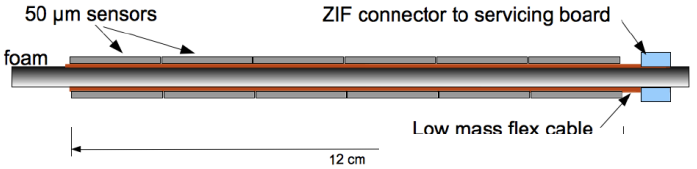
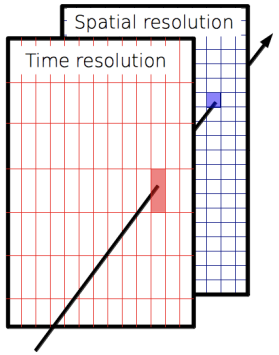
CMOS Pixel Sensors for the ILD-VXD



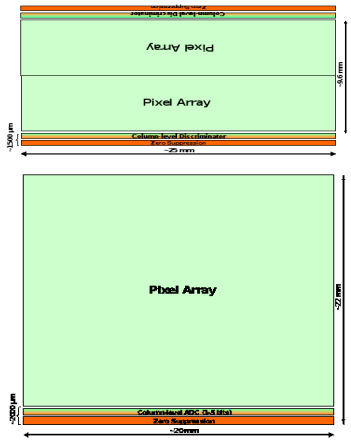
- **Two types of CMOS Pixel Sensors (CPS):**
  - ⁕ **Inner layers** ($\lesssim$ 300 cm^2) : priority to read-out speed & spatial resolution
    - ↪ small pixels (16×16 / 80 μm^2) with binary charge encoding
      - ↪ $t_{r.o.} \sim$ 50 / 10 μs; $\sigma_{sp} \lesssim$ 3 / 6 μm
  - ⁕ **Outer layers** ($\sim$ 3000 cm^2) : priority to power consumption and good resolution
    - ↪ large pixels (35×35 μm^2) with 3-4 bits charge encoding
      - ↪ $t_{r.o.} \sim$ 100 μs; $\sigma_{sp} \lesssim$ 4 μm
  - ⁕ Total VXD instantaneous/average power $<$ 700/20 W (0.35 μm process)



- **2-sided ladder concept for inner layer :**
  - ⁕ *S*quare pixels (16×16 μm^2) on internal ladder face ($\sigma_{sp} < 3\ \mu m$)
    & *E*longated pixels (16×80 μm^2) on external ladder face ($t_{r.o.} \sim 10\ \mu s$)

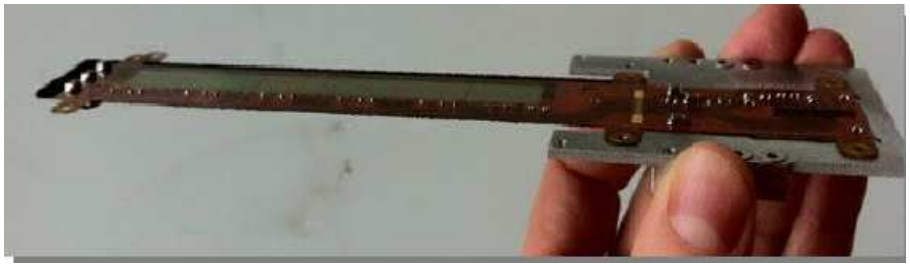


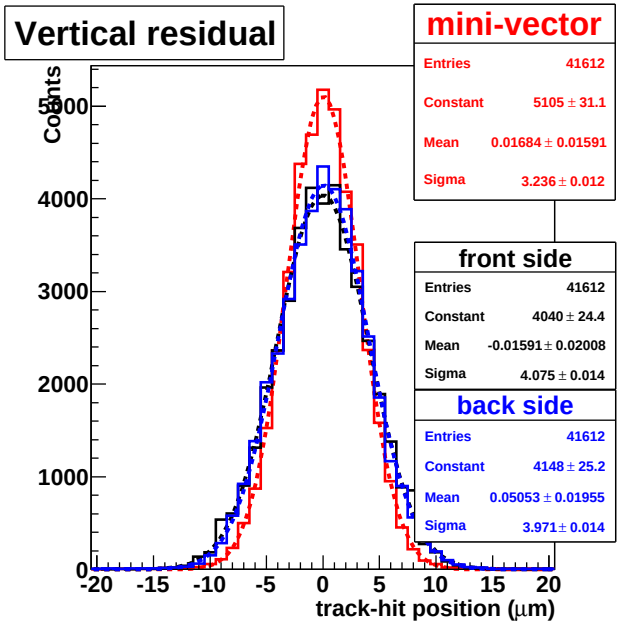
- **Sensor final prototypes :** fabricated in Q4/2011
  - ⁕ **MIMOSA-30:** inner layer prototype with 2-sided read-out ▷ ▷ ▷
    - ↪ one side : 256 pixels (16×16 μm^2)
      other side : 64 pixels (16×64 μm^2)
  - ⁕ **MIMOSA-31:** outer layer prototype ▷ ▷ ▷
    - ↪ 48 col. of 64 pixels (35×35 μm^2) ended with 4-bit ADC

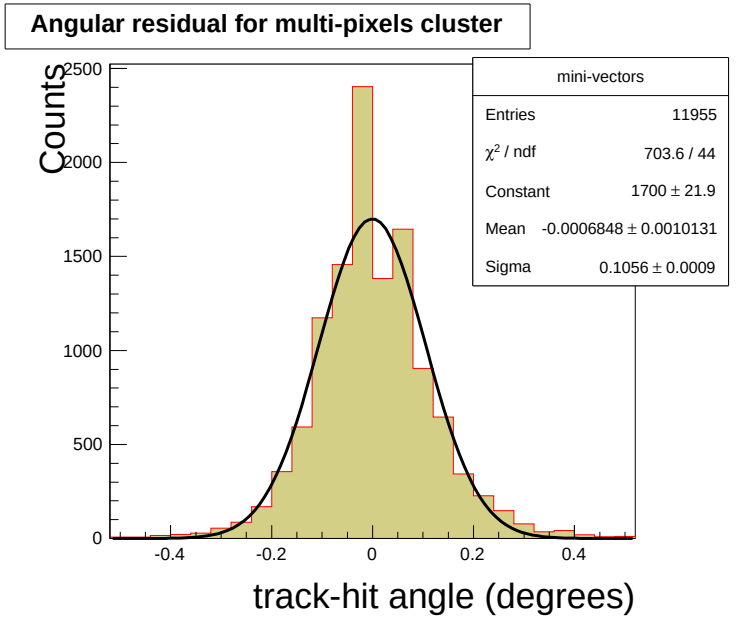


2-Sided Ladder Beam Test Results

- **PLUME prototype-2010 tested at SPS in Nov. 2011:**
  - ⁂ *Beam telescope : 2 arms, each composed of 2 MIMOSA-26 sensors*
  - ⁂ *DUT : 1 PLUME ladder prototype (0.6 % X_0)*
    - ⟶ *6 MIMOSA-26 sensors on each ladder face (8 Mpixels)*
  - ⁂ *CERN-SPS beam : $\gtrsim$ 100 GeV "π^-" beam*
  - ⁂ *BT (track extrapolation) resolution on DUT : $\sim$ 1.8 μm*
  - ⁂ *Studies with PLUME perpendicular and inclined ($\sim 36^\circ$) w.r.t. beam line*
  - ⁂ *Preliminary results (no pick-up observed): combined impact resolution & pointing resolution*



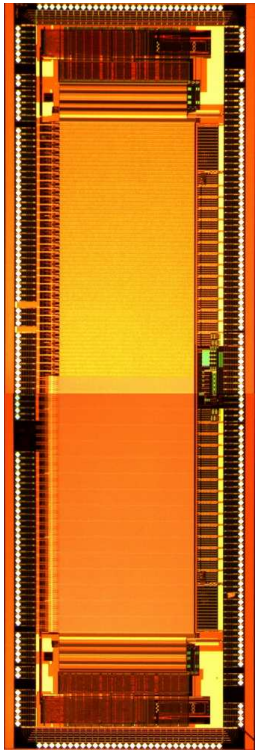




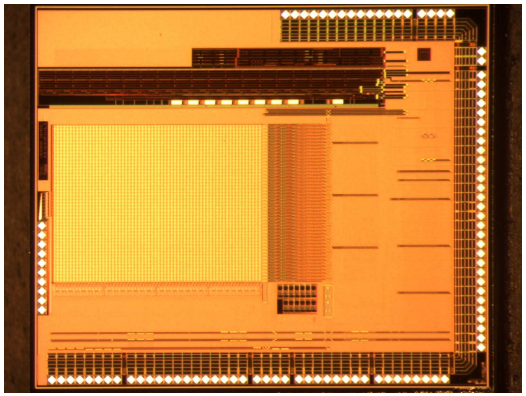
- **New PLUME prototype under construction with 0.35 % X0** (X-section) ⟼ **beam tests in Q4/2012**

CMOS Pixel Sensors: Status of Baseline Devt

- **MIMOSA-30: prototype for ILD-VXD innermost layer** ▷ ▷ ▷
  - ⁂ 0.35 CMOS μm process with high-resistivity epitaxy
  - ⁂ in-pixel CDS, rolling shutter read-out, binary sparsified output
  - ⁂ **high resolution side : pixels of 16×16 μm^2 ⇛ expect $\sigma_{sp} < 3\ \mu m$**
    - 128 columns (discri) & 8 col. (analog) of 256 rows (final scale)
    - read-out time $\lesssim 50\ \mu s$
  - ⁂ **time stamping side : pixels of 16×64 μm^2 ⇛ $t_{r.o.} \sim$ 10 μs**
    - (expect $\sigma_{sp} \sim 6\ \mu m$)
    - 128 columns (discri) and 8 col. (analog) of 64 rows (final scale)
    - lab tests positive : N $\sim$ 15 e^- ENC & discri. all OK for $t_{r.o.} = 10 \mu s$
  - ⁂ beam tests (CERN-SPS) in June/July '12 ⇛ σ_{sp}, ϵ_{det}, fake rate



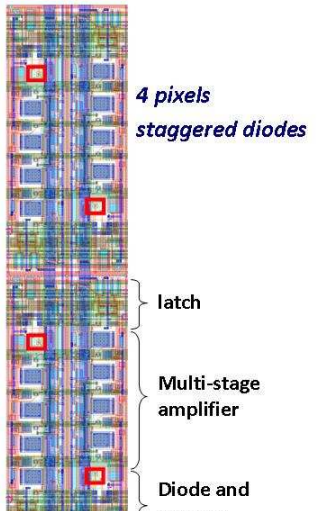
- **MIMOSA-31: prototype for ILD-VXD outer layers** ▷ ▷ ▷
  - ⁂ pixels of 35×35 μm^2 (power saving)
  - ⁂ 48 columns of 64 pixels ended with 4-bit ADC (1/10 of full scale chip)
    ↪ expect $\sigma_{sp} \lesssim 3.5\ \mu m$
  - ⁂ $t_{r.o.} \sim 10\ \mu s$ (1/10 of full scale chip)
  - ⁂ beam tests (DESY) in Q1/2013 ⇛ σ_{sp}, ϵ_{det}, fake rate

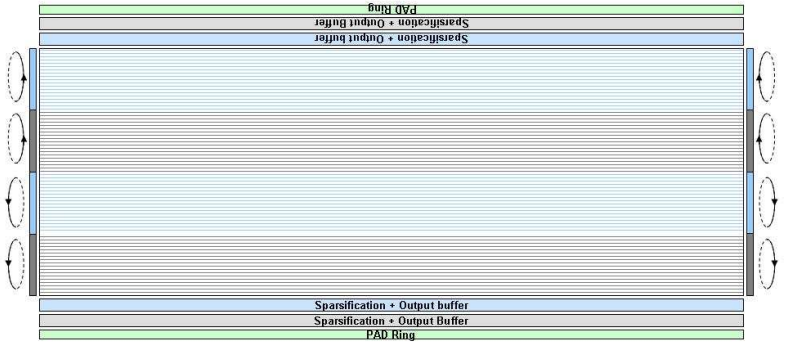


Read-Out Acceleration

- **Motivations**
  - ⁕ robustness w.r.t. predicted BG rate (keep small inner radius, no Anti-DID, ..)
  - ⁕ standalone inner tracking capability (e.g. soft tracks, SiD ?)
  - ⁕ compatibility with high-energy running: beam BG at $\sqrt{s} \gtrsim 1$ TeV
    - ↪ beam BG ($\gtrsim 1$ TeV) at least $3\times$BG (500 GeV)

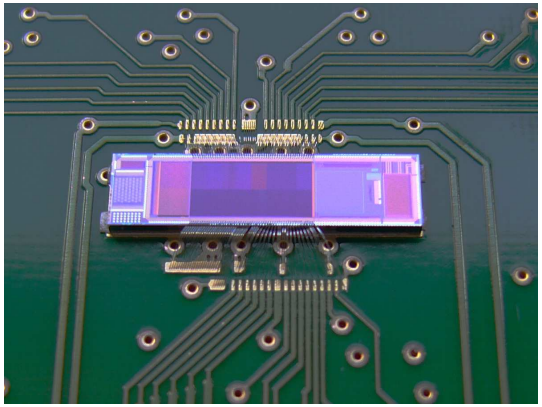
- **How to accelerate the elongated pixel read-out**
  - ⁕ elongated pixel dimensions allow for in-pixel discriminators ⇛ $\geq$ 2 faster r.o. ▷ ▷
  - ⁕ read out simultaneously 2 or 4 rows ⇛ 2-4 faster r.o./side
  - ⁕ subdivide pixel area in 4-8 sub-arrays read out in // ⇛ 2-4 faster r.o.
  - ▷ 0.18 μm CMOS process needed
    - ↪ 6-7 ML,, design compactness, in-pixel CMOS T, ...
  - ⁕ conservative step: 2 discri./column **end** (22 μm wide)
    - ⇛ read out 2 rows simultaneously
    - ↪ 1st stage improvement: 50/10 $\mu s \rightarrowtail$ 25/5 μs
    - (works even with 0.35 μm technology)

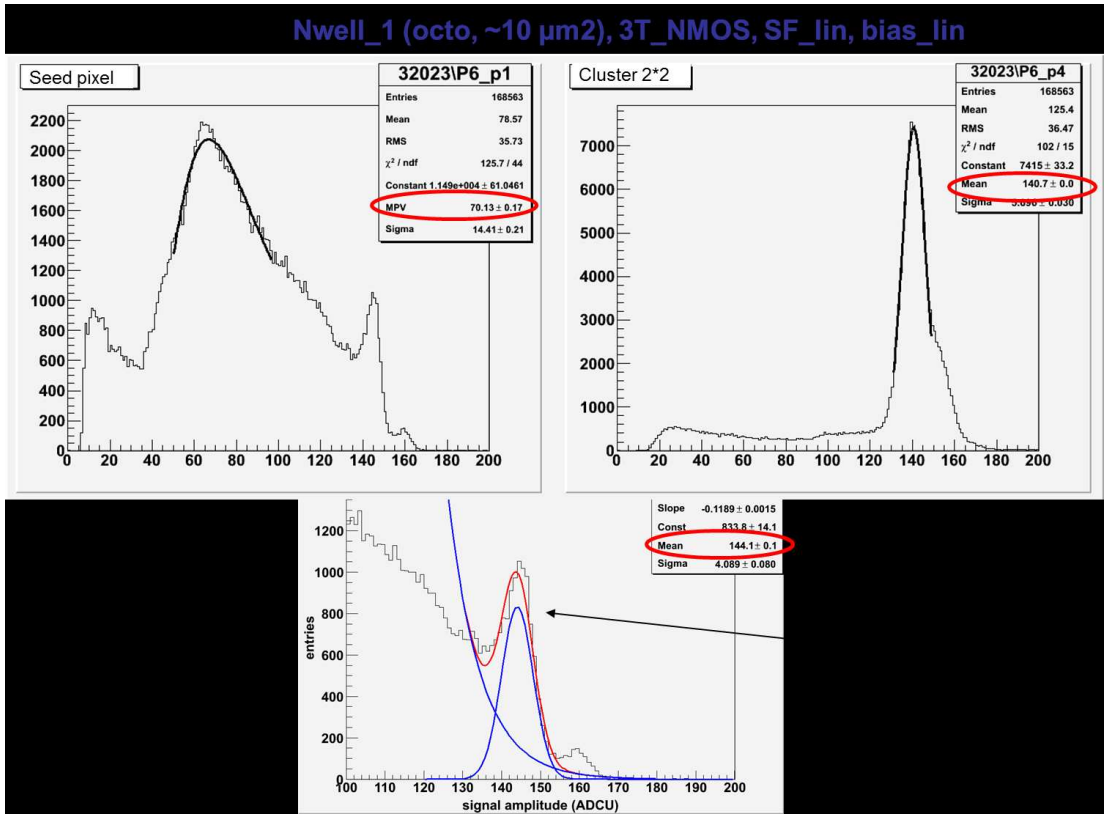




0.18 μm Technology Prototyping

- **MIMOSA-32 : technology exploration** ▷ ▷ ▷
  - ⁂ fabricated in Q4/2011 with high resistivity epitaxial layer
  - ⁂ numerous different pixels (sensing syst., pre-ampli., elongated pix.), etc.
  - ⁂ lab tests under way (^{55}Fe source)
    - ⟶ good charge collection observed (high-res epi) but noise high
  - ⁂ beam tests foreseen in June-July '12





- **Next steps**
  - ⁂ Q3:
    - MIMOSA-22THR1 ≡ MIMOSA-30 translation
    - MIMOSA-22THR1 ≡ same with 2-discri/col.
  - ⁂ Q4:
    - AROM-1 ≡ Accelerated Read-Out MIMOSA sensor
      - ⟶ prototype with in-pixel discrimination
    - SUZE-02 ≡ Zero-Suppression & output buffer circuit
      - ⟶ sparsification: 4 rows simultaneous r.o.
  - ⁂ 2013: first full scale (1 cm^2) basic block fabrication
    - ⇒ final full size proto. in 2014/15 (ALICE, CBM, AIDA)

Characteristics & Variants of MIMOSA & AROM Sensors

- **Assuming MIMOSA and AROM variants to equip innermost and outer layers**
  - ※ MIMOSA-in and AROM-1 equip innermost layer
  - ※ MIMOSA-out and AROM-2 equip outer layers

Sensor version	**MIMOSA-in**	**MIMOSA-out**	**AROM-1**	**AROM-2**
Active area dimensions $[\mathrm{mm}^2]$	8.7×31.0	19.6×31.0	10.9×31.0	20.8×31.0
Pixel dimensions $[\mu m^2]$	17×17	34×34	17×85	34×72
Single point resolution $[\mu m]$	$\lesssim 3$	$\lesssim 4$	5-7	~ 10
Read-out time $[\mu s]$	50	~ 100	1.5	7
Power consumption: instantaneous [W]	~ 1.8	~ 0.6	2.7	0.7
average [mW]	36	12	55	14

- **Power consumption (average value stands for 5 ms long power-on periods $\equiv$ 2% duty cycle):**
  - ※ layer 1: 250 W (inst.) $\Rrightarrow$ 5 W (average)
  - ※ layer 2: 120 W (inst.) $\Rrightarrow$ 2.4 W (average)
  - ※ layer 3: 200 W (inst.) $\Rrightarrow$ 4 W (average)

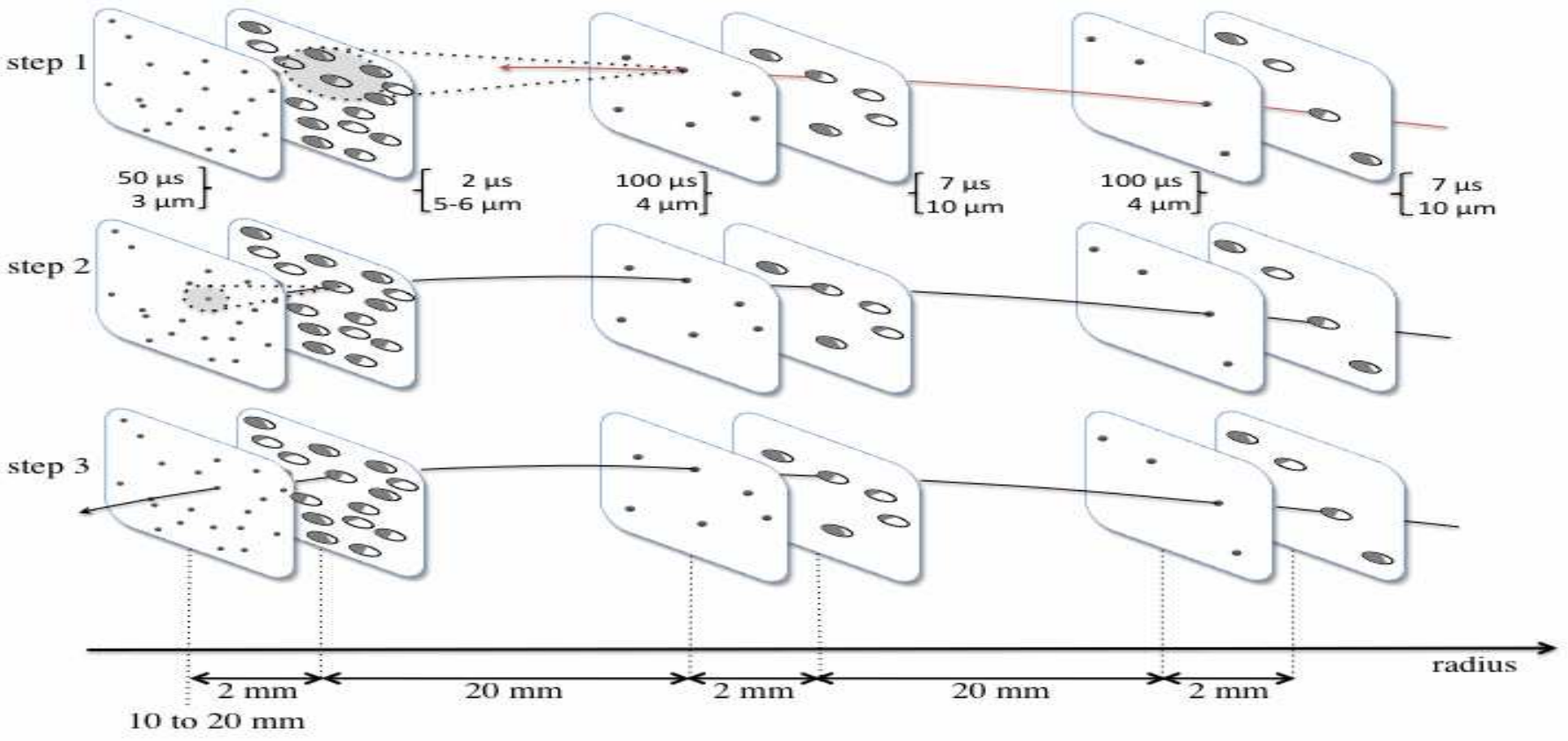
$\Rrightarrow$ **Complete detector instanteneous power $\lesssim$ 600 W $\Rrightarrow$ $<$12 W in average**

Tracking through ILD-VXD

- **Tracking from outside towards IP combining MIMOSA spatial resolution & AROM timestamp**

  ※ MIMOSA provides $<$ 3 or 4 μm spatial resolution

  ※ AROM provides 2 or 7 μs time stamping



	M-in	A-1	M-out	A-2	M-out	A-2
Pixel occupancy [%] :	0.9	0.1	0.3	0.04	0.06	0.01
with safety factor 3 [%] :	2.6	0.3	0.9	0.1	0.2	0.03

VXD - SIT Variant Composed of CPS

- **ILD-SIT : baseline assumes 2 double-sided μstrip detector layers**
  - ⁂ try understanding if CMOS sensors could improve performance with their high spatial resolution
  - ⁂ advantage : spatial resolution ▷ $4\times4\ \mu m^2$ instead of $7\times50\ \mu m^2$

    ⇛ improved soft track reconstruction (p) and TPC link

    potentially : material budget, cost
  - ⁂ disadvantage : time resolution ▷ 7 μs instead of O(100)ns – Is power a pb ?

- **Variant of VXD–SIT design made of CMOS pixel sensors (other variants give similar performances)**

Layer	σ_{sp} MIMOSA/AROM	t_{int} MIMOSA/AROM	**Occupancy [%]** w/o safey factor	**Power** inst./average
VXD-1	3 / 5-6 μm	50 / 2 μs	0.9(2.6) / 0.1(0.3)	250/5 W
VXD-2	4 / 10 μm	100 / 7 μs	0.3(0.9) / 0.04(0.1)	120/2.4 W
VXD-3	4 / 10 μm	100 / 7 μs	0.06(0.2) / 0.01(0.03)	200/4 W
SIT-1	4 / 15 μm	100 / 7 μs	$\lesssim$ 0.01	$\sim$ 1.3 kW/26 W
SIT-2	4 μm	100 μs	$\lesssim$ 0.01	$\sim$ 2.5 kW/50 W

- **ILD-SIT : power consumption** (average $\lesssim$ 100 W for $\gtrsim$ 4 m^2 coverage) **seems affordable**

  ⇛ **need benchmark event study with beam BG to evaluate track reconstruction performance**

SUMMARY

- **Mature sensor architecture complies with all VXD specifications at $\sqrt{s}$=500 GeV :**
  - architecture based on sensors realised for EUDET-BT and STAR-PXL (0.35 μm CMOS process)
  - based on 2-sided ladder concept $\Rrightarrow$ hit resolution/timestamp on opposite ladder sides (PLUME project)
  - innermost layer : $<$ 3 μm and $\lesssim$ 10 μs (upgradable to $\lesssim$ 5 μs with 2 discri/col)
  - outer layers : $<$ 4 μm (ADCs not yet tested) and $\sim$ 100 μs
  - VXD power consumption : $<$ 700 W (inst.) / $<$ 20 W (average)
  - final prototypes fabricated $\Rrightarrow$ tests under way : MIMOSA-30(in) & MIMOSA-31(out)
  - validation of concept $\pm$ completed in 2012 with 2-sided ladder (PLUME) offering 0.35 % X_0 (X-section)

- **Translation 0.35 $\mu m \rightarrowtail$ 0.18 μm CMOS under way for $\sqrt{s} \gtrsim$ 1 TeV :**
  - benefits: read-out $<$ 2/10μs (inner/outer layers), $>$ 20% less power, sensor throughput, pixelated SIT, ...
  - exploratory chip (MIMOSA-32) under test
  - mid-scale prototypes validating architecture planned for submission in Q3/ & Q4/2012
  - Full Scale Basic Block (FSBB - 1cm^2 active area) expected to be fabricated in 2013

    $\Rrightarrow$ Final (full scale) prototype in 2014/15
  - synergy with AIDA-SALAT, ALICE-ITS & -MFT, CMB-MVD, ...