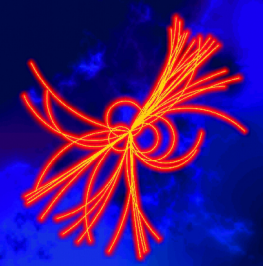


Summary of the Tracking and Vertexing Sessions

J. Kaminski
U. Bonn

Vertexing & Tracking

Main requirement for the vertex detectors is an impact resolution of:

$$\sigma_{d_0}^2 = a^2 + \frac{b^2}{p^2 \sin^3 \theta}$$

with a ≤ 5 μm and b ≤ 10-15 μm GeV

For the tracking detector the momentum resolution $dp_t/p_t \leq 2\times10^{-5}$ /GeV/c (e.g. ILD) and tracking efficiency is most important (>99%, ILD).

And of course the 'standard' requirements:

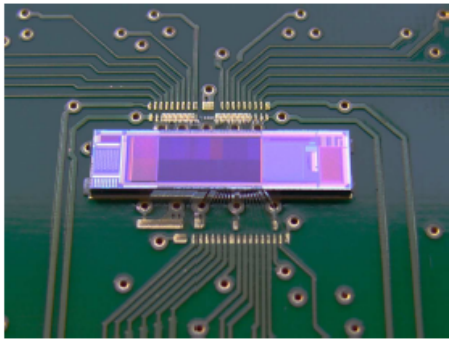
- Low material budget: 0.1-0.15% X_0 per layer
- Low power consumption (to make air cooling possible)

=> New results were presented in 4 session with 18 presentations followed by intense discussions.

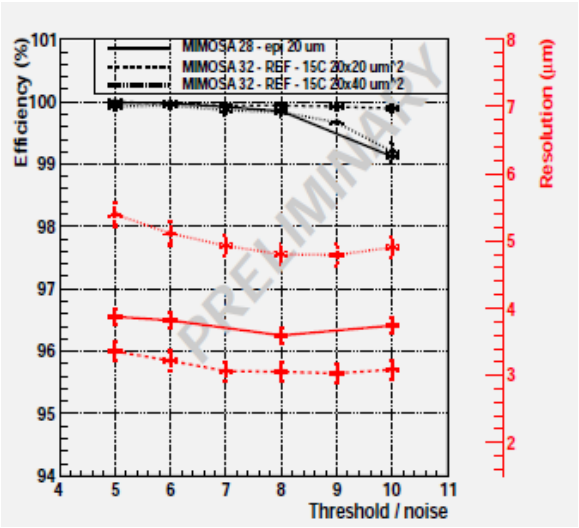
CMOS

Previous detectors were made in 350 nm technology, but there are limitations:

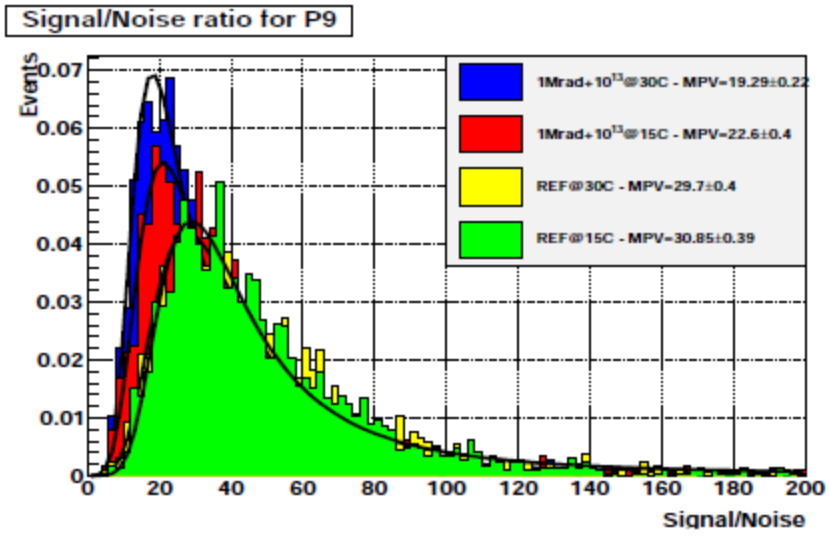
CMOS process fab. parametres	In-pixel circuitry	Read-out speed	Power consum.	Insensitive areas	TID (> ILC)	Data throughput
Feature size	X	X	X	X	X	
Planar techno.	X	X	X		x	
Nb (metal layers)	X	X		X		
Clock frequency				X		X



Switching to 180 nm process: 6 metal layers, deep p-wells, smaller feature sizes
First prototype produced MIMOSA-32

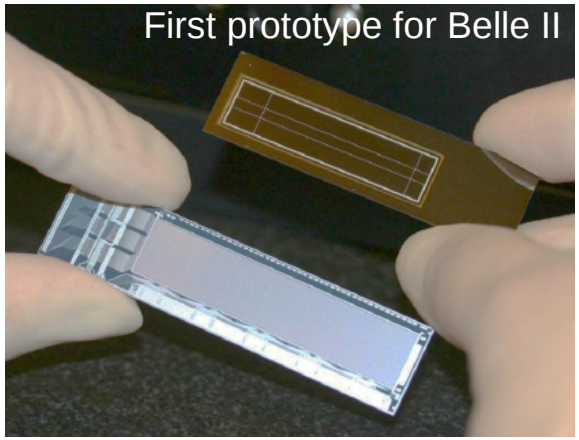


- Already test beam results and device has been irradiated up to 1 MRad + 10^{13} n_{eq}/cm^2
- No loss in efficiency
- Spin off for ALICE-ITS (10m²).



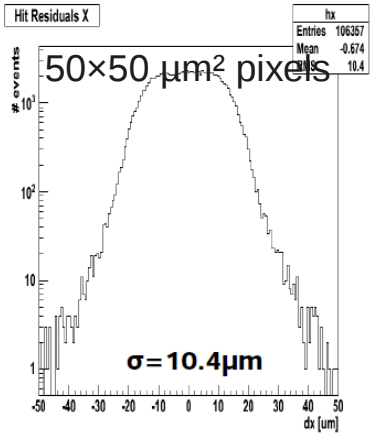
DEPFET

Spin off for Belle II is produced (requirements are similar to ILC).



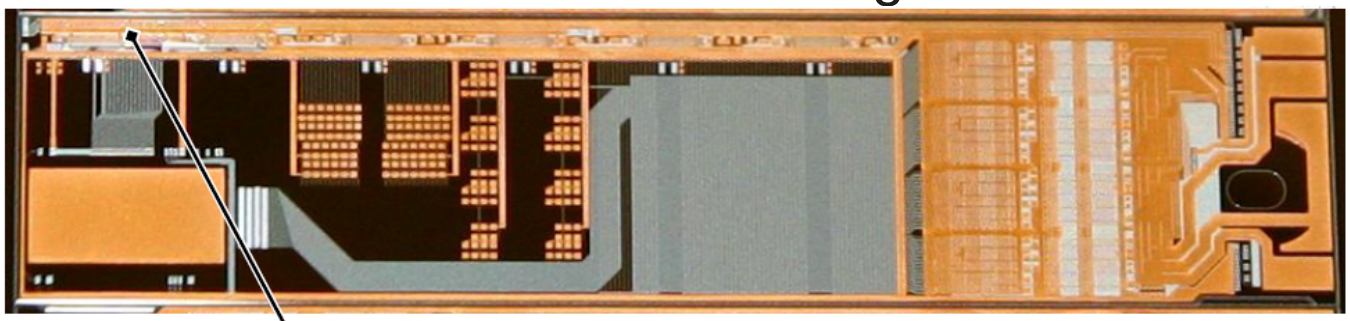
	ILD LOI 5-layer layout	Belle II	
Radii	15, 26, 38, 49, 60	14, 22	mm
Sensitive length	123 (L1), 250 (L2-L5)	90 (L1), 122 (L2)	mm
Sensitive width	13 (L1), 22 (L2-L5)	12.5 (L1-L2)	mm
Number of ladders	8, 8, 12, 16, 20	8, 12	
Pixel size	25x25 (L1-L5)	55x50 & 60X50 (L1), 70x50 & 85x50 (L2)	μm^2
frame rate	20 (L1), 4 (L2-L5)	50	kHz
Number of pixels	800	8	Mpix

First tests with thinned modules (50 µm) have been performed
- 100 ns/row => total readout time 100 µs / chip
- Further improvement by adding third metal layer or optimizing layout



First test beam measurements with larger pixels (50×50µm²)
- Showed good results.

First realizations of a ladder are being discussed and tested.

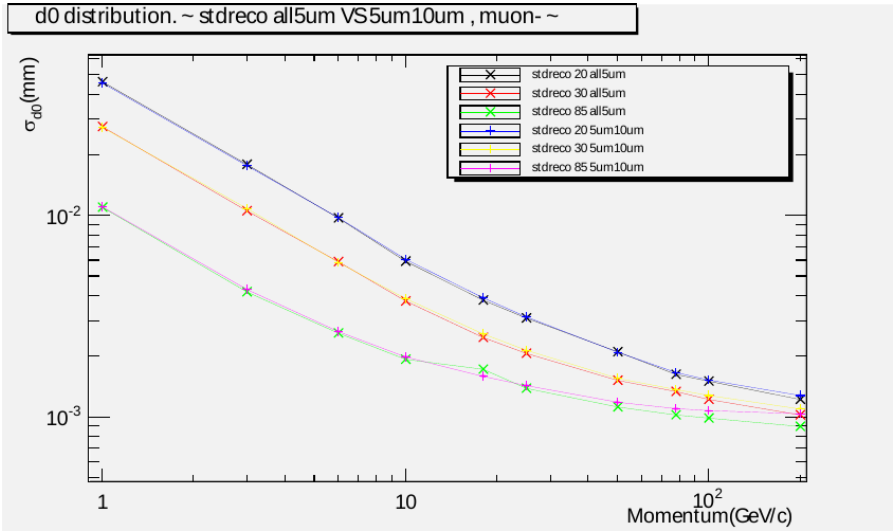


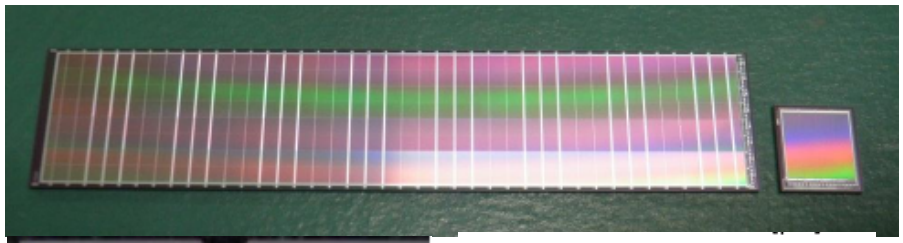
FPCCD

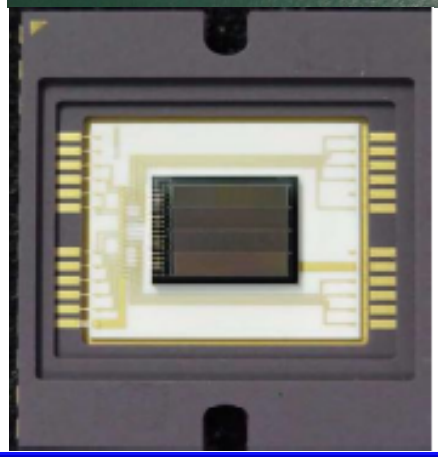
New study of increased pixel size
(5 μm → 10 μm) in outer 4 layers
Reduces number of pixels from 7k to 2k
→ 1/3 of the power consumption
34 W only!
Impact resolution not influenced,
occupancy roughly doubles to 0.5 %

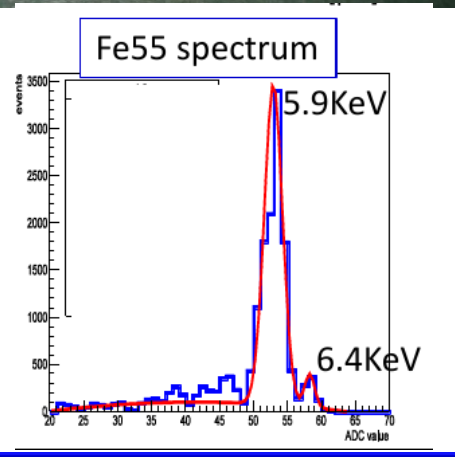
For experimental tests 2 sensors with various pixel sizes of 6×6 μm² to 6×24 μm² was produced.

2nd readout ASICS has been tested:
Energy resolution of 120 eV (^{55}Fe)
S/N ≈ 37 (^{90}Sr), CTE ≥ 98%
3rd readout ASIC will be tested with new sensors soon.
Smallest pixels (6×6 μm²) do not work.



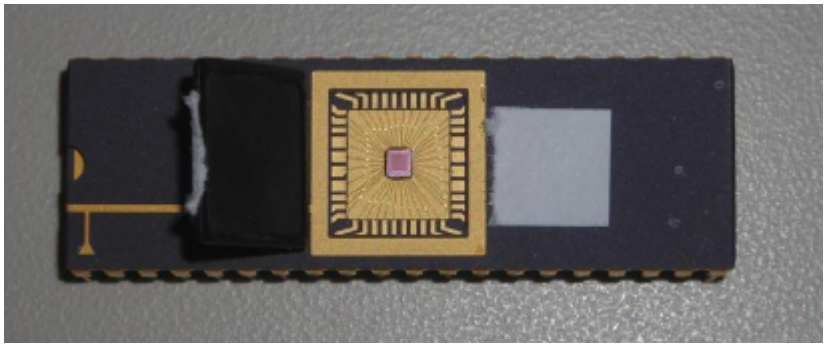


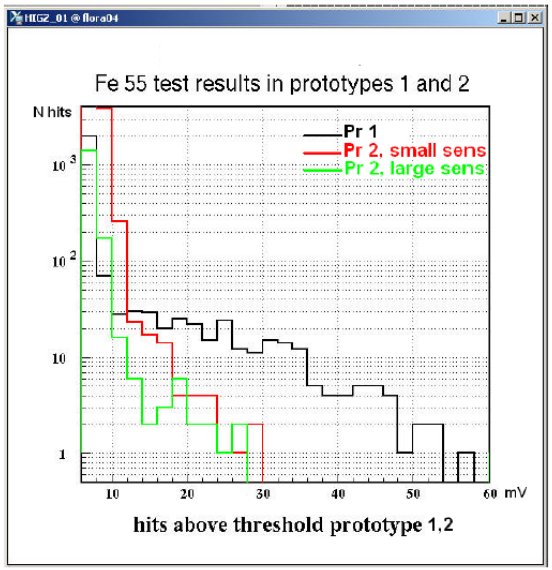




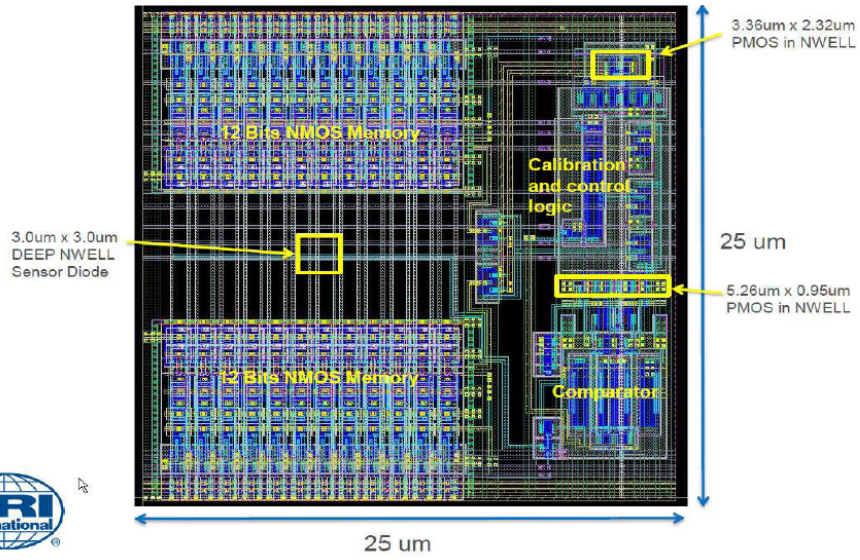
Chronopixel

- To reduce the background time stamps with a length of 10 µs are added to the hit information. - Not the complete bunch train is integrated over.
=> Use monolithic CMOS detector and record time information.
- In 9/2011 work resumed, in 2/2012 chip was submitted and delivered in 6/2012
- This was done in 90 nm- technology. But comparators are difficult to implement
=> use PMOS for comparator
- Charge collection efficiency is only 67 %





Some parameters not as expected.
Discussions with foundries are necessary to find a way to improve the layout.

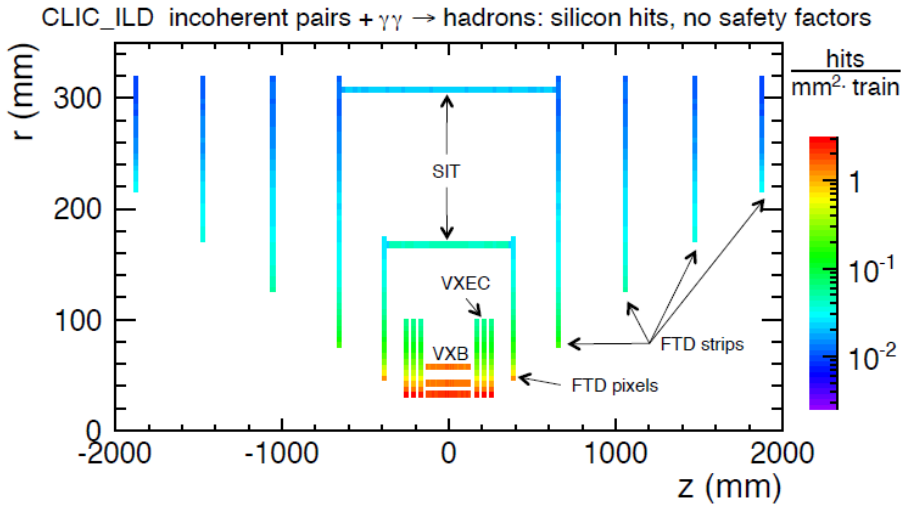


CLIC

Simulations of CLIC backgrounds showed that the requirements are much more demanding: higher occupancy and radiation doses

→ need faster readout (10 ns time slices) and small pixels (25×25 μm²).

→ Hybrid approach: Benefits of two different technologies can be used.

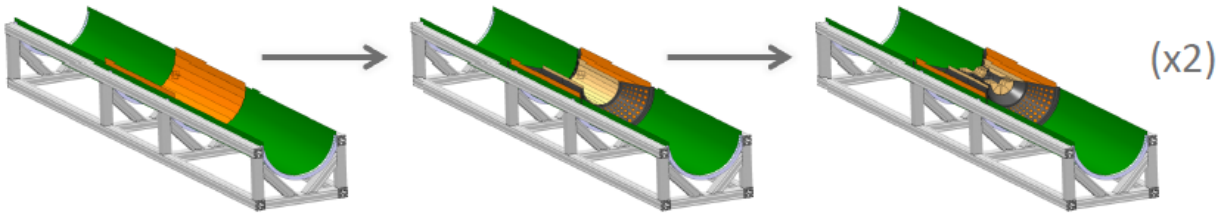


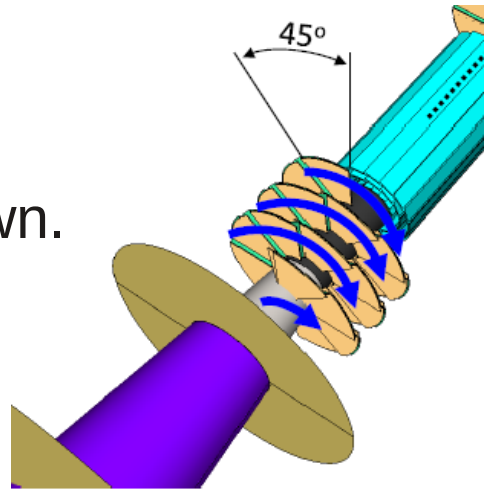
Development of new readout chip SmallPix almost done.

Shares many features with Timepix3, but smaller pixel sizes (40×40 μm²) because of reduced complexity.

First tests for a final CLICPix (25×25 μm²) are being made.

Some interesting idea concerning the integration were shown.

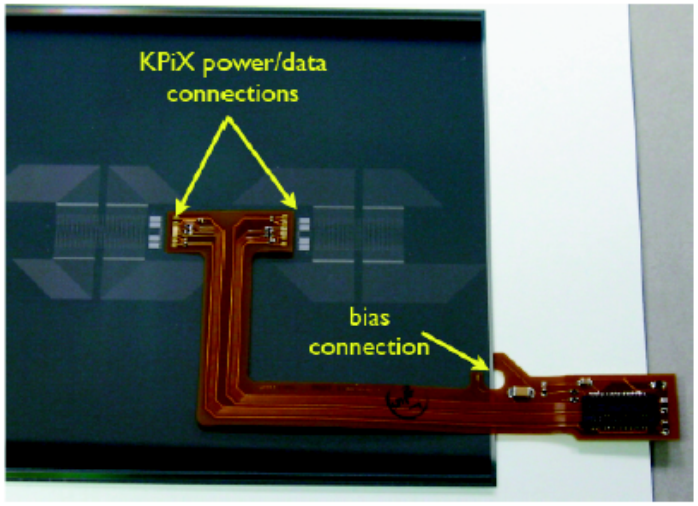


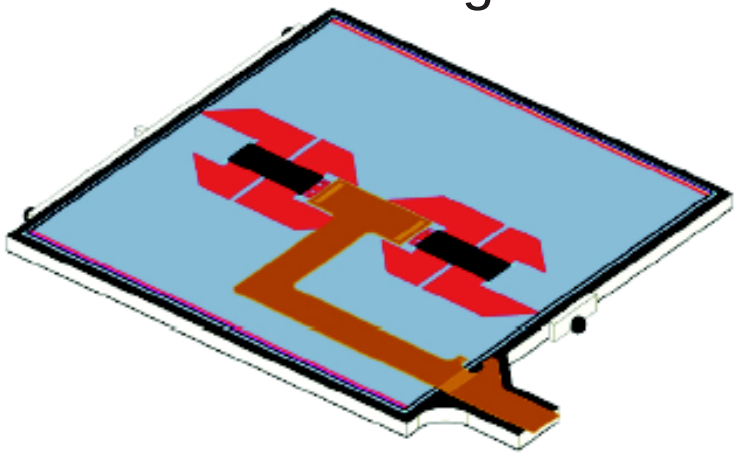


Silicon-Tracking

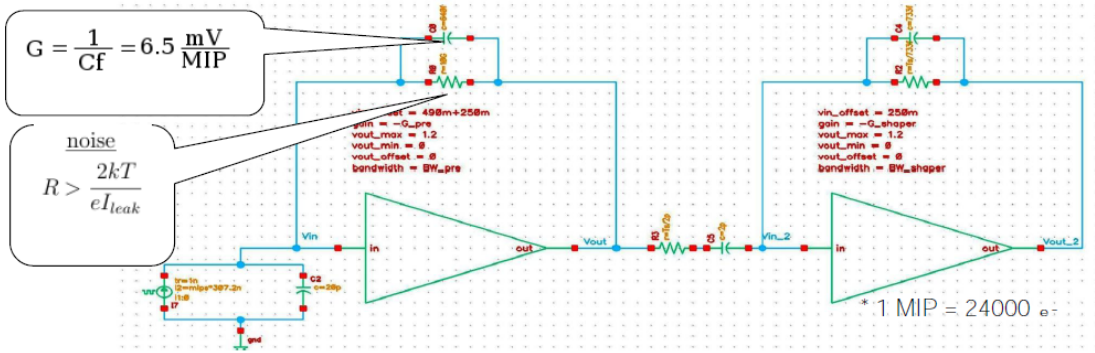
For SiD tracker modules all items are in house:
- 1024 channel Kpix
- sensors with double metal layer routing
- Kapton cable

Issues with the bonding have to be overcome.



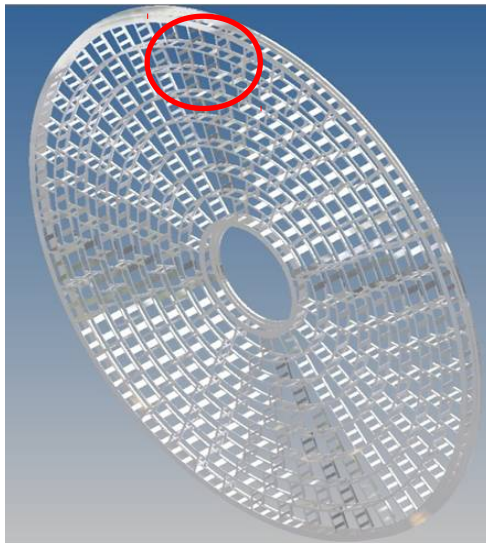


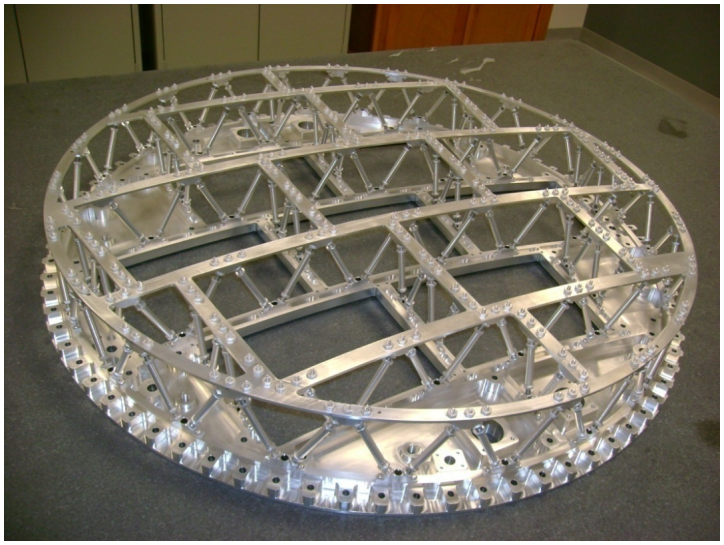
For the forward tracker a new chip is being planned - TSMC 65
Verilog simulation of the 256 channel chip using 65 nm CMOS technology



TPC

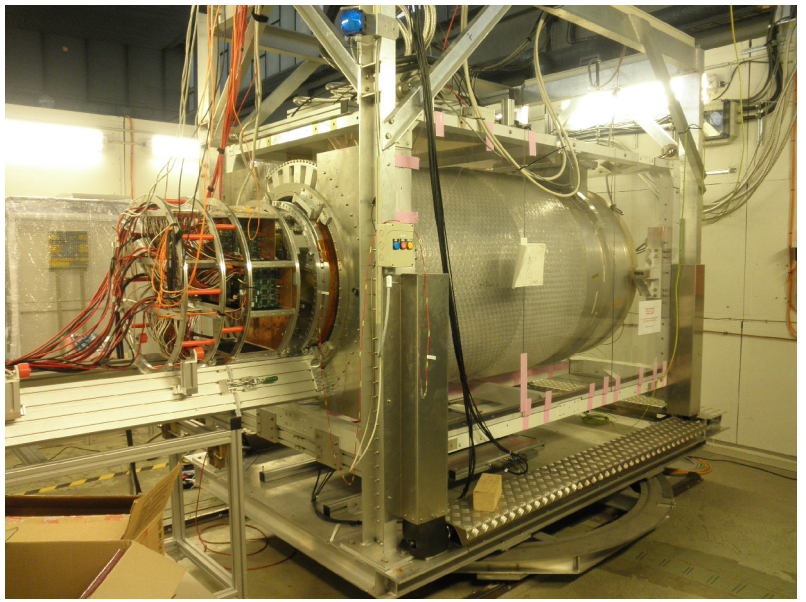
- LCTPC-collaboration has looked more into how to build a large detector.
- Detailed FEM-studies of endplate have been performed.
- The model has been tested by producing a new endplate for the large prototype at DESY.





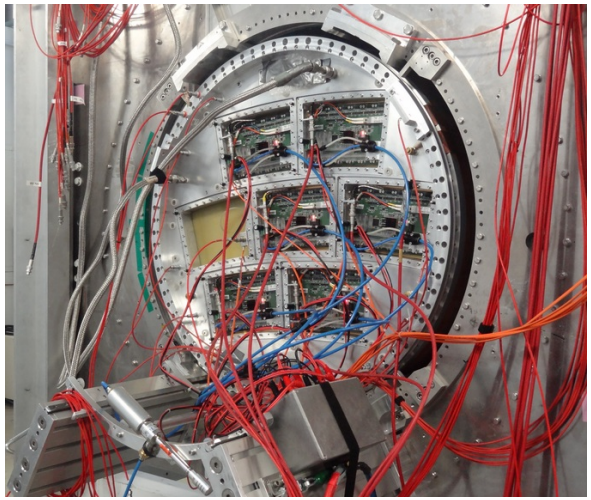
Also, integration issues like the influence of support and the mounting of modules are being studied.

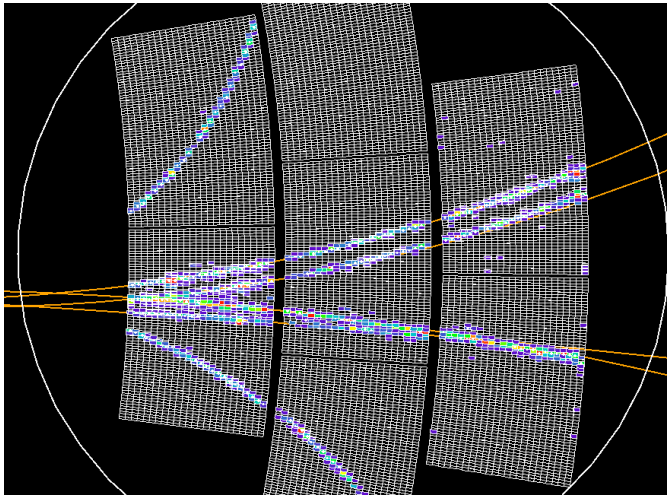
EUDET/AIDA test facility at DESY was upgraded

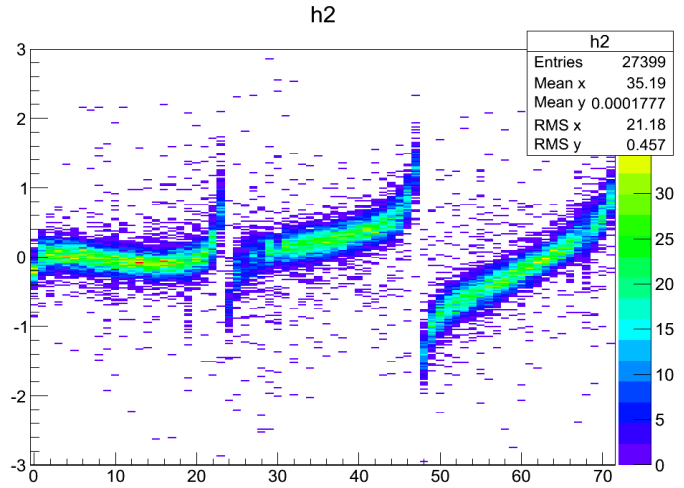


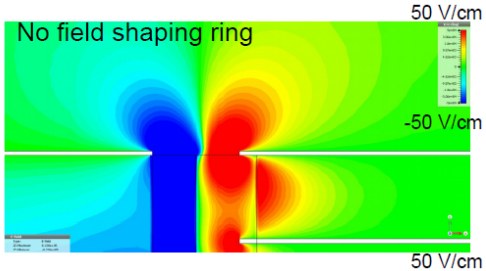
Modules

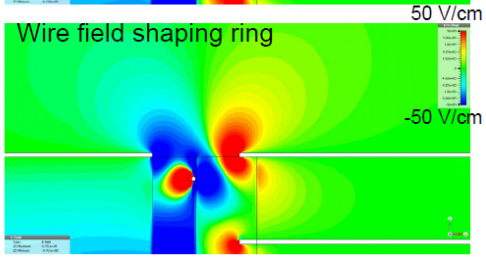
Multi-module setups with highly integrated electronics are tested in the LP:
For example the 6-module setup with MM+resistive layer modules in 7/2012.



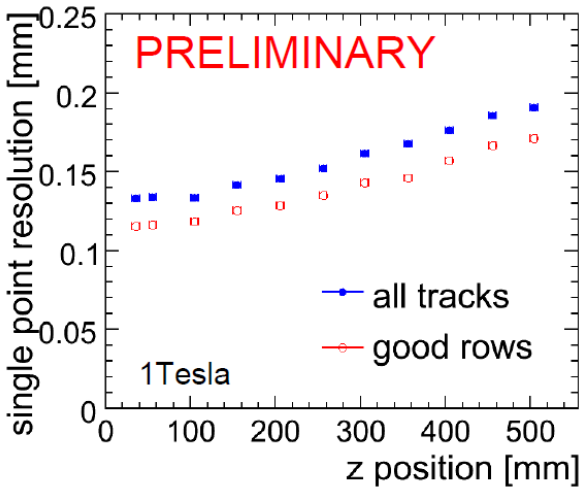








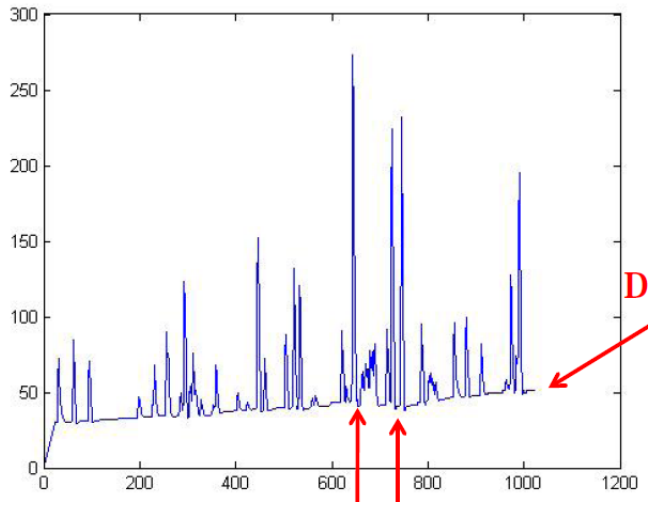
Field distortions at the border of the modules are seen with all gas amplification technologies (GEMs, MM, InGrids) and solutions are being investigated.

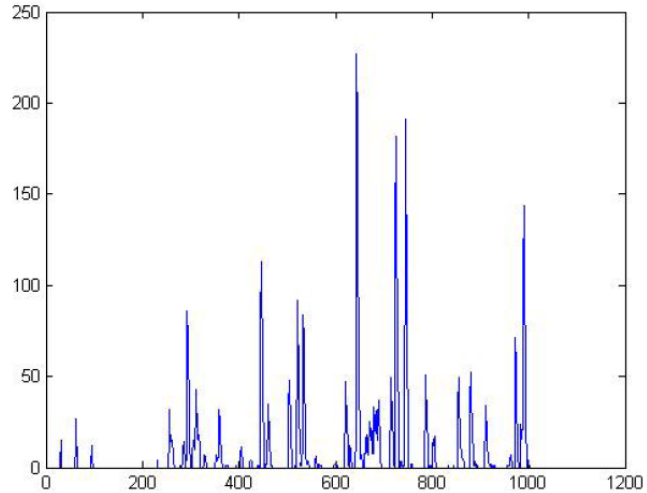


Electronics

For reading out the TPC two different concepts are being pursued:

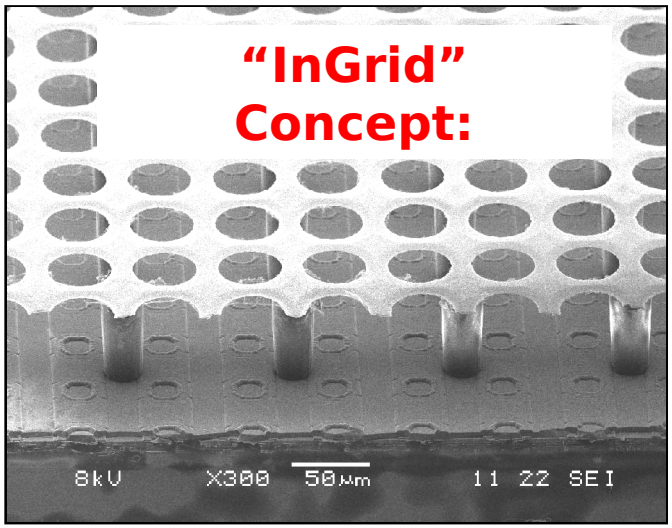
1.) Conventional FADC-based electronics + pads:
First step SALTRO
– delivered this year:
Good performance
(noise ~ 300 e-, PP: 12.5mW/channel at ILC)
BUT: Further improvements are necessary.
New chip GdSP is planned in collaboration with CMS
Further reduction of power consumption + higher integration (64-128 channels)



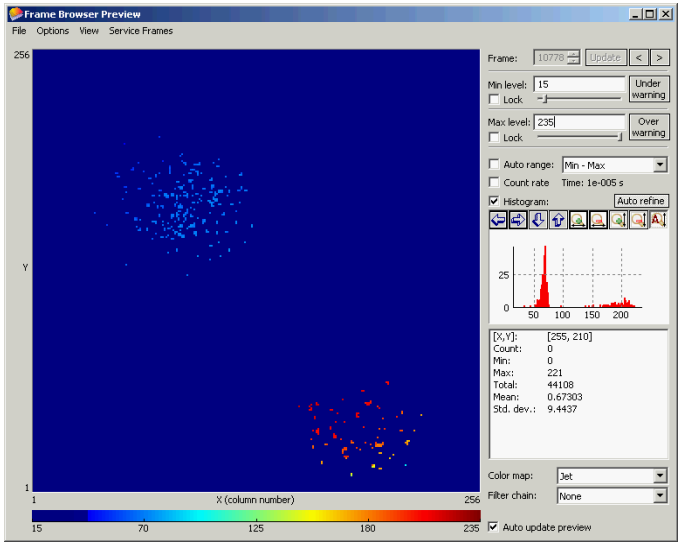


2.) Highly pixelized readout: Use a pixel readout ASIC for charge collection and digitization.
Chip of choice is Timepix, but has many limitations
Successor (Timepix3) will be produced next year.

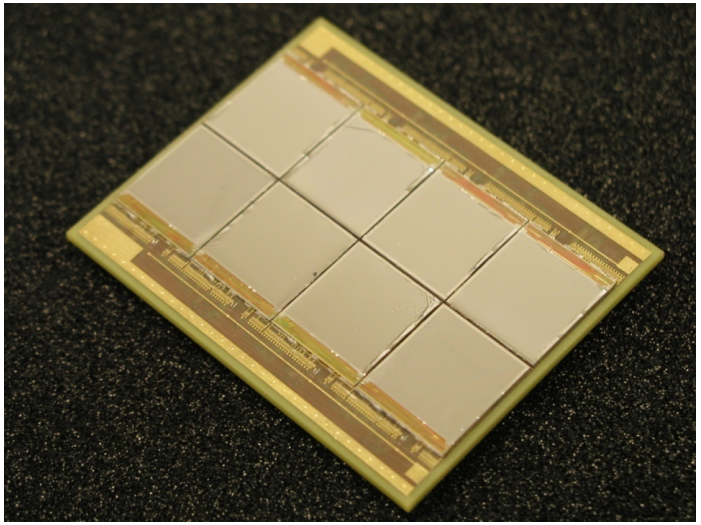
Highly Pixelized Readout



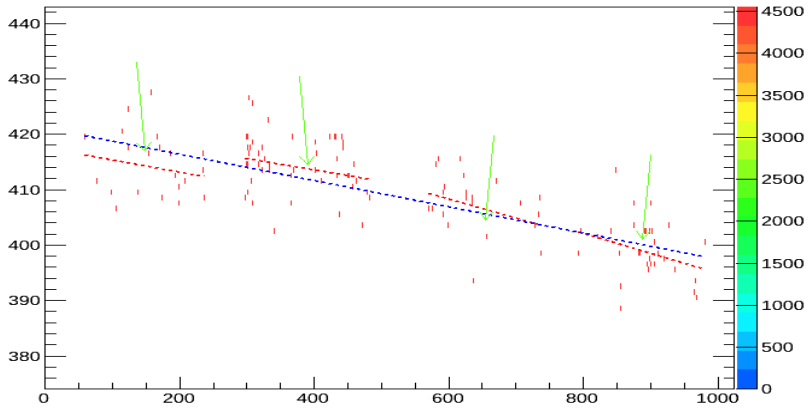
Micromegas-mesh is built on the readout chip with post-processing steps. Ideal alignment of grid holes to pads.



New production techniques allows the production of ~100 InGrids simultaneously.

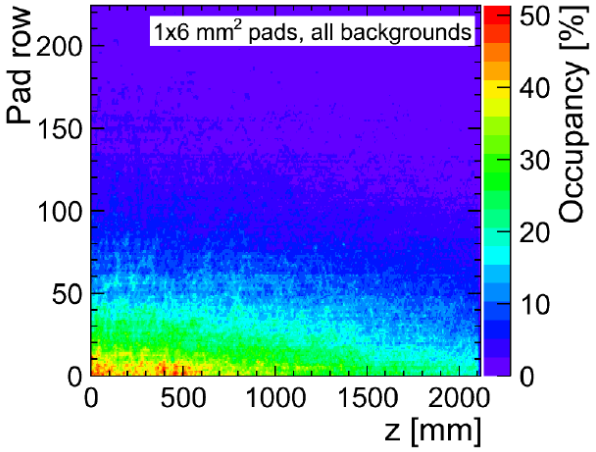


Analysis of the first 8 chip modules has started, but data Sample is limited. New test beam campaign is planned for next year.



Simulations for CLIC

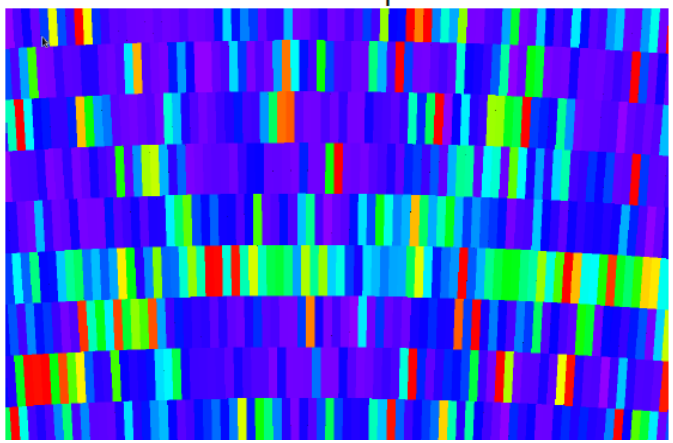
For the CLIC-CDR many studies have been performed investigation the performance of a TPC in the CLIC environment.
Problematic are the high backgrounds of yy-> hadrons and incoherent pairs.

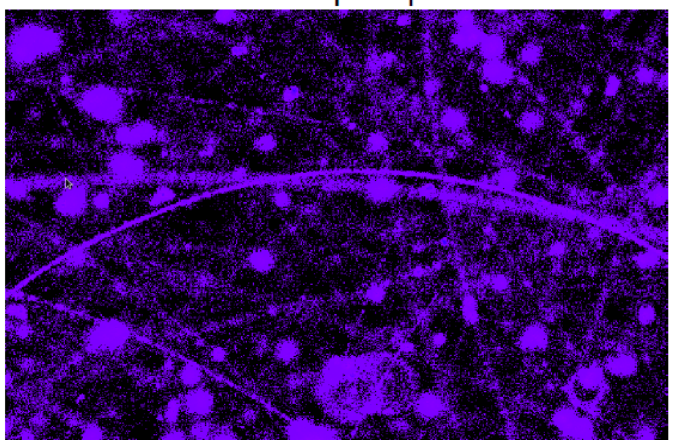


With ILD-like TPC (i.e. 1*4 mm² pads) very high occupancies are expected.

If highly pixelized readouts are used, this occupancy Is reduced down to < 3%

=> for CLIC TPC the InGrids seem to be necessary





However, with current reconstruction code it is only possible to reconstruct muons without background.

Summary

In the last year quite some progress was made:
Many new iterations of the electronics was delivered and tested.

For ILD several pixel technologies and readout approaches are on a good track, while more R&D is necessary for a CLIC-type detector.
Further developments will be guided by applications/spin offs in upcoming detectors (ALICE, STAR, ALICE, Belle, CBM).

Prove of feasibility has been demonstrated for several technologies for the tracking.

Main focus also includes now many integration issues:
- Building ladder with pixel sensors
- Operating multi-module set-ups at the Large Prototype TPC
- Cooling and mechanical aspects