

FPCCD option of ILD vertex detector

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@LCWS2012

Outline

- FPCCD VTX design parameter
- FPCCD sensors
- Support structure

FPCCD VTX design parameter

Layer	R (mm)	Z (mm)	cos θ	Pixel size (μm)
1	16	62.5	0.97	5
2	18	62.5	0.96	5
3	37	125	0.96	10
4	39	125	0.95	10
5	58	125	0.91	10
6	60	125	0.9	10

- Pixel size of outer layers
 - It was $5\mu\text{m}$, but changed to $10\mu\text{m}$
 - ➔ Reduction of number of readout channels and power consumption

Power consumption

- Assumptions

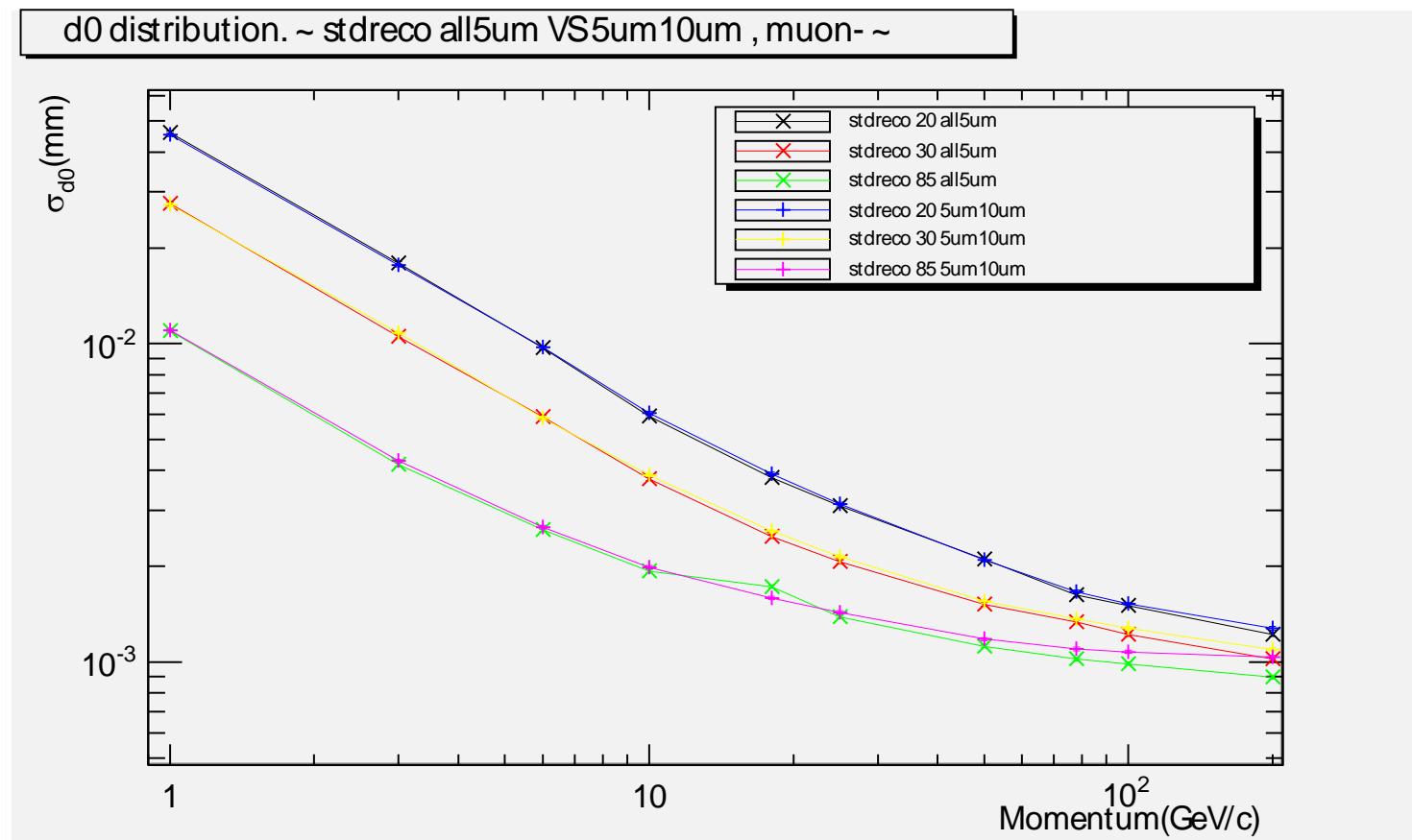
Readout frequency	10 Mpix/s
Readout time	200 ms
Clock timing	Same for inner and outer layers
Vertical shift time	40 us/line
Power consumption	15 mW/ch
Chip size (in/out)	11x62.5mm ² / 22x125mm ²
Number of chips (in/out)	40 (=10x2x2) / 112 (=(11+17)x2x2)

- Results

Pixel size (in)	Pixel size (out)	# of ch/chip (in)	# of ch/chip (out)	# of ch (total)	Power consumption
5 um	5 um	28	56	7392	111 W
5 um	10 um	15	15	2280	34 W

Expected IP resolution

- Increase of pixel size of outer layers does not affect the IP resolution



Pixel occupancy

- Simulation results for pixel occupancy at 1TeV (statistics:10BX)
- Increase of occupancy due to decrease of # of pixels (1/4) is less than x4

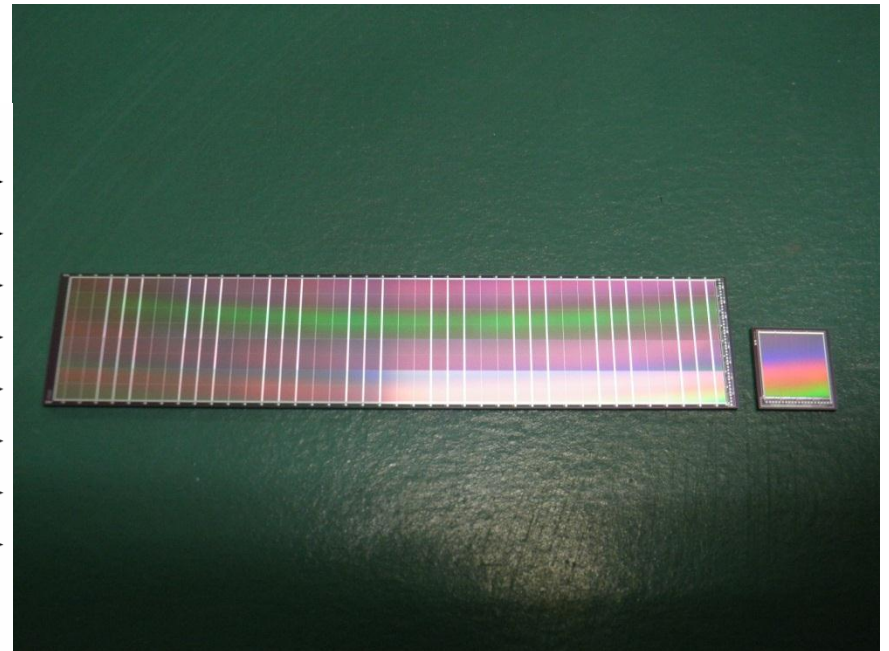
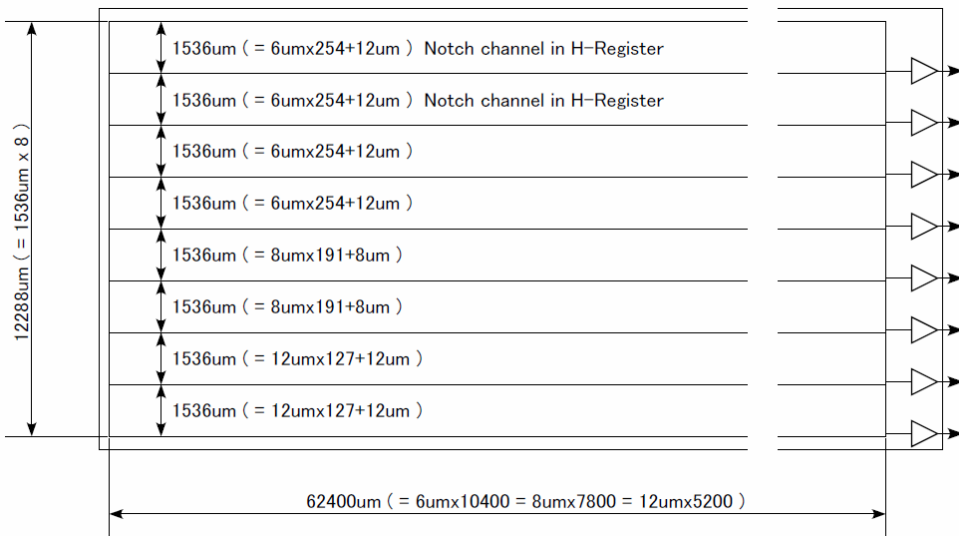
Layer	Occupancy for 5um (%)			Occupancy for 10um (%)		
	Direct	B.S.	Total	Direct	B.S.	Total
1	5.1	14.5	19.6			
2	3.1	7.3	10.4			
3	0.18	0.06	0.24	0.41	0.14	0.55
4	0.15	0.06	0.20	0.33	0.13	0.46
5	0.033	0.014	0.047	0.075	0.032	0.107
6	0.029	0.017	0.046	0.064	0.039	0.104

FPCCD sensors

- Small prototype in FY2012
 - 6mm square image area
 - 6um pixel size
 - 4ch/chip with different horizontal shift register size: 6x6, 6x12, 6x18, 6x24 μm^2
 - It works except for the channel with 6x6 μm^2 horizontal shift register

FPCCD sensors

- Large prototype
 - $62.4 \times 12.3 \text{mm}^2$ image area ~ Real size prototype for inner layers
 - 8ch/chip with several pixel sizes: 4chx6 μm , 2chx8 μm , 2chx12 μm
 - Si wafer has been made, but waiting for packaging

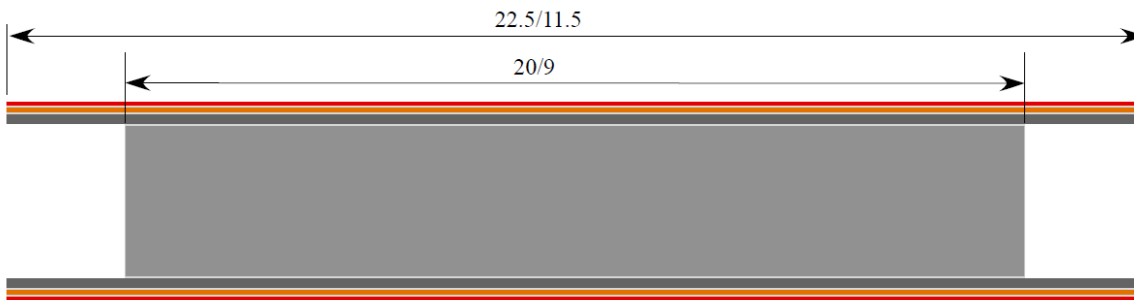


Support structure

- Ladder design

- Ladder has a tricky shape to allow overlapping of sensors with adjacent ladder

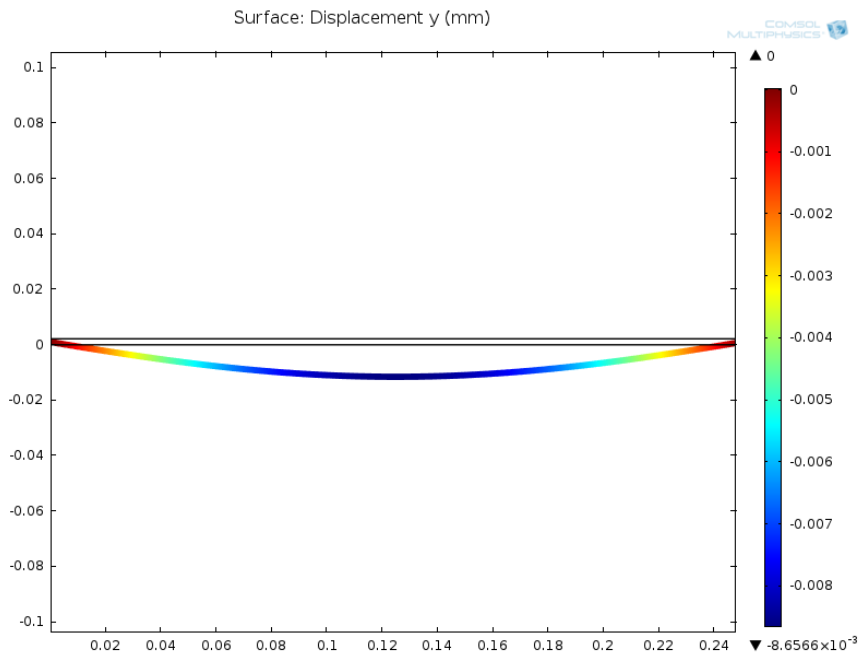
- Material budget
 $\sim 0.3\% X_0 / \text{ladder} =$
 $0.15\% X_0 / \text{sensor layer}$



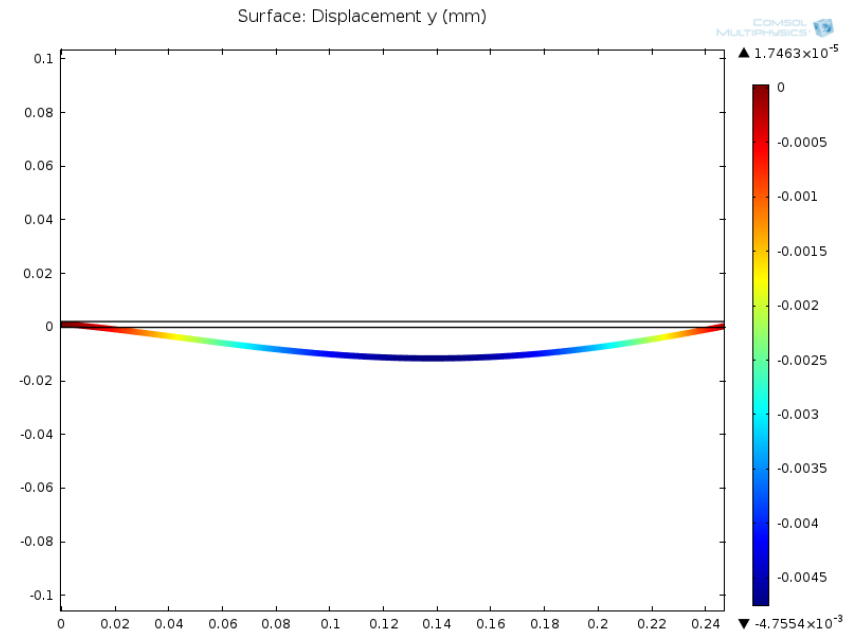
		t (μm)	Total t (μm)	X0 (%)
Si		50	50	0.0534
Epoxi		10	2000	0.0028
FPC	Cu	9		0.0125
	Kapton	51		0.0179
Epoxi		10		0.0028
CFRP		100		0.0383
Epoxi		20		0.0056
RVC		1600		0.0300
Epoxi		20		0.0056
CFRP		100		0.0383
Epoxi		10		0.0028
FPC	Cu	9		0.0125
	Kapton	51		0.0179
Epoxi		10		0.0028
Si		50		50
Total			2100	0.2966

Support structure

- Ladder deformation by self weight
 - Simplified geometry of 50um Si sensors (200um gap between two sensors) + CFRP sheets and RVC core



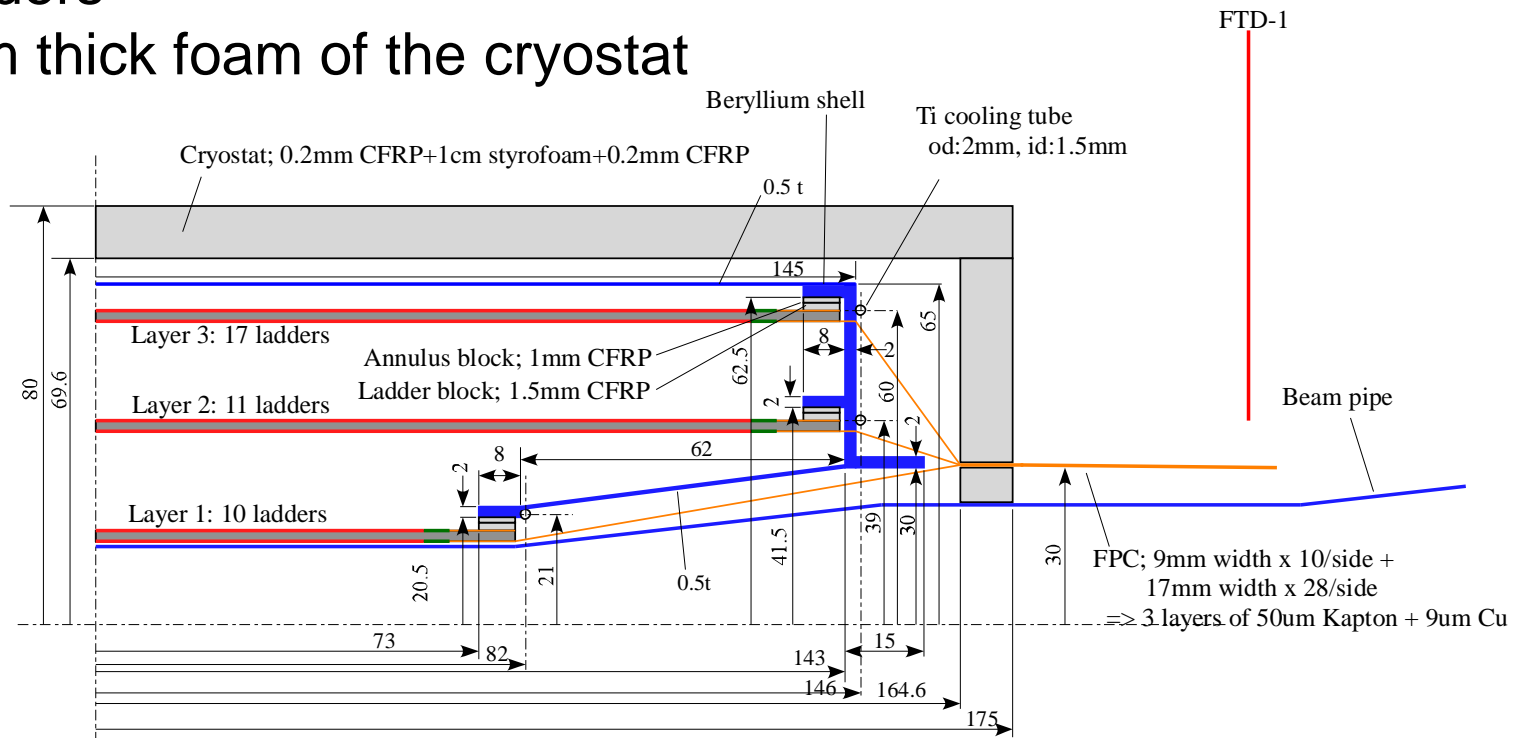
Two edges support:
Maximum deformation ~ 8.66 μm



One edge fix, one edge support:
Maximum deformation ~ 4.76 μm

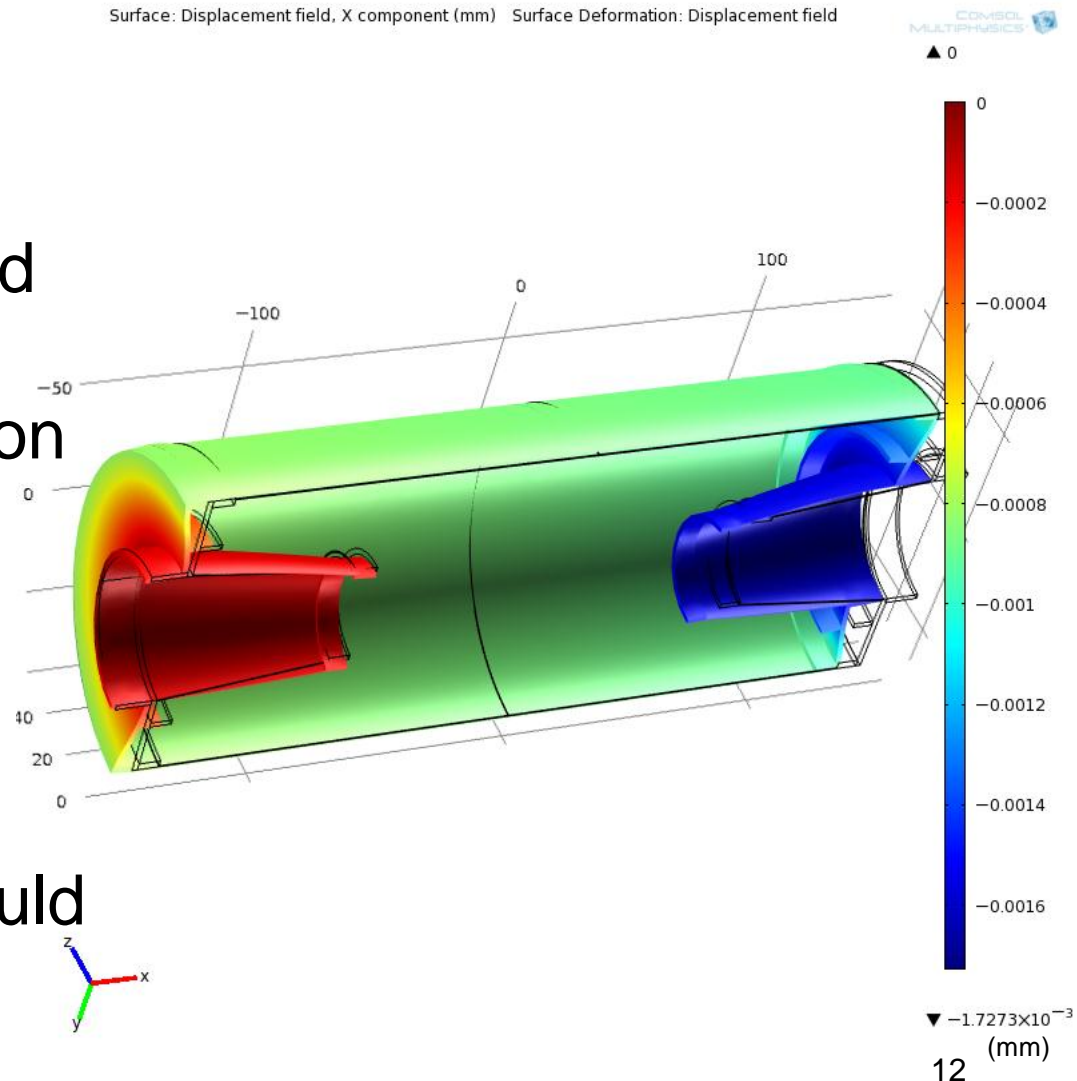
Support structure

- Design in ILD simulation model
 - Similar to SLD vertex detector
 - 2 mm thick Be end plate, 0.5 mm thick Be support shell
 - Kapton+Cu flexible cables
 - Ladders
 - 1 cm thick foam of the cryostat



Beryllium support shell

- FEA calculation of deformation
 - 1kgf (9.8N) is applied in z-direction
 - Maximum deformation is less than $2\mu\text{m}$
 - Total weight is less than 500g \rightarrow max force caused by the friction at the kinematic mount would be less than 500gf



Summary

- FPCCD vertex detector design for DBD
 - 3 sets of double-layer ladders: total 6 layers
 - $R_{in}=16\text{mm}$, $R_{out}=60\text{mm}$
 - Pixels size is $5\mu\text{m}$ for inner two layers and $10\mu\text{m}$ for outer 4 layers: Impact parameter resolution is almost same as the all $5\mu\text{m}$ pixel case
 - Material budget $\sim 0.3\%X_0/\text{ladder} = 0.15\%X_0/\text{layer}$
 - Ladders are supported by a Beryllium support structure: 2mm-thick end-plate and 0.5mm-thick cylindrical support shell
 - The support structure is enclosed in a rigid foam cryostat and operated at -40°C
- Sensor R&D status
 - A small size prototype with $6\mu\text{m}$ pixel size has been made and it works
 - Almost real size large prototype with $6 - 12\mu\text{m}$ pixel size has been made: to be tested soon
 - Detailed characterization is expected in coming 1~2 years