FPCCD option

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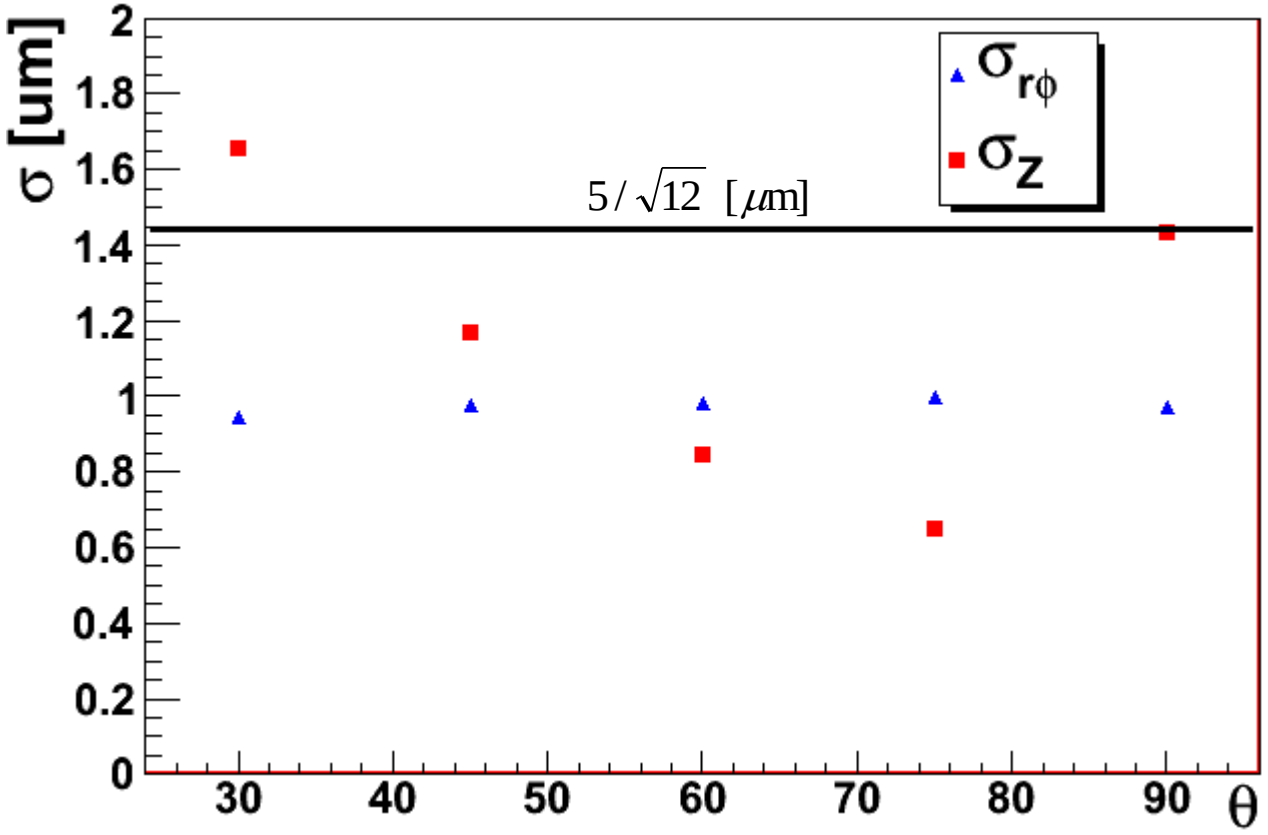
ILD Workshop @Fukuoka

Features of FPCCD option

- Fine pixels of ~5μm
  - Excellent spatial resolution (1.4μm with digital readout, ~1μm with analog readout)
  - Larger pixel size is acceptable for outer layers
- Fully depleted epitaxial layer of ~15μm thick
  - Suppress the charge spread and the number of hit pixels
  - Excellent two-track separation
  - Pair-background rejection by cluster shape
- Reasonably low pixel occupancy even with accumulation of hit signals in one train
- Read out between trains
  - Completely free from beam-induced RF noise
  - No need for power pulsing
- Large chip (22x125 mm^2) can be fabricated

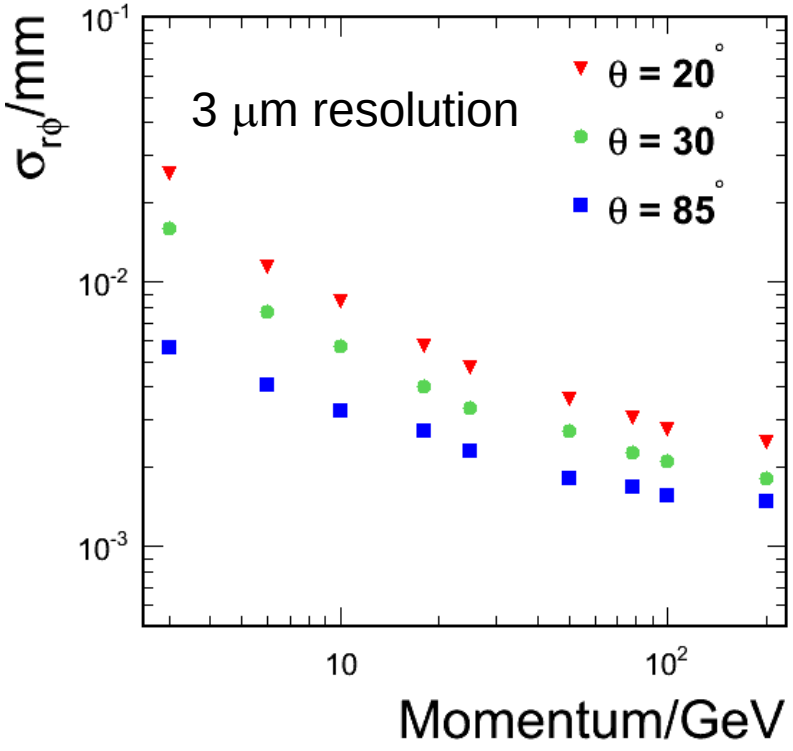
Spatial resolution

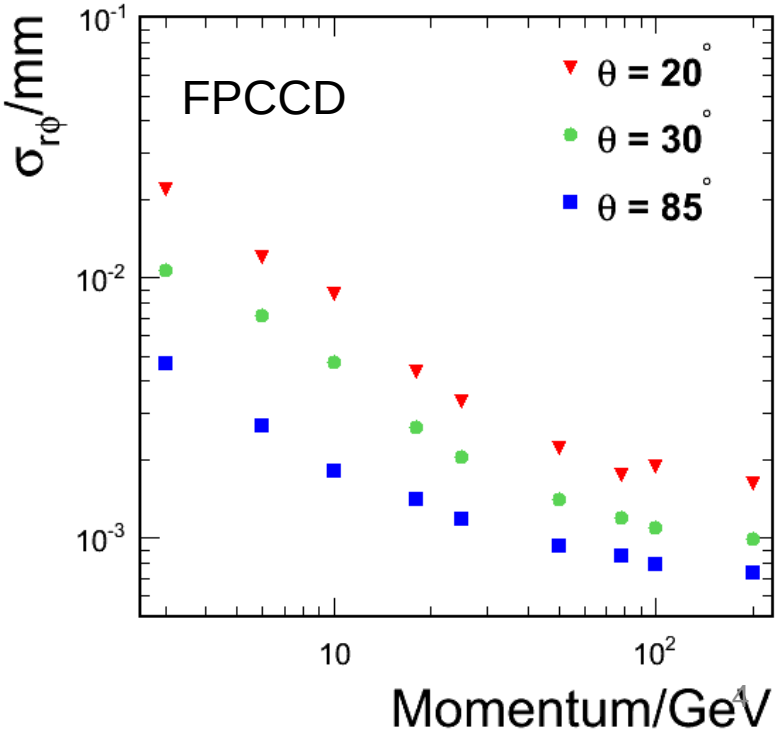
- Simulation study for analog readout



Impact parameter resolution

- Impact parameter resolution in R-ϕ
  - Significant improvement in high momentum region





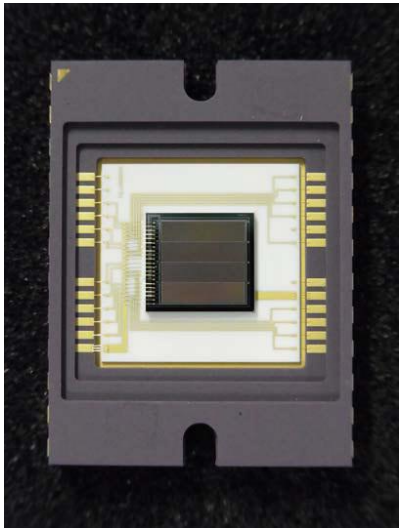
Pixel occupancy

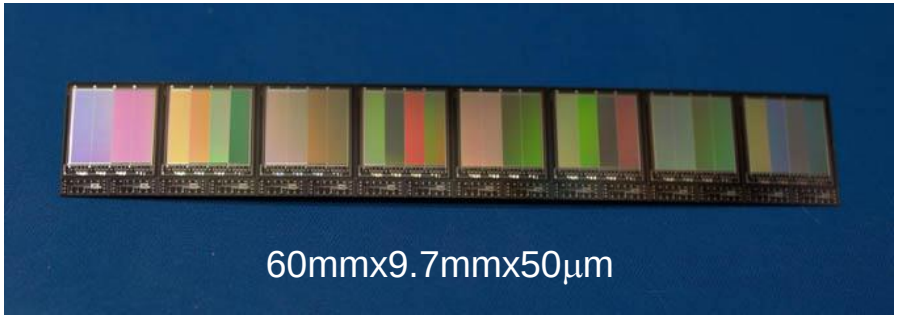
- 500 GeV simulation
  - Detector model: ILD_01pre02
  - Data statistics: 1600 BX
  - 1312 BX/train
- 1 TeV simulation
  - Detector model: ILD_O1_v02
  - Data statistics: 20 BX
  - 2450 BX/train
- Both cases
  - Signal threshold cut of >200 electrons/pixel

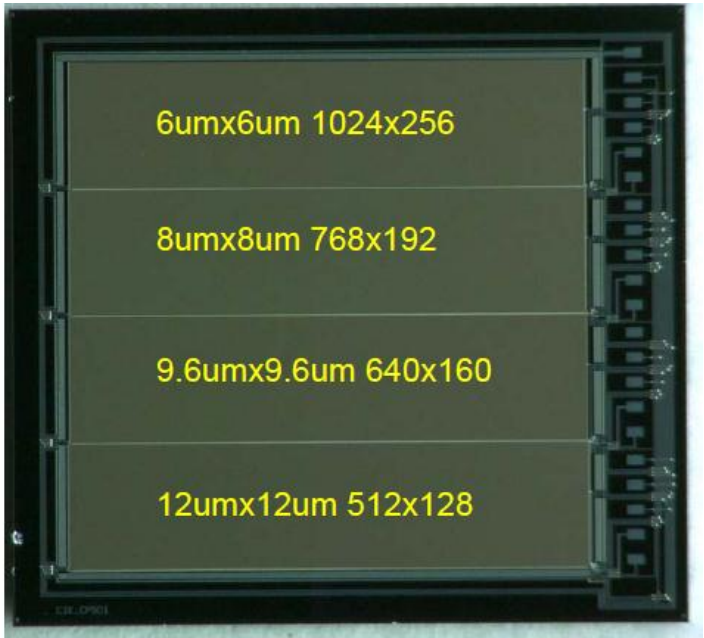
Layer	500 GeV (sb2009wTF) [%]	1 TeV [%]
1	3.1	15.5
2	1.7	7.8
3	0.09	0.67
4	0.07	0.36
5	0.017	0.12
6	0.015	0.094

Sensor R&D status

- Small prototypes 4 times
  - 6x6mm^2 image area
  - 4ch/chip
  - Gain: 5μV/electron
  - FY2008: 12 μm pixel
  - FY2009: 12 μm pixel
  - FY2010: 12, 9.6, 8, 6 μm pixels
  - FY2011: 12, 9.6, 8, 6 μm pixels, 50μm thick
- Wafer thinning
  - Thinning down to 50 μm is an established technology

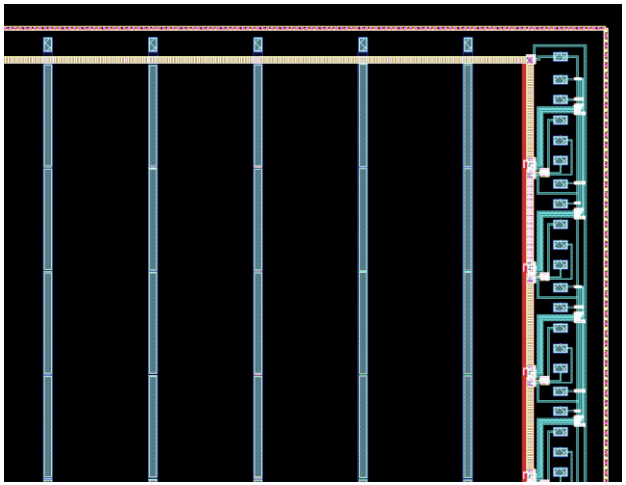


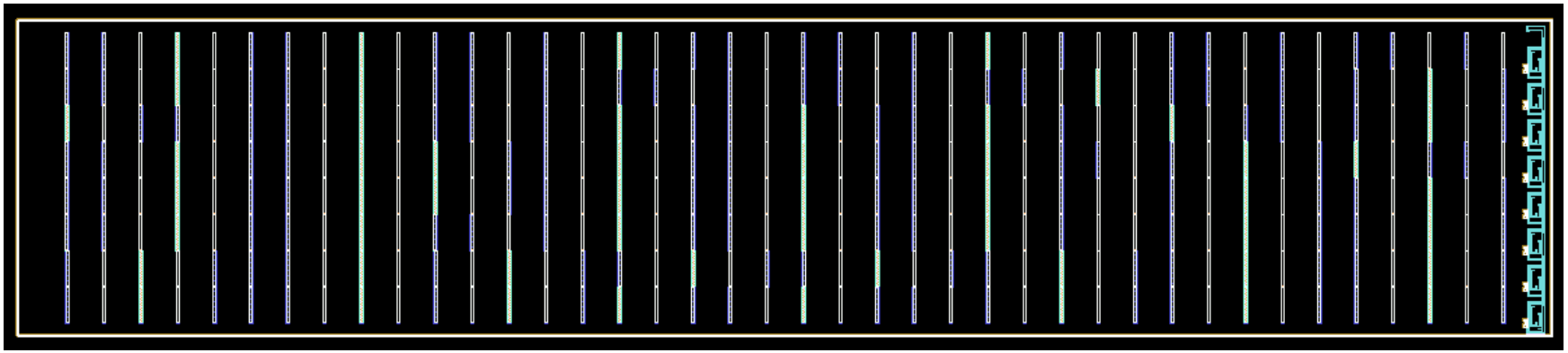




Sensor R&D status

- Large prototype in FY2012
  - 12.3x62.4mm^2 image area
  - 12, 8, 6 μm pixel size
  - 8ch/chip (4ch: 6μm, 2ch: 8μm, 2ch:12μm)
  - Gain: 5μV/electron
  - Layout: almost completed
  - Delivered in October (before DBD deadline)





Readout ASIC R&D

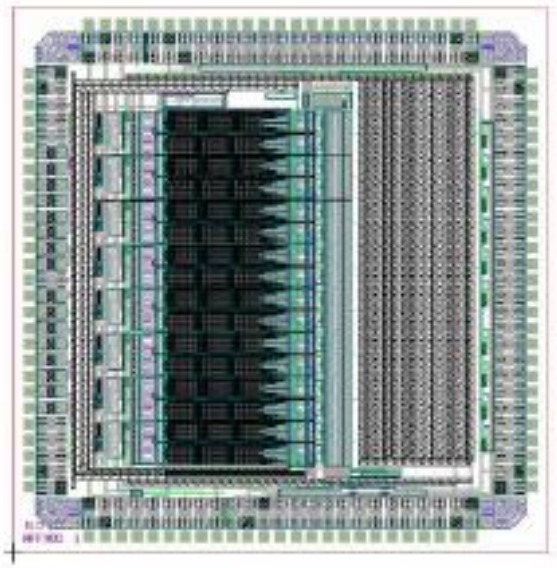
- Prototype ASICs 3 times
  - Preamp+LPF+CDS+ADC
  - 8ch/chip
  - Charge sharing ADCs of 7 bit resolution
  - Two 5MHz ADCs/ch → 10MHz/ch
  - Power consumption target: < 6mW/ch

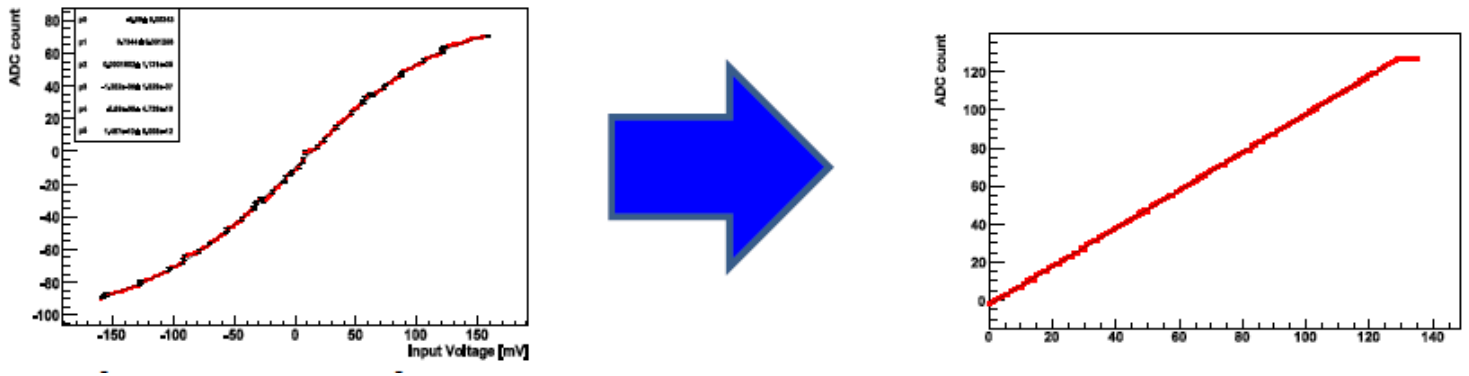
	1st	2nd	3rd
Process [μm]	0.35	0.35	0.25
Speed	×	△ 1)	◯ 2)
Power consumption [mW/ch]	30	30	5.4 2)
Linearity	× 3)	△ 4)	◯ 2)

1) Emitter follower is needed between CCD and ASIC
2) Post-layout simulation results
3) Discontinuity in ADC output
4) Slightly S-shape

Readout ASIC R&D

- 3rd prototype ASIC
  - Layout completed
  - Post-layout simulation and verification underway
  - Submitted in June and will be delivered in August

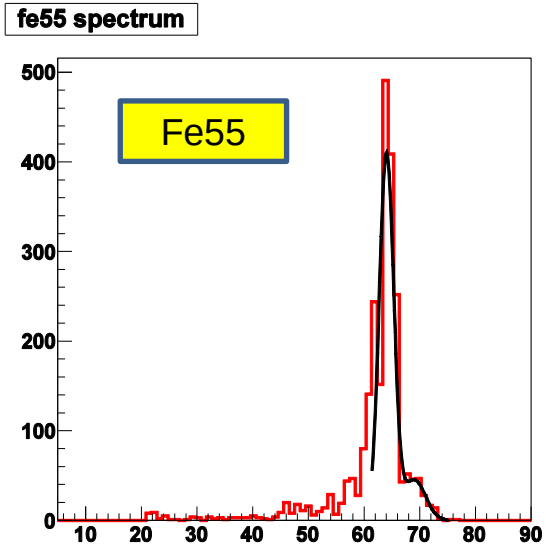


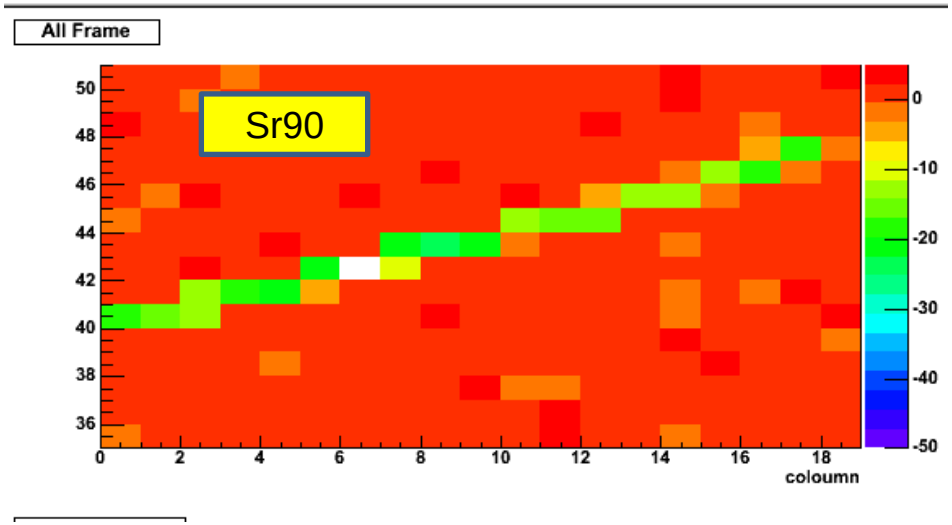


Linearity improvement shown by post-layout simulation

Test with Fe55 & Sr90

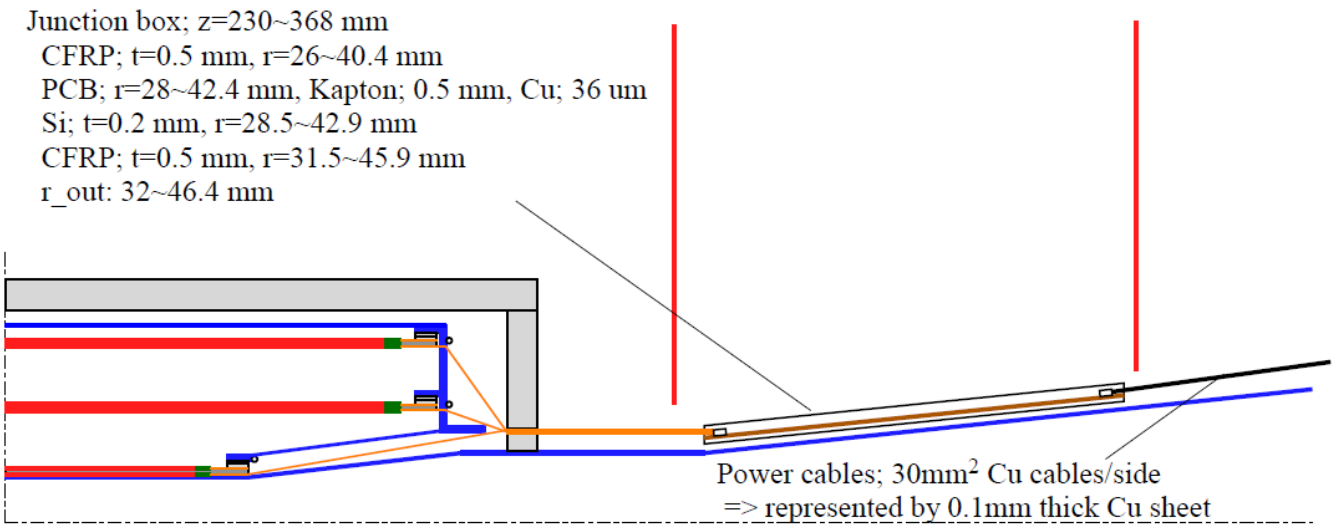
- FPCCD 2008 + 2nd ASIC
- Fe55 X-ray test
  - Operated at −40℃ and 2.5 Mpix/s
  - 5.9 keV and 6.5 keV peaks are observed
  - S/N>40 for 1630 electrons (5.9 keV peak/pedestal width) before non-linearity correction
- Sr90 β-ray test
  - Operated at ~10 ℃ and 2.5 Mpix/s
  - Charge spread to the adjacent pixels is small





Peripheral circuits

- Pig-tail cables (FPC) come out from the cryostat
- Junction box near the cryostat
- The electronics circuit in the junction box includes CCD clock drivers, clock timing generators, signal processors for data reduction, optical fiber cable drivers, etc.
- The junction box (PCBs) are placed surrounding beam pipe
- Patch panel outside the inner support tube

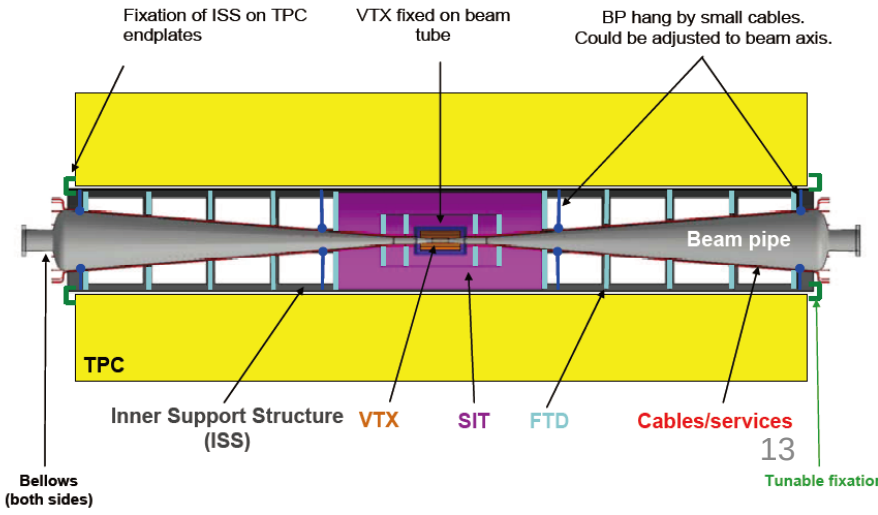


CO2 cooling system

- Operation temperature and power
  - −40℃ from the radiation immunity point of view
  - > 50 W inside cryostat
- Cold nitrogen gas
  - Flow rate of ~1 L/s is necessary to extract 50W power with ΔT=40K
  - Thick cooling tube would be necessary
- Two-phase CO2
  - Flow rate of ~0.15 g/s is necessary to extract 50W power with ΔT~0K (latent heat)
  - Thin tube is OK →
    - Less material budget
    - Less space needed between forward Si disks and beam pipe

CO2 cooling system

- Cooling tube is attached to VTX end-plate and heat produced by CCD output amp and ASIC is removed by conduction through CFRP ladder (simulation study for thermal design is necessary)
- Return line of CO2 will be used to cool the electronics outside the cryostat (~200W/side)
- Inner support tube should be air-tight and filled with dry air/nitrogen in order to prevent condensation on the CO2 tube



R&D plan

- FPCCD sensor and readout ASIC
  - Large prototype sensor + 3rd ASIC → Demonstrate to work by the DBD deadline
  - Beam tests to confirm σ~1μm: 2013~2014
  - Radiation immunity test: 2013~2015
- Engineering R&D
  - Circulating 2-phase CO2 cooling system using a CO2 compressor and condenser : 2012~2014
    - Possibility of one compressor system for all sub-detectors (−40℃ – +15℃)
  - Full-size engineering prototype: 2014~2015