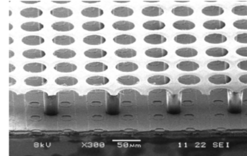
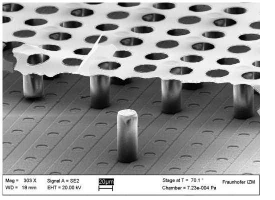
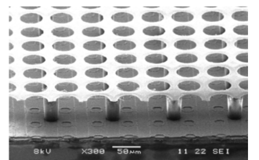




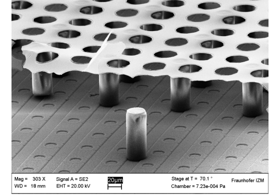
Status of the European Pixel Modules

J. Kaminski
for
U. Bonn, NIKHEF, SACLAY

LCTPC Collaboration Meeting, DESY
26th-27th March 2012



Why highly pixelized modules?



Standard MPGDs use pads of the size O(mm^2) or long strips with a pitch of O(100-200 μm).
This does not fully exploit the resolution of MPGDs.

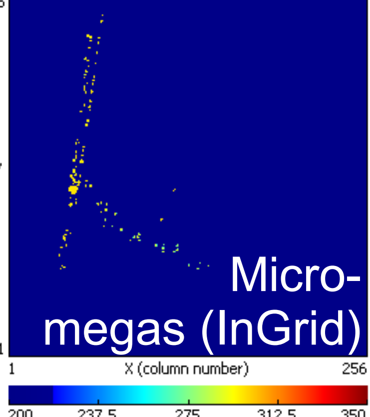
72x24 pads of ~3x7 mm^2

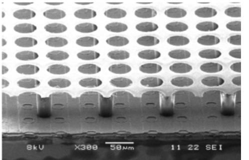
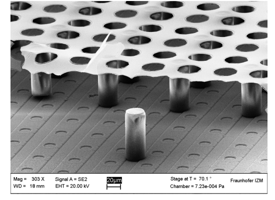
B = 1 T

Need smaller pads O(50-100 μm) => Timepix

Timepix

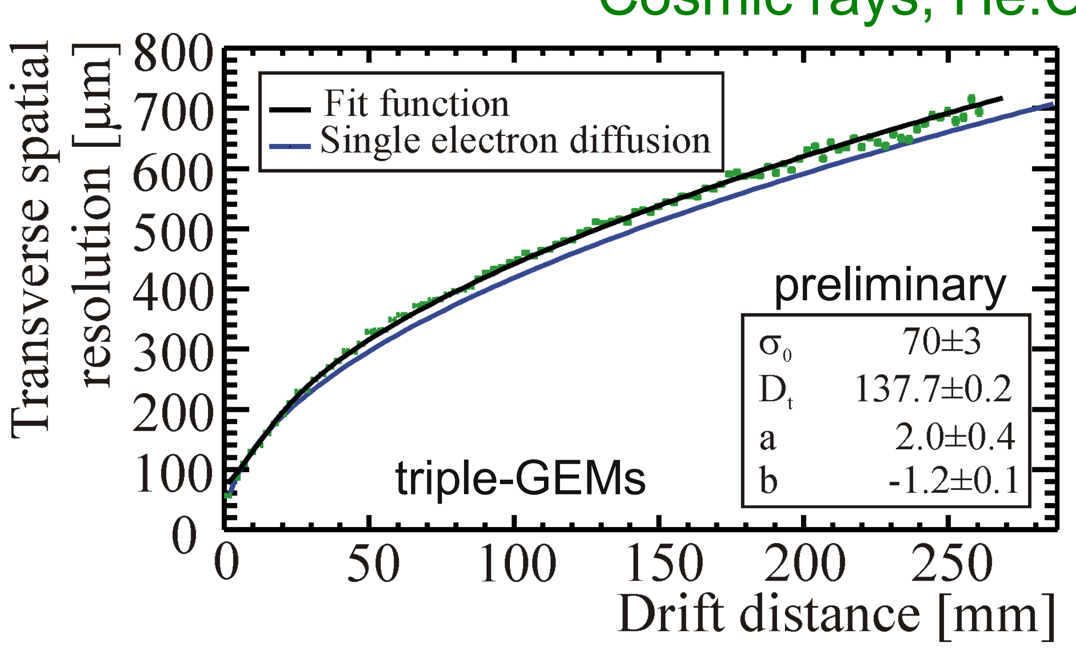
5 GeV e^- beam

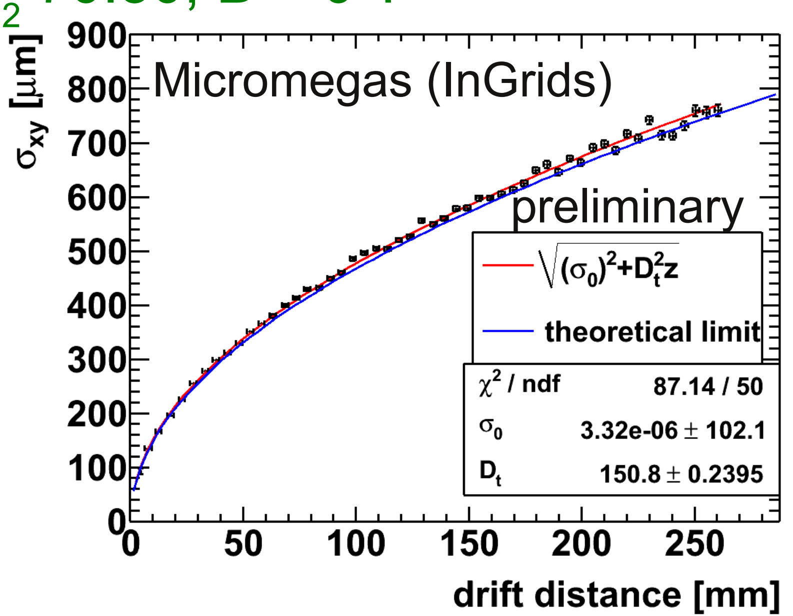


Excellent performance in small prototype detectors

Cosmic rays, He:CO_2 70:30, B = 0 T





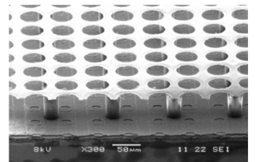
Fit function:

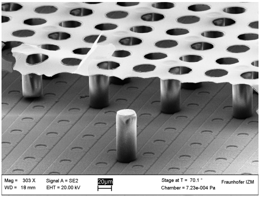
$\sigma = \sqrt{\sigma_0{}^2 + D_t{}^2 z/(1 + a\, e^{bz})}$

Theoretical limit:

Single electron diffusion

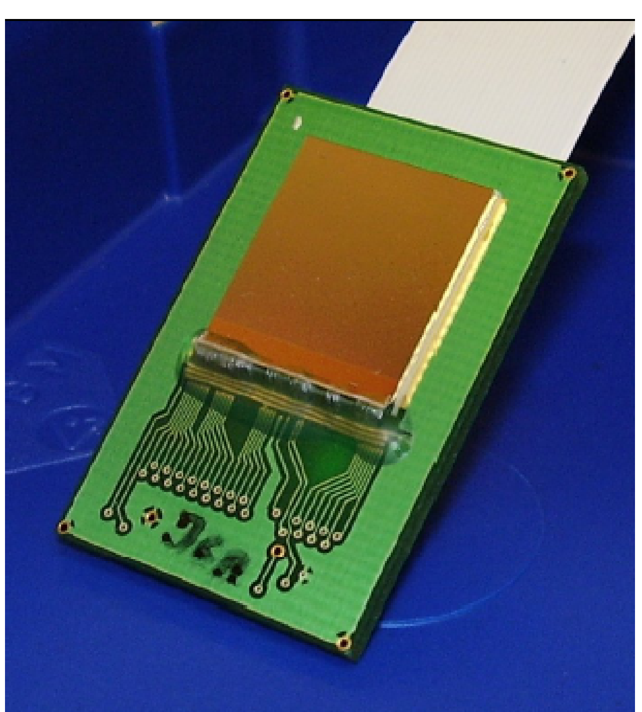
$\sigma = D_t \sqrt{z}$





Timepix chip

Bare CMOS chip is placed below the gas amplification stage (GEM or Micromegas), bump bond pads act as charge collection pads.



Timepix chip derived from MediPix-2

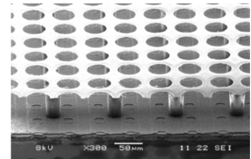
256 × 256 pixels

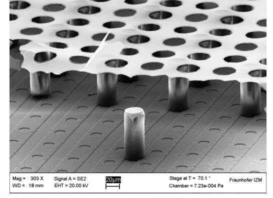
Pixel size: 55 × 55 μm²

Chip dimension: 1.4 × 1.4 cm²

Each pixel can be set to one of these modes:

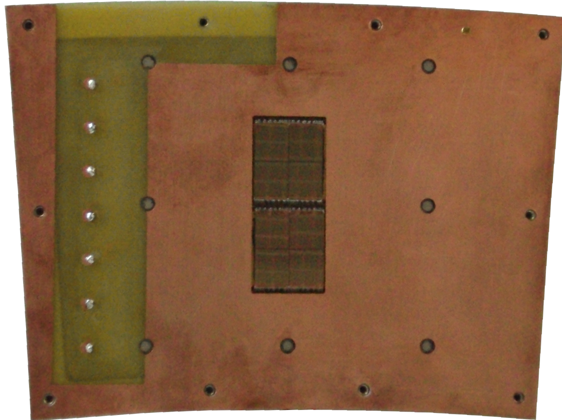
- Hit counting
- TOT = time over threshold gives integrated charge
- Time between hit and shutter end



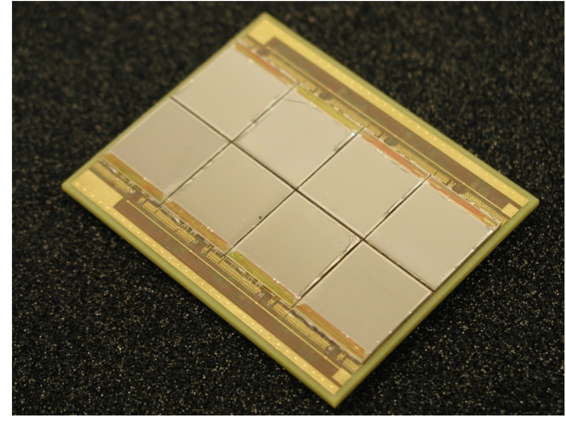


Past LP-modules

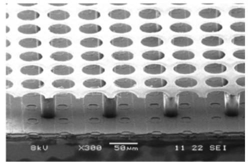
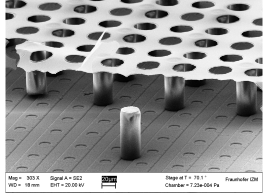
LP-modules were built with the two different gas amplification stages



Triple-GEM U Bonn/Freiburg
3 standard CERN-GEMs
2 NIKHEF-Quadboards read out by MUROS
synchronized with EUDAQ/TLU

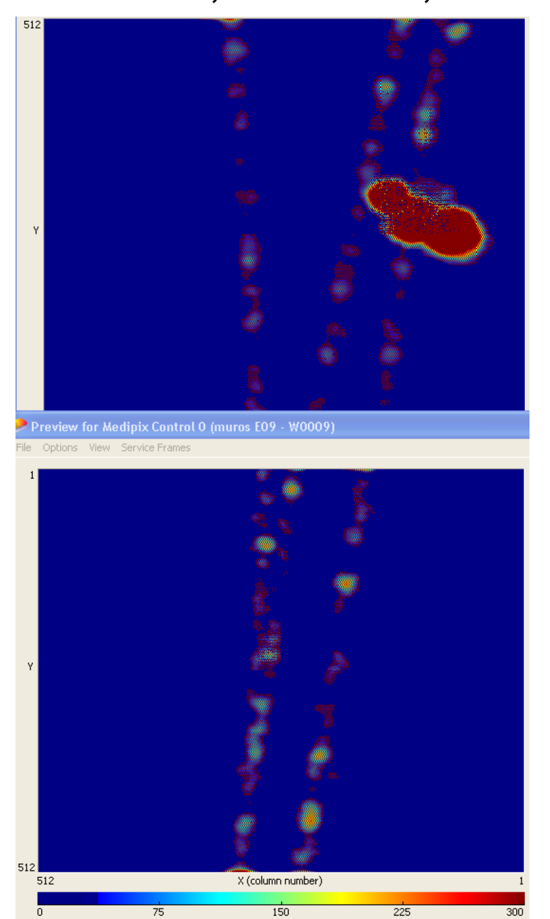


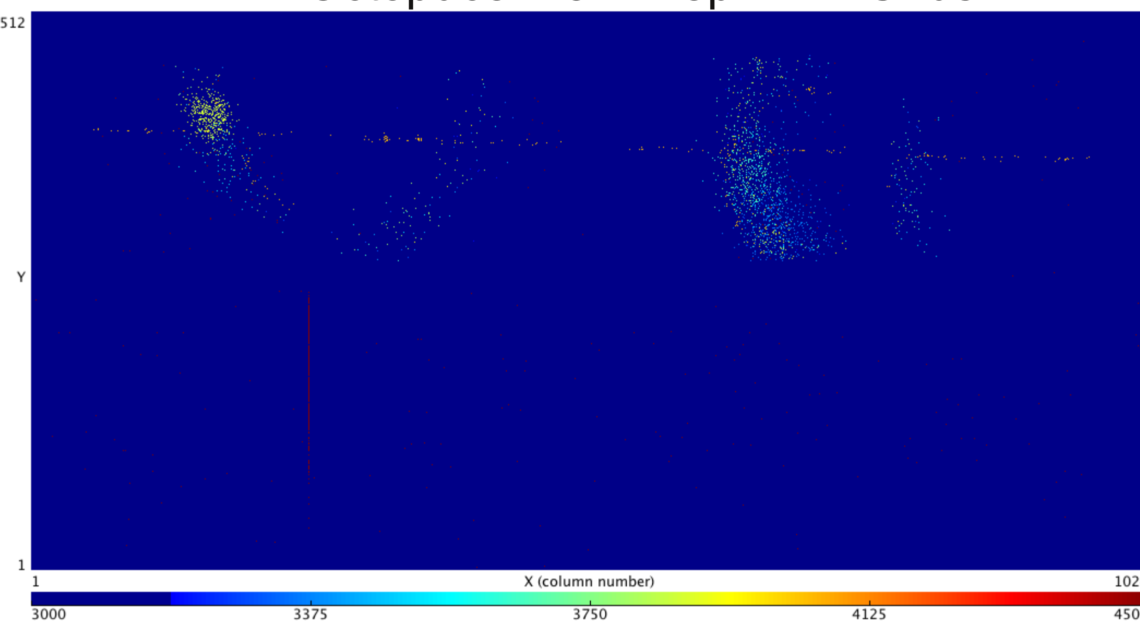
InGrid SACLAY/NIKHEF
8 InGrids on a custom designed board Octopuce read out by one MUROS

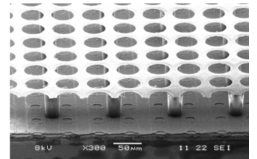
Example event

tGEM: T2K, d = 6 cm, B = 1 T

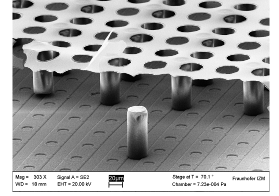




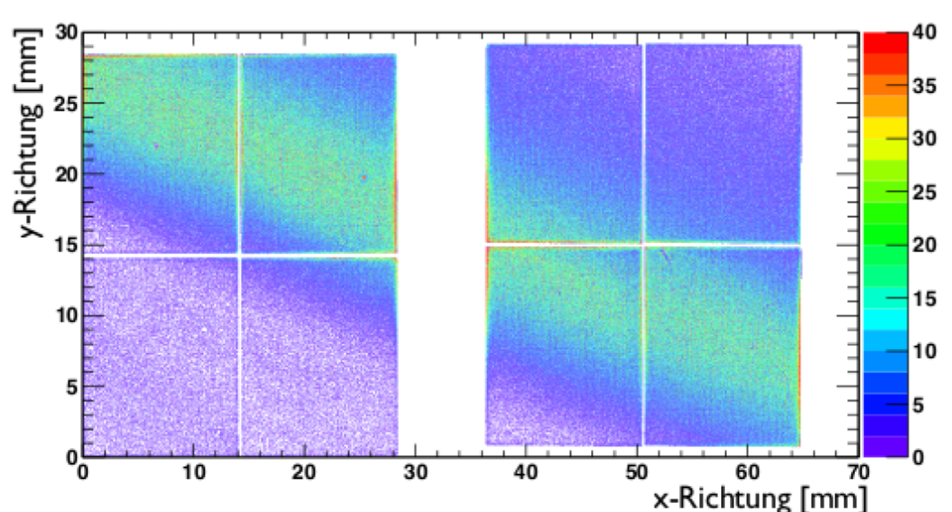
He/iC_4H_{10} 80/20 V_{grid} = -400 V B = 1 T

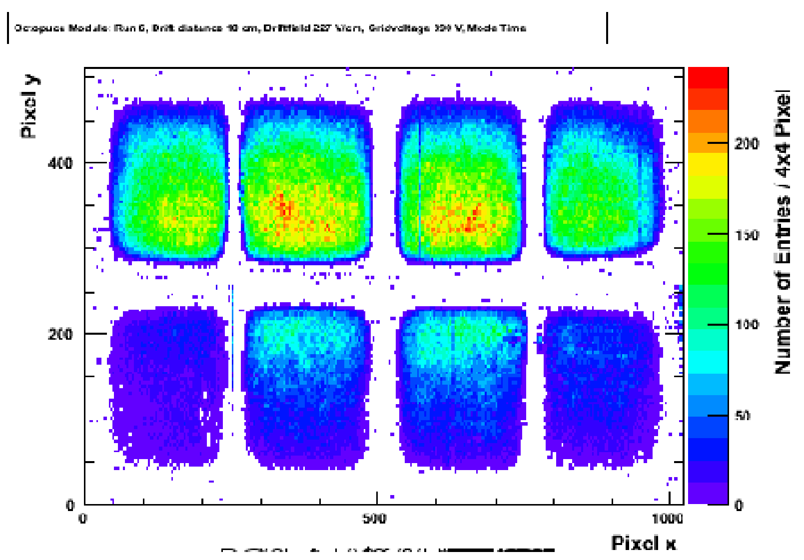


Results from past modules

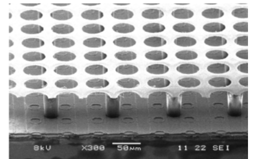


For both modules the results were not as good as expected:
- Triple-GEM module suffered from inhomogeneous B-fields
- InGrid module suffered from E-field inhomogeneities between Grids and due to bonding wires.

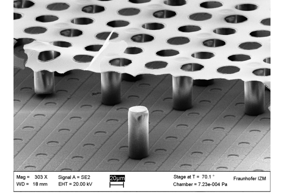




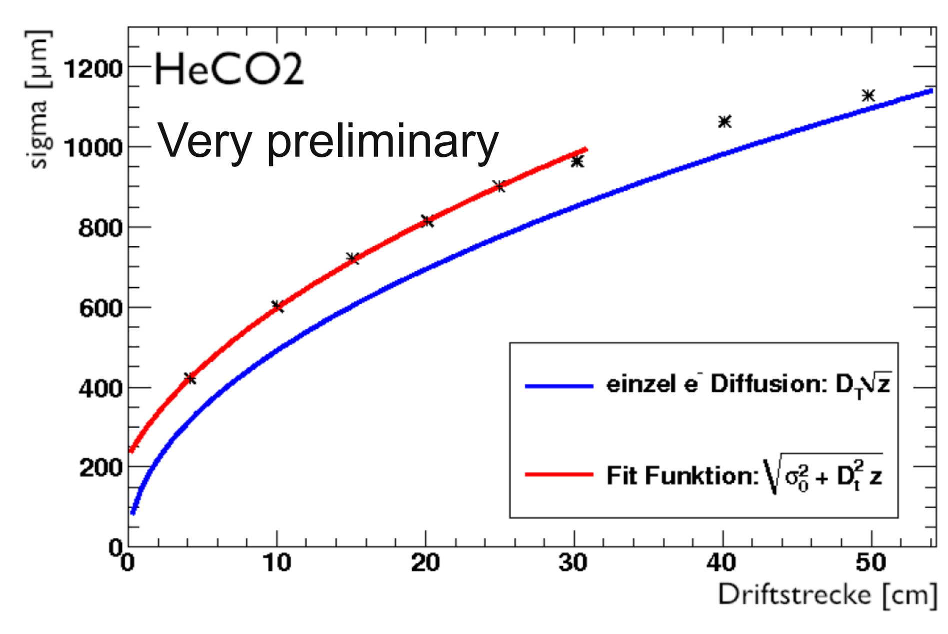
Improved modules are being designed.

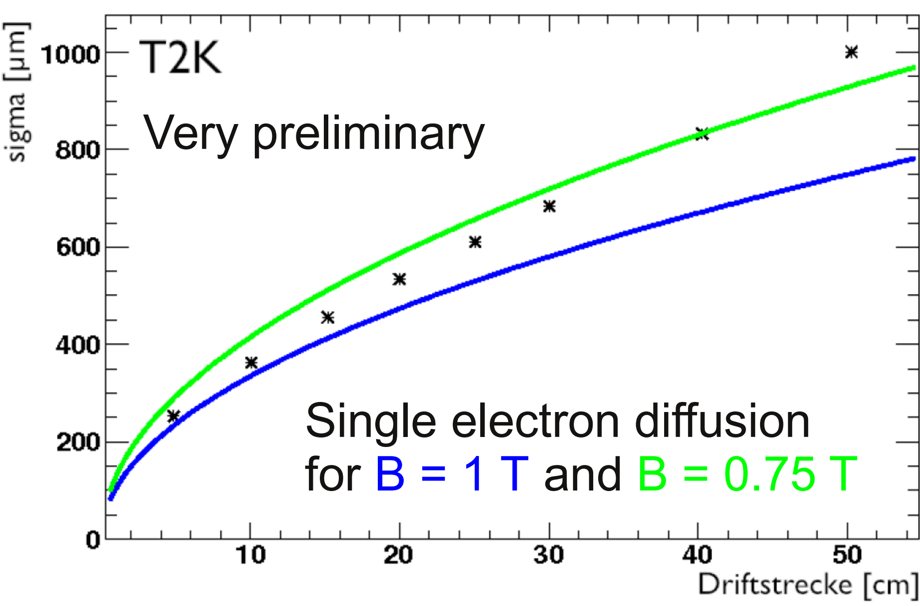


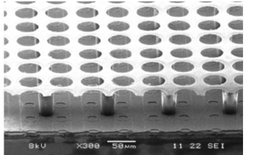
Some more results for tGEM



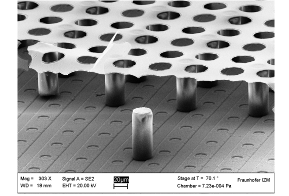
Data was taken before PCMAG was placed on a movable stage.
=> field inhomogeneities were more prominent as was observed with GEM and MM modules



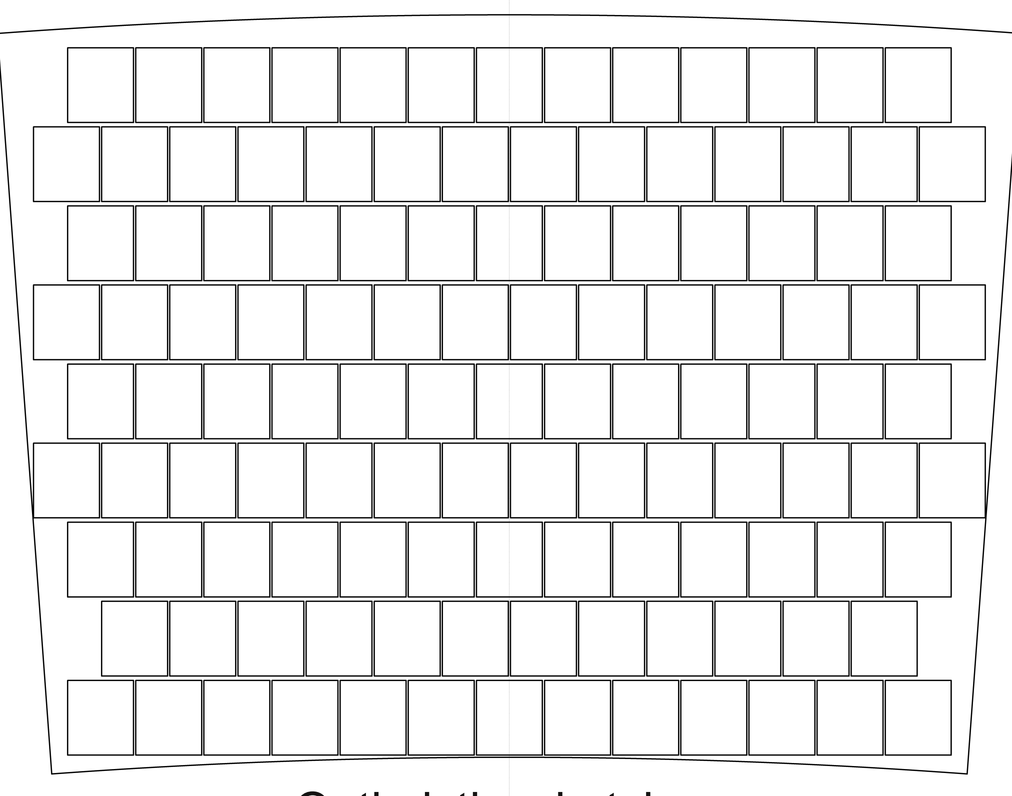




Road map towards a full module



A fully equipped module could hold up to 120 Timepix chips.
This raises several issues, which have to be solved:



Optimistic sketch

Production of InGrids:

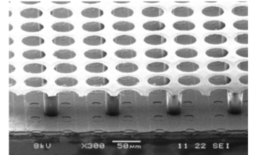
current production technique single/9 InGrids at the Twente, production takes about a week producing 120 is unrealistic

Cooling

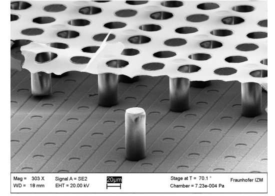
each TP produces ~1 W
→ have to cool ~ 120 W

Readout

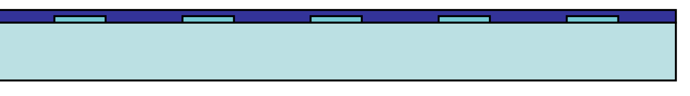
current readout (MUROS) is not scalable nor in production



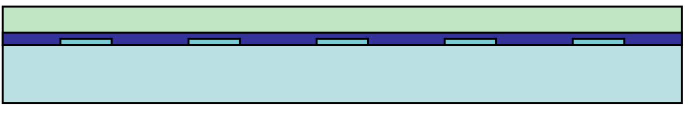
Production of new InGrids (I)



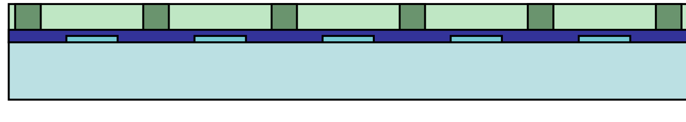
A new wafer-based production process is being established at IZM, Berlin



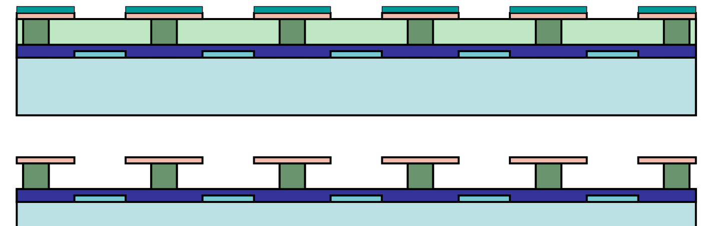
1. Formation of Si_xN_y protection layer (done at Twente)



2. Deposition of SU-8

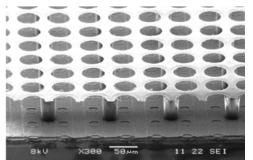


3. Pillars-like structure formation

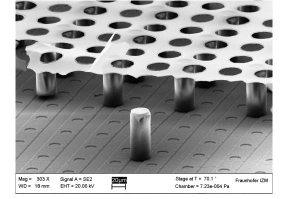


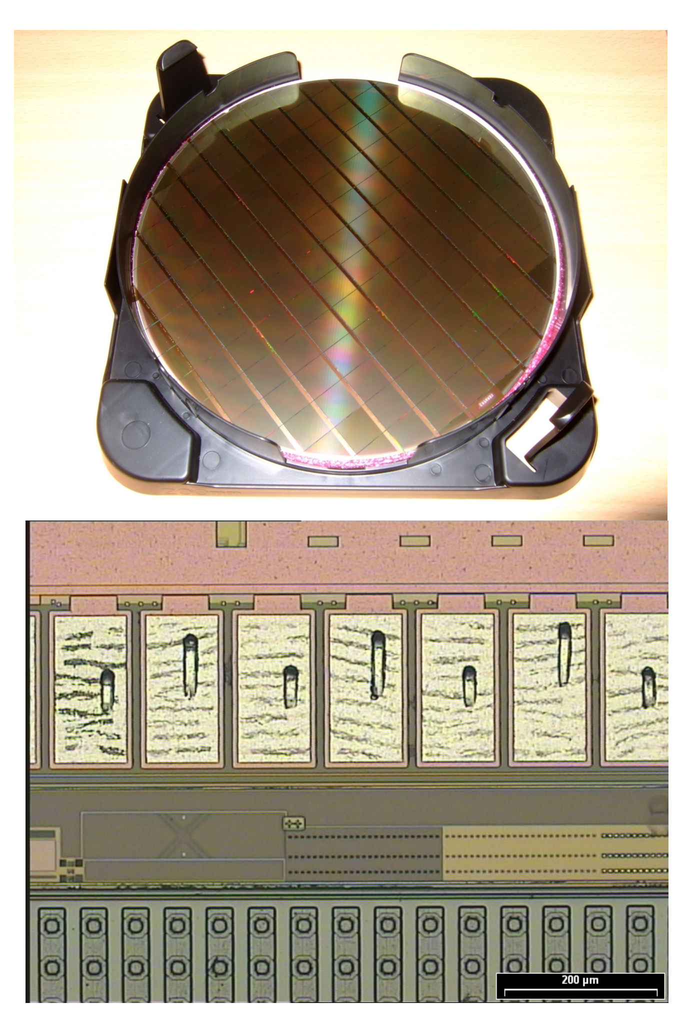
4. Formation of Al grid
   4b dicing of wafer
5. Development of SU-8

Process not quite straight forward: protection layer and SU-8 development difficult



Production of new InGrids (II)





Protection layer should cover only active area, not wire bond pads.

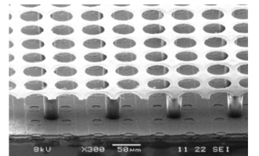
=> bond pads have to be protected

Use polyimide layer

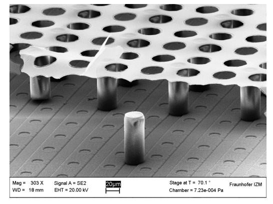
- Spinning
- Baking
- Exposition
- Development
- Silicon nitride deposition
- Chemical activation of polyimide
- Stripping

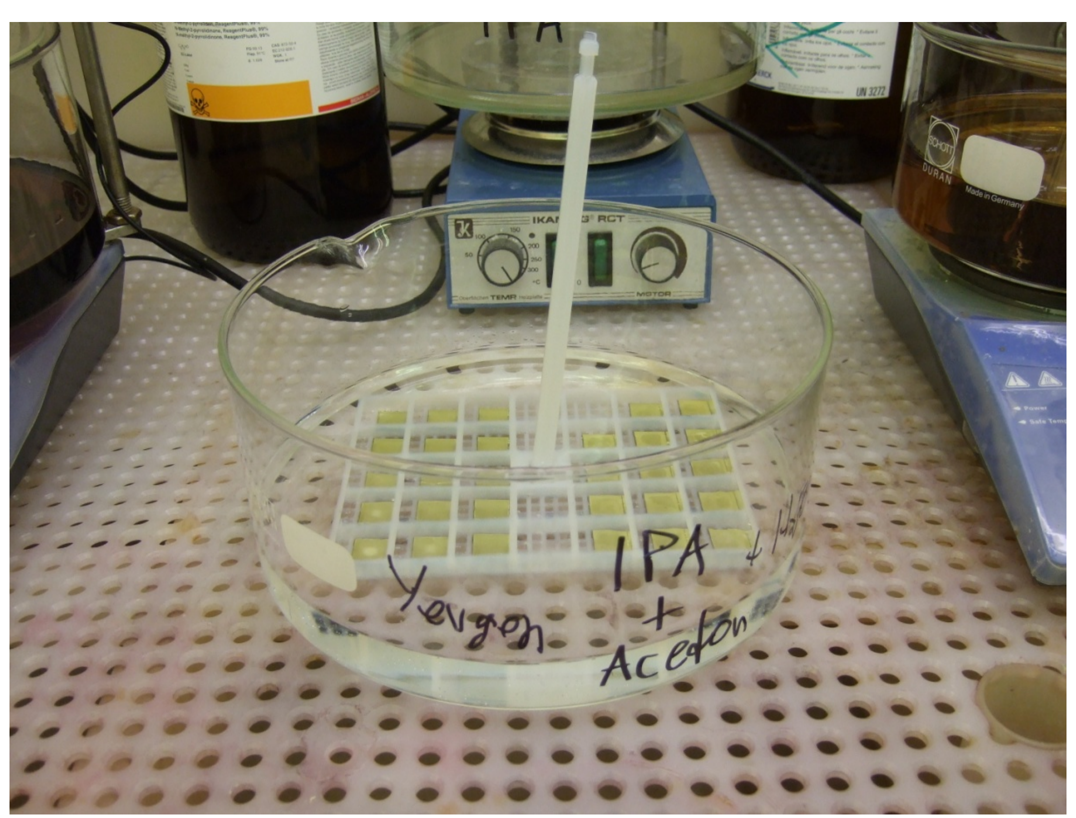
Advantage: Silicon technology compatible, perfect alignment, no residuals

Disadvantage: temperature sensitive process, time consuming process, mechanical scratching of bonding pads



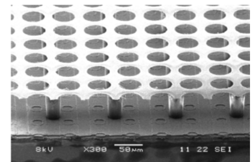
Production of new InGrids (III)

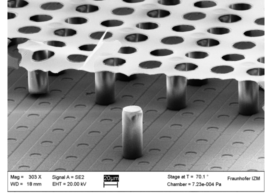




Development of SU-8
1) Acetone
2) Acetone:IPA:H_2O (1:1:2)
3) Acetone:IPA:H_2O (1:1:1)
4) Acetone:IPA (1:1)
5) Microstrip 6001
6) H_2O
7) IPA
8) Acetone
9) Drying in the air

Has to be done after dicing to ensure the stability of the grid during dicing

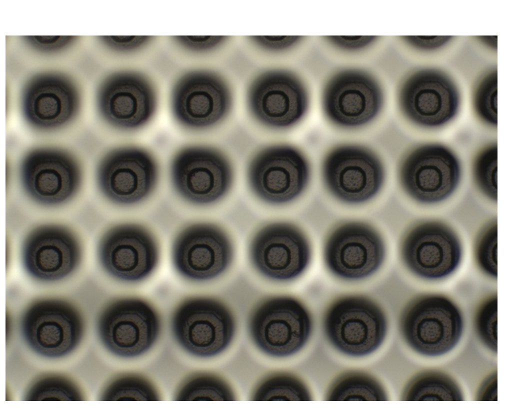


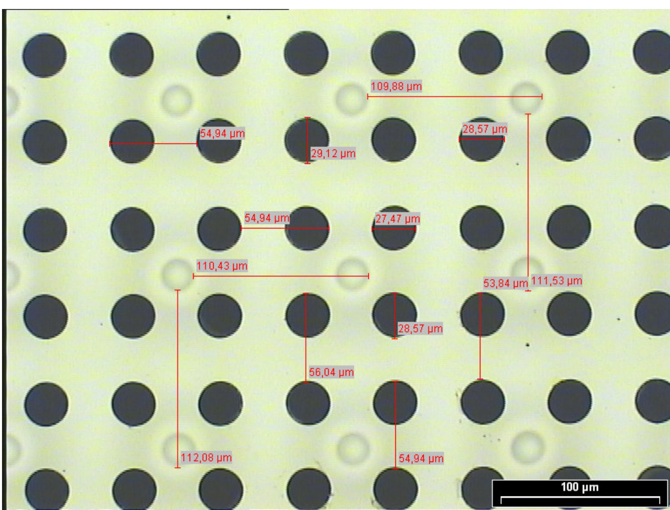


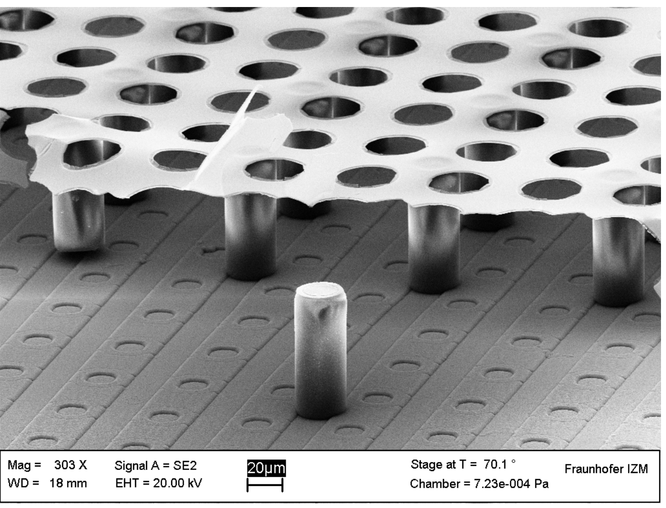
Status of production

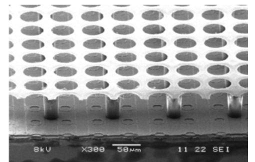
First wafer (fall 2011) was a test run
→ several problems with protection layer and SU-8 development

Second wafer (December 2011) yielded >64 good InGrids
delivered to Bonn, NIKHEF, Saclay
Grids look very good, are robust and of high quality

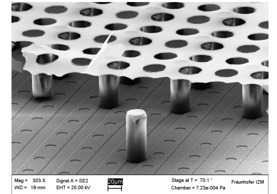








First results with new InGrids



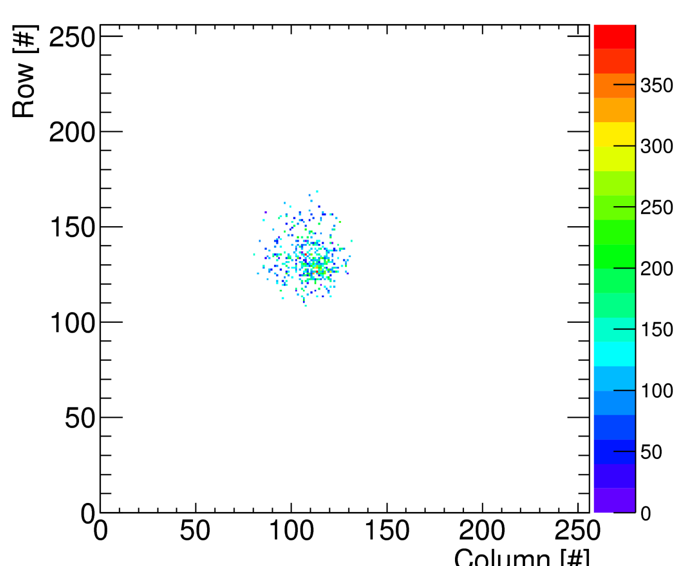
Drift field: 200 V/cm

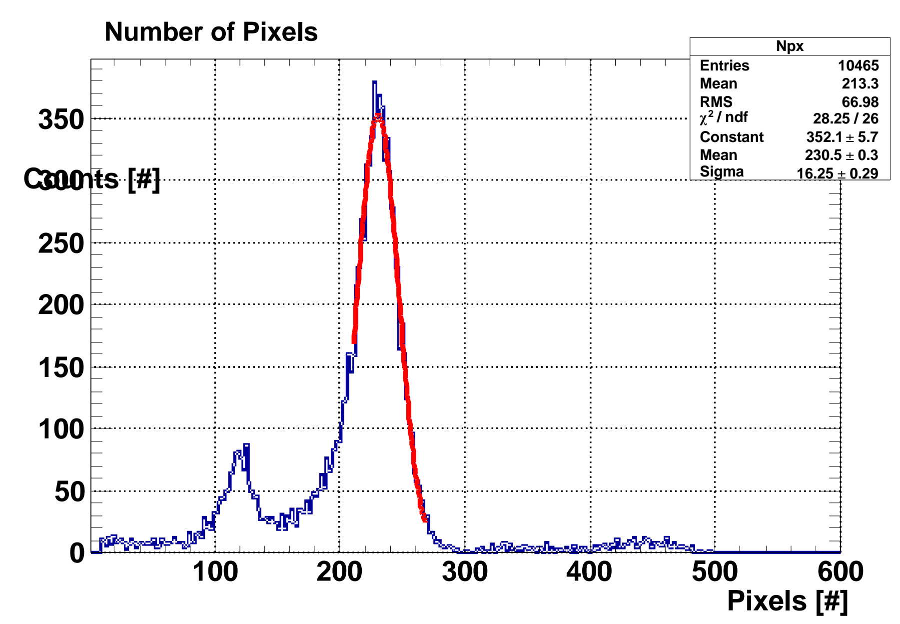
Grid voltage: 350 V

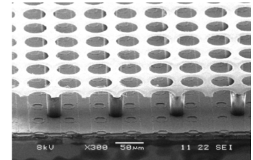
Gas mixture:
Ar:iButane 95:5

Source ^{55}Fe

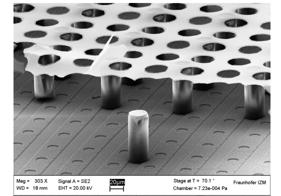
Energy resolution σ_E/E:
7.0 % (pixel spectrum)







Some more improvements



… are needed for the protection layer

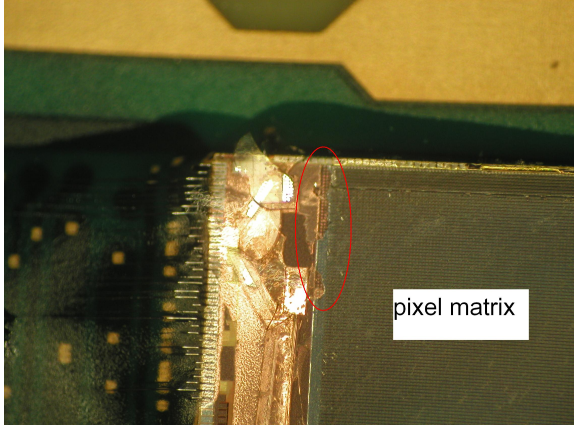
Twente-InGrids: survive months/years of operation
New IZM-InGrids die after 2 weeks (or less)

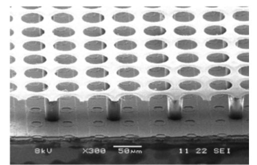
Investigation has started
(google spreadsheet to collect information from all institutes,
detailed optical and mechanical inspection of broken chips, …)
a few ideas have been voiced

Timepix wafers (chips) control

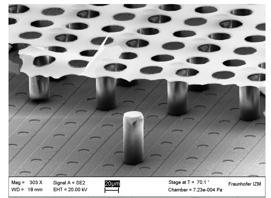
Chip ID	Type (Initial probing)	Final postprocessing		Final control	Location		Responsible person			Operational experience		
	(A/B/C/D/E/F)	Date	Comments	Comments	Date	Location	Date	Name	Purpose	Commissioning (Date)	Maximum HV reached (Gas - default: Ar/iButane 95/5)	Grid leakage current [nA]
F7	C			bad grid	-	-	-	-	-	-	-	-
G7	B				14.12.2011	Saclay						
H7	C			bad grid	-	-	-	-	-	-	-	-
I7	A				14.12.2011	Bonn						
J7	A				14.12.2011	Bonn						
K7	A				14.12.2011	Bonn	12.01.2012	Thorsten Krautscheid	General testing	08.03.2012	400 V (Ar/iButane 95/5)	0.05 nA
L7	A				14.12.2011	Bonn						
M7	F	-	-	-	-	-	-	-	-	-	-	-
B8	A				14.12.2011	Nikhef						
C8	A				14.12.2011	Nikhef						
D8	B				14.12.2011	Saclay						
E8	B				14.12.2011	Saclay						
F8	B				14.12.2011	Saclay						
G8	D				14.12.2011	Bonn						

Wafers info | Blank template | Blank template - Revised | E85MXGX - W0056 | EL5MX3X - W0057 | EW5MWBX - W0058





Readout electronics

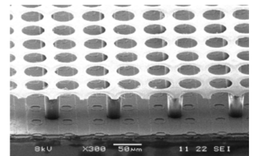


A successor of MUROS has to be used in next LP-module.

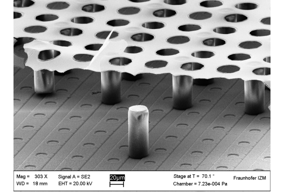
2 candidates:

1) RELAXD system of NIKHEF
   - very fast (4 chips are readout in parallel)
   - commercially available
   - FPGA placed directly on backside of chip carrier

2) Scalable Readout System
   - scalable up to large numbers of chips
   - based on SRS of RD51 → many groups have already the hardware from other applications
   - FPGA-code for Timepix readout developed by U Mainz and U Bonn within AIDA - see presentation of M. Lupberger on Wednesday



Scalable Readout System

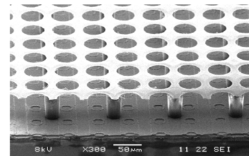


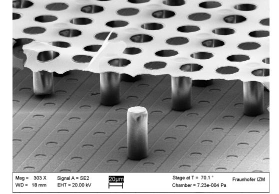
DAQ is a command line C++ program Interfacing to EUDAQ

For large systems a SRU is needed

Quasi-passive adapter card need to interface the FEC (FPGA)

Chip carrier with 8 Timepix chips (up to 16 possible, but reduces readout speed)





SRS with Timepix

Currently: VHDCI 68-pin cable

Timepix ASIC on chip carrier

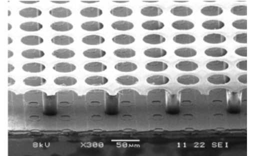
passive A-card

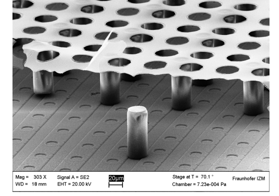
Intermediate board (layout out for up to 8 chips)

JTAG connector

SRS FEC with Virtex 5 FPGA

Ethernet connection to SRU / PC



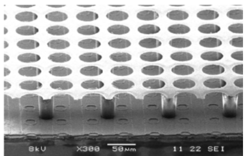


Status

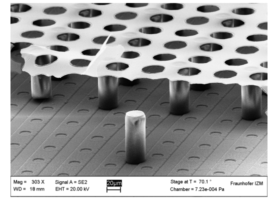
Code has been tested on a separate Xilinx test board.
Readout rates of ~50 Hz could be reached with a single chip.
Code is now being tested with SRS
- communication has been established between SRS

Further steps with SRS

Implementation of additional functionality
(equalization, calibration, map handling, …..)
Hardware modification (different, longer cable, ...)
Development and testing of multi-chip carrier
Integrating EUDAQ

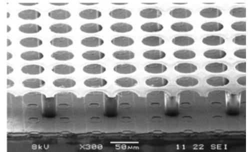


What remains to be done?

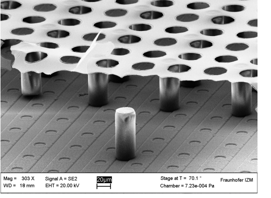


- Improve protection layer
- Implement improvements in SRS readout
- Work on layout of module:
  - Where to place chips (small carrier with 8 chips vs. large one)
  - Services
    - Cooling
    - Power distribution
    - HV distribution
- Minimize field distortions in case of InGrids
- Improve 'pixel-branch' of MarlinTPC code (tracking, δ-exclusion..)

Possible roadmap: first a module with DESY-GEMs gas amplification
(chips are easier to handle – some issues can be addressed)
then one with InGrids, where handling is more delicate



Outlook – even further in the future



Successor Chip Timepix-3
- Design, production and testing
- Build InGrids with Timepix-3

Through Silicon Vias:
- Colleagues at Bonn (N. Wermes / SiLab) are exploring this new Techniques in the context of ATLAS with different chips but in collaboration with IZM

Once they succeed, we try to copy the process with Timepix

Some more basic R&D:
e.g. new materials (ceramics for pillars, GEMGrids, piggy-back Micromegas, ...)