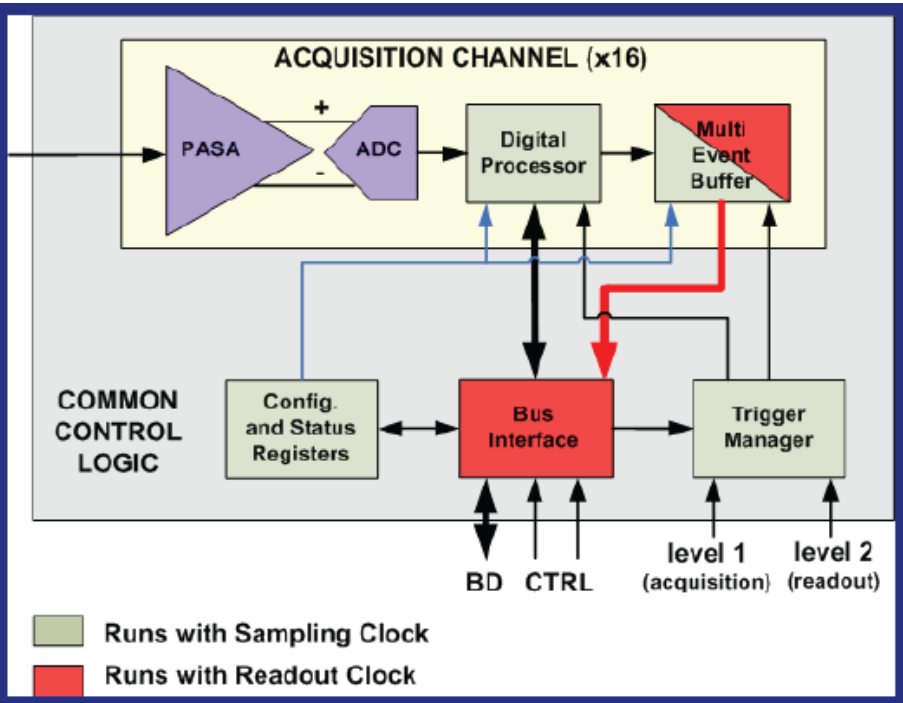
Irfu - CEA Saclay
Institut de recherche sur les lois fondamentales de l'Univers

GdSP ASIC Development status

Eric Delagnes slides mainly from
P. Aspell (CERN)
& F. Guilloux (Saclay)

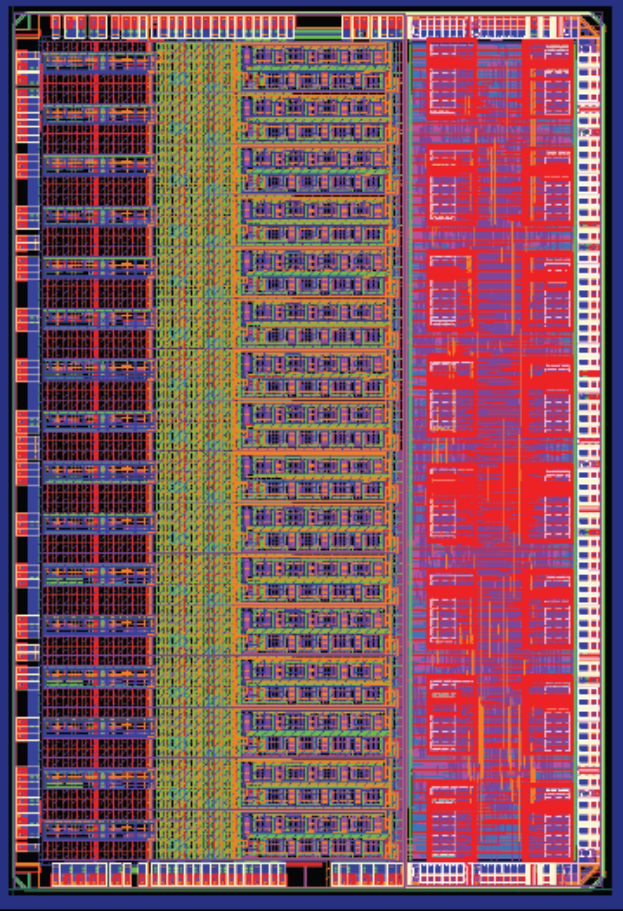
Tuesday, March 27, 2012

SALTRO16



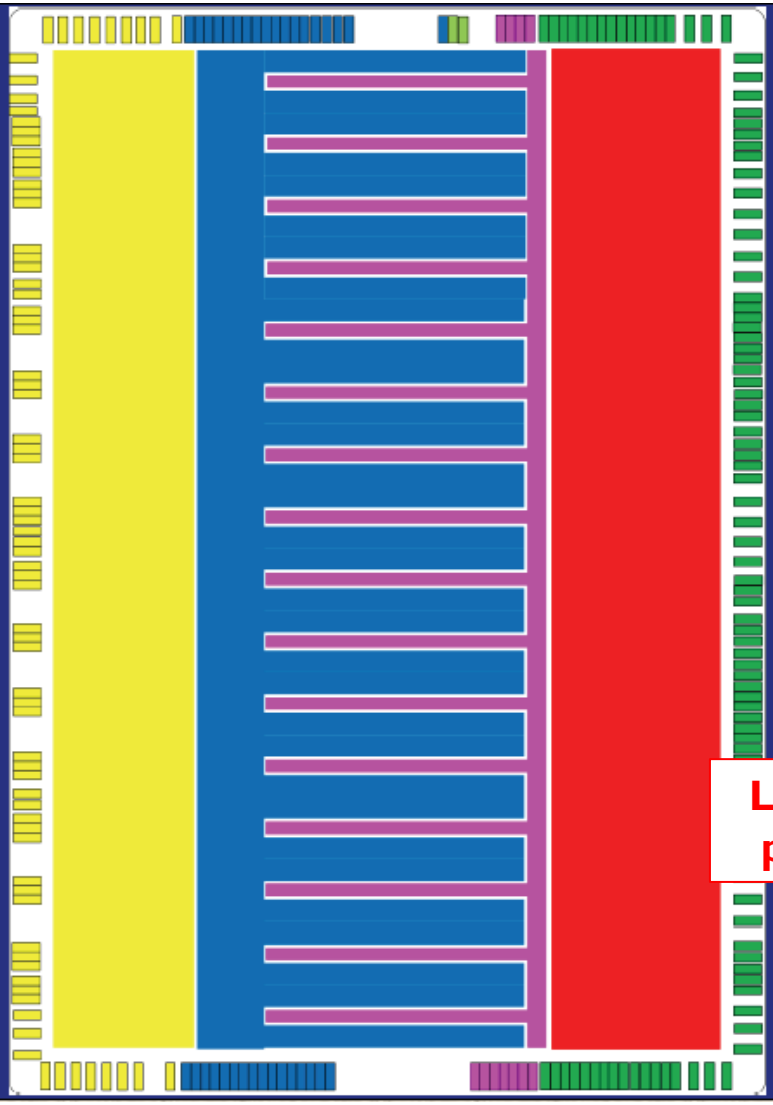
Designed in 2009-2010
Beautiful success.
First chip integrating low noise FE, ADC & DSP

Technology :
IBM 130nm
CMOS



Luciano Musa ..... S-Altro Specs. & Architecture
Paul Aspell ..... Coordinator of design
Designers :
Massimiliano De Gaspari ..... Front-end + ADC
Hugo França-Santos ..... ADC core
Eduardo Garcia ..... Data Processing & Control

SALTRO16: Power consumption



Power domains:

PASA analog

ADC analog

ADC digital

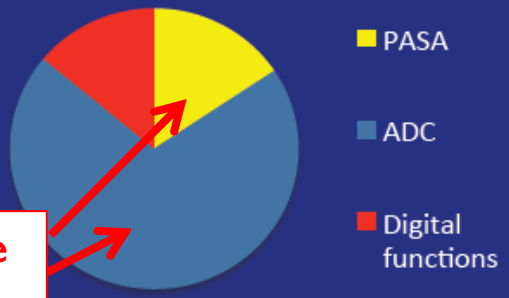
Digital core

Digital Pads

PASA ~8mW/ch,
ADC 36mW/ch @40MHz
Digital functions ~114mW
Total power ~ 750mW

Succesful power pulsing operation

Power Distribution for 16 channels



Large gain are possible here

It is clear that the ADC power consumption limits the design to small channels counts.

But times are changing.

From SALTRO16 to GdSP

… or **Gas Detector Signal Processor**
Go Digital as Soon as Possible

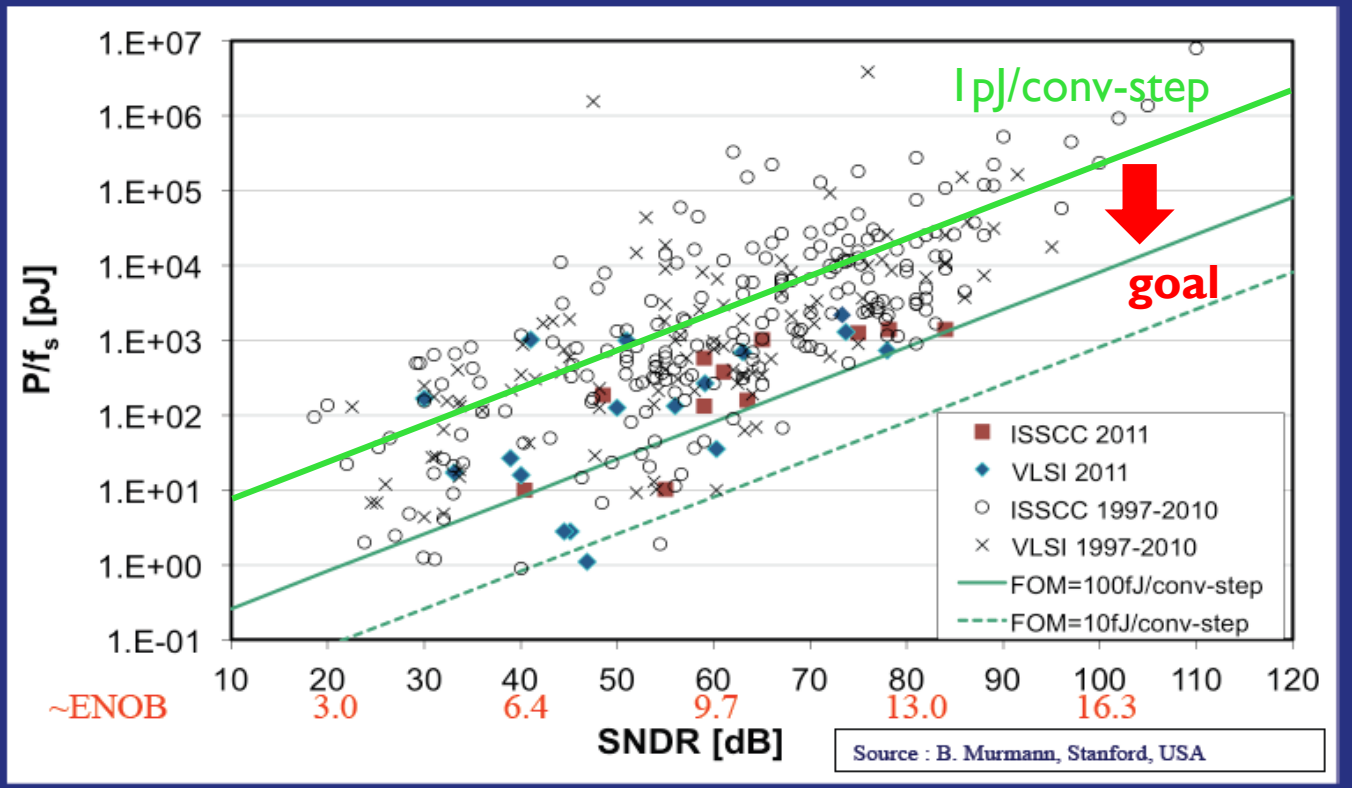
- Larger number of channels (16 => 64): **more compact**
- **Lower power consumption:**
  - ADC,
  - Front-end.
- Larger versatility, programability (gain, shaping, range of Cin).
- Optimization of DSP.
- New readout.
- But large design effort required (~10 man.y) and (S)ALTRO team is no more available:
  - ⇒ Common design for CMS muon upgrade and for LCTPC.
  - ⇒ International design team led by P.Aspell (CERN).

ADC technology Trends

- FOM ~ P / (2^{ENOB}. 2BW)

- 1pJ is high
- (~40mW @ ENOB 9, 40MS/s)
- 100fJ is good
- (~4mW @ ENOB 9, 40MS/s)
- 50fJ excellent
- (~2mW @ ENOB 9, 40MS/s)

Rise of new architectures: as asynchronous SAR



State of the art :

A 30fJ/conversion 8b 0 to 10MS/s Asynchronous SAR ADC in 90nm CMOS. P. Harp et. al. IMEC ISSCC 2010
[They measured 69uW at 10MS/s,]

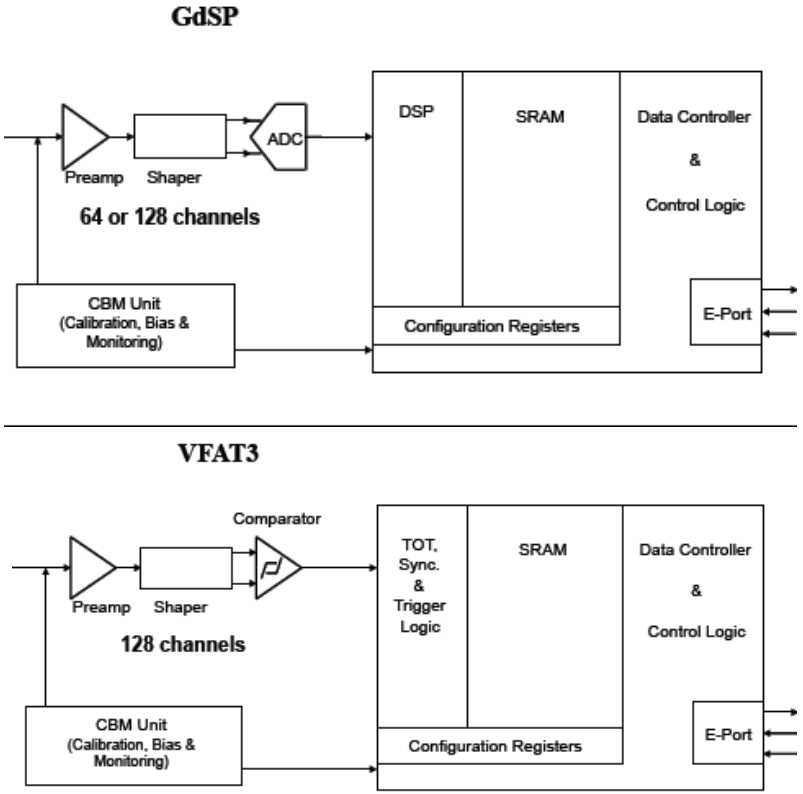
A 550uW 10b 40MS/s SAR ADC with Multistep Addition-only Digital Error Correction, *Sang-Hyun Cho et al.*
CICC 2010 *(FOM = 42fJ/conversion)* designed in 0.13um CMOS

GdSP ASIC

- Join effort to have one ASIC for 2 projects. Or at least large common parts.
  - LCTPC (AIDA)
    - ➔ **specifications derived from SALTRO16**

    (slower, low cap)
  - Muon CMS upgrade :
    - First option :VFAT3 ASIC = PSD chip
    - Second option : GdSP ASIC
    - VFAT3 & GdSP share half of their blocks (i.e. Front End, SRAM …)
    - ➔ **Specifications derived from previousVFAT2**

    (faster, high cap)

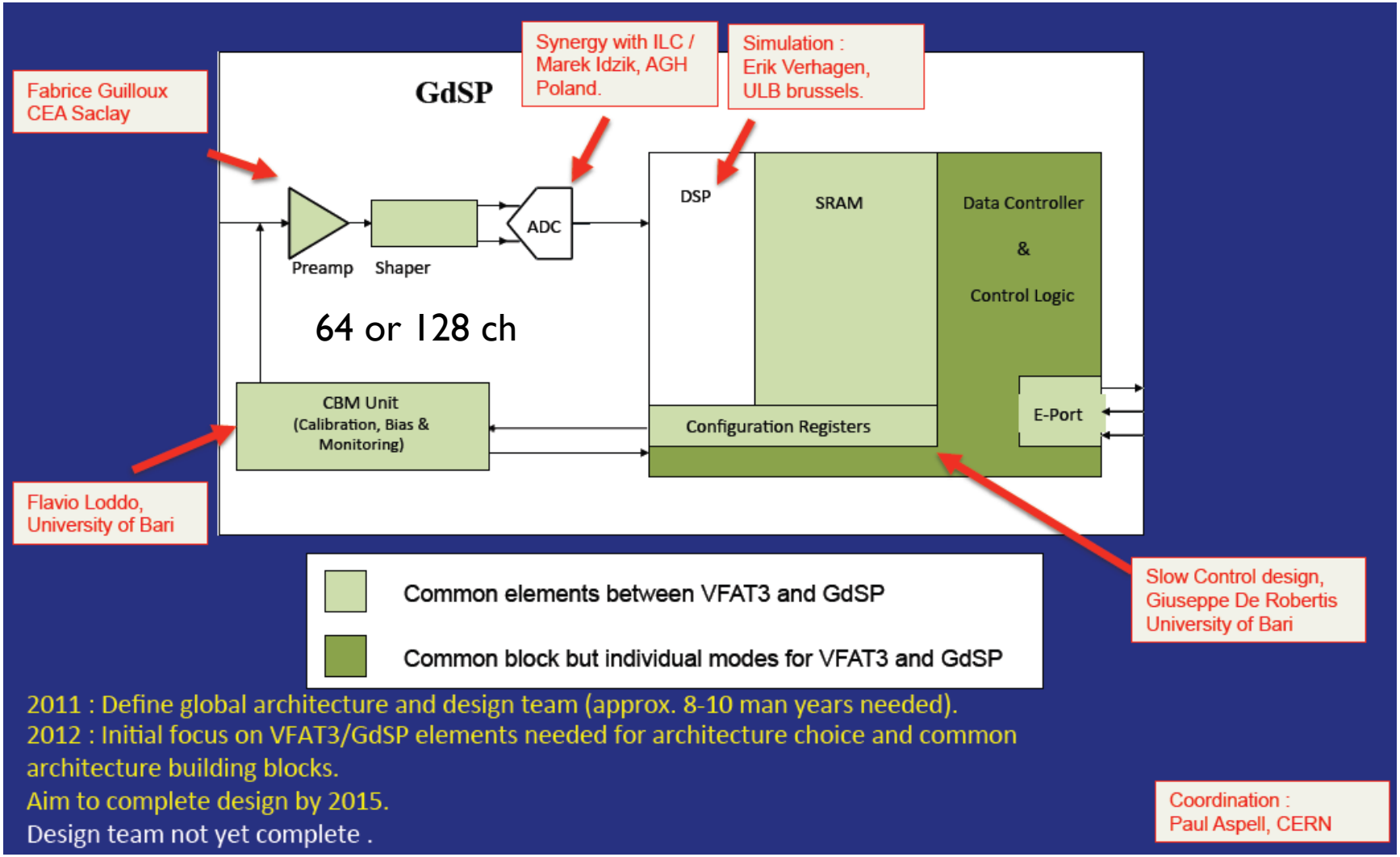


- The technology issue:
  - Long term project (> 2014-2015)
  - Uncertainties on the future of IBM 130nm ?
  - Cern is moving to TSMC technology for 65nm technology.

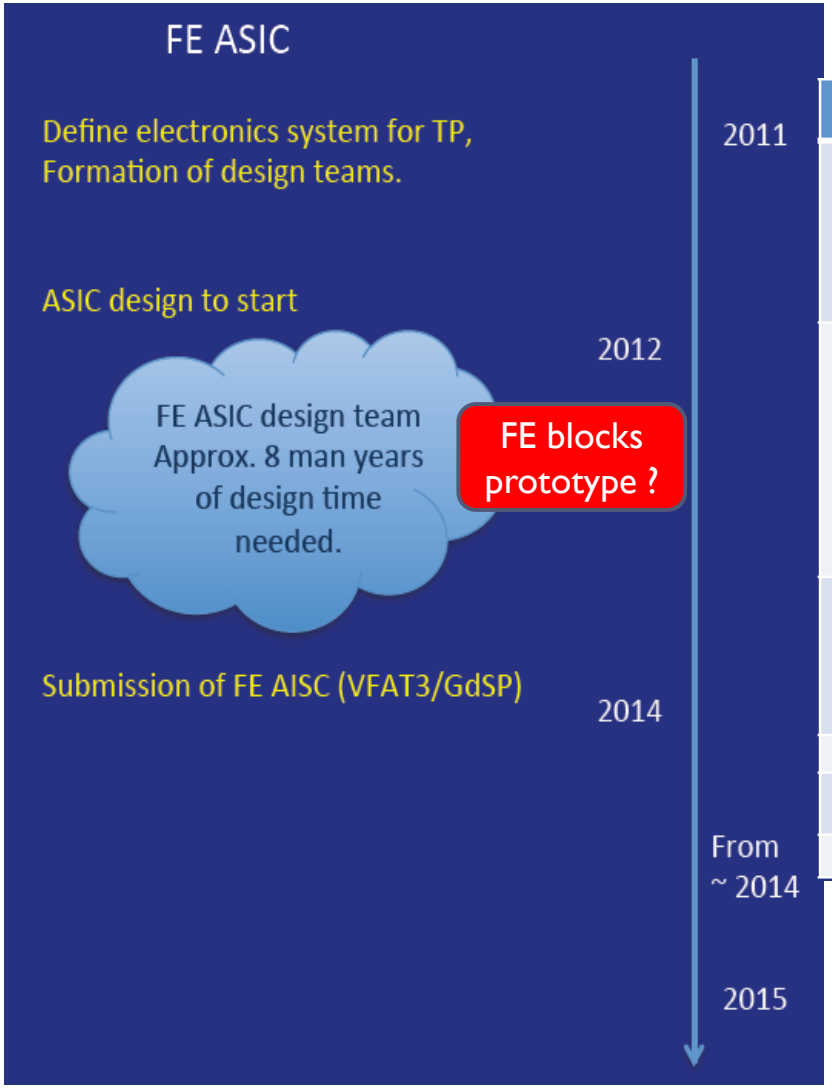
➔ Development ~ frozen during few months (simulations only):

➔ **decision now taken to go on with IBM 130nm.**

Microelectronics design

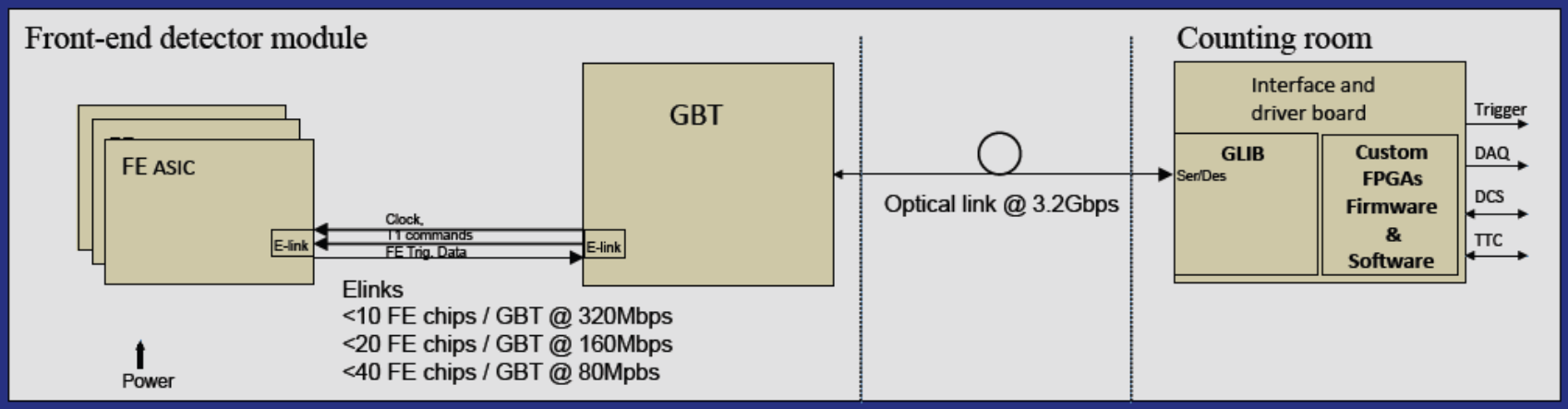


Schedule for GdSP electronics



	Main Tasks	Estimated man months
Phase 1 "Specification" We are still here	Technology Choice DSP functionality & simulation Identify IP components, vendors & collaborators Specification (memory sizes, data packet structure etc) Specification document Verilog high level simulation of full chip	2 6 1 3 4 6 (Sub total = 22)
Phase 2 "Module design"	Preamp + shaper Comparator + Sync ADC DSP CBM unit SRAMs Digital control GBT interface Verilog AMS modelling	6 4 2 6 4 4 6 4 6 (Sub total = 42)
Phase 3 "Full chip design"	Buy IP blocks if needed & simulate, DRC check Assembly of full chip Checking (DRC/LVS) of full chip Verilog and verilog AMS simulation of full chip MPW	2 6 4 6 1 (Sub Total = 19)
Phase 4 "Testing"	Testing	12
Sub total		95 (8 man years)
Phase 4 "Production"	Engineering run submission	9

E-Link + GBT =>LHC upgrade readout

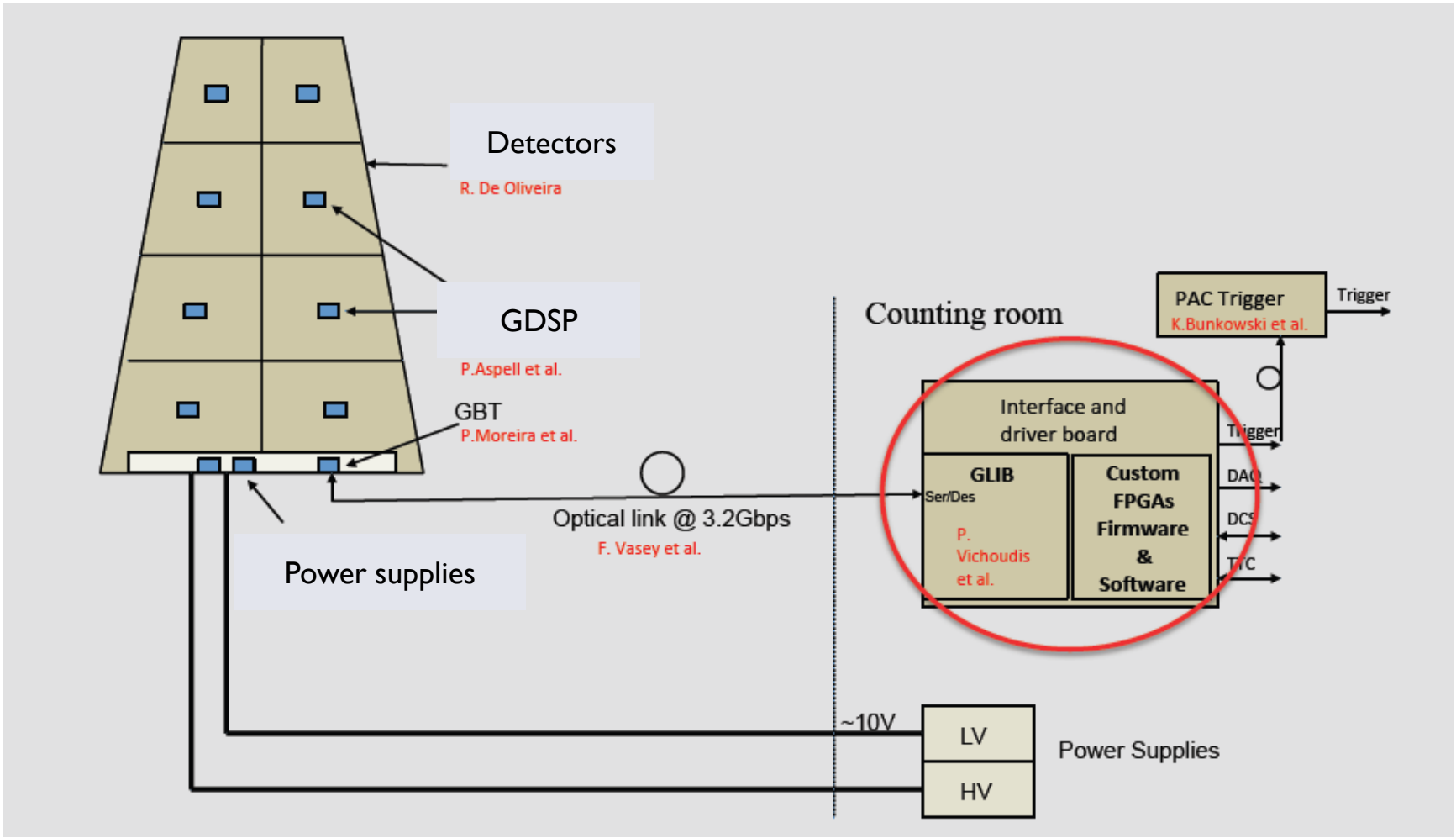


The GBT is currently foreseen for many LHC upgrades :
CMS tracker, HCAL, Atlas tracker, LHCb (all upgrades)

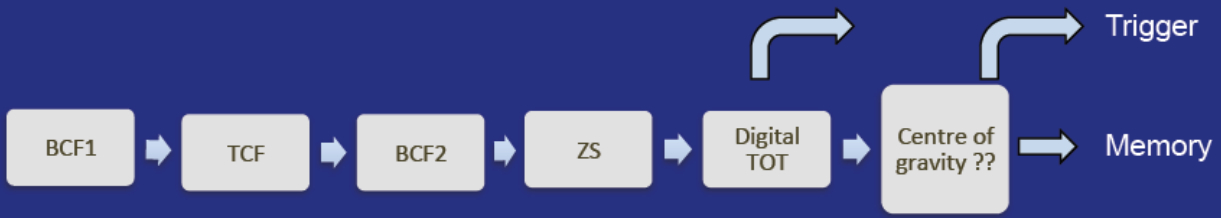
Generic projects in CERN for :

DC/DC Powering
GBT
Versatile Link
GLIB - Giga-Bit Link Interface Board

General RO architecture (SLHC type)



DSP part : what is required for CMS



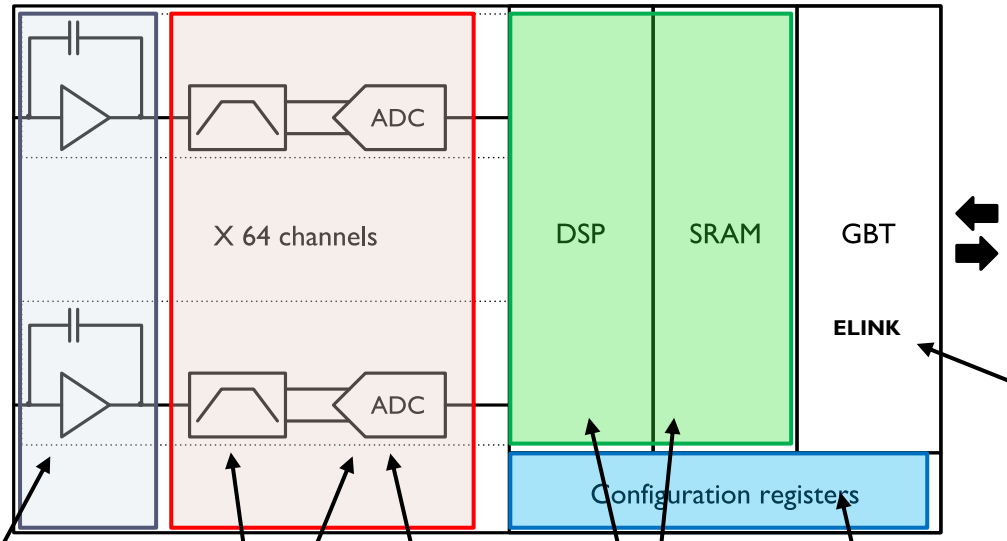
Trigger Processing latency

Not all stages are necessarily needed for all detectors.

Baseline correction 1	Removes systematic offsets that may have been introduced due to clock noise pickup etc. The SRAM is used for storage of baseline constants which can then be used a look-up table and subtracted from the signal.
Tail cancellation	Compensates the distortion of the signal shape due to undershoot.
Baseline correction 2	Reduces low frequency baseline movements based on a moving average filter.
Zero suppression	Removes samples that fall below a programmable threshold.
Digital TOT	To maintain accurate time resolution
Centre of gravity ??	Could be used to obtain a finer binary granularity. ?????

DSP part required for LCTPC still to be defined.
Larger memory, minimum treatment ?

Multiple domains Power Pulsing strategy



To be defined with GLINK group

Reduce current to a non zero value to keep a low impedance

Reduce current to 0. Keep vdd

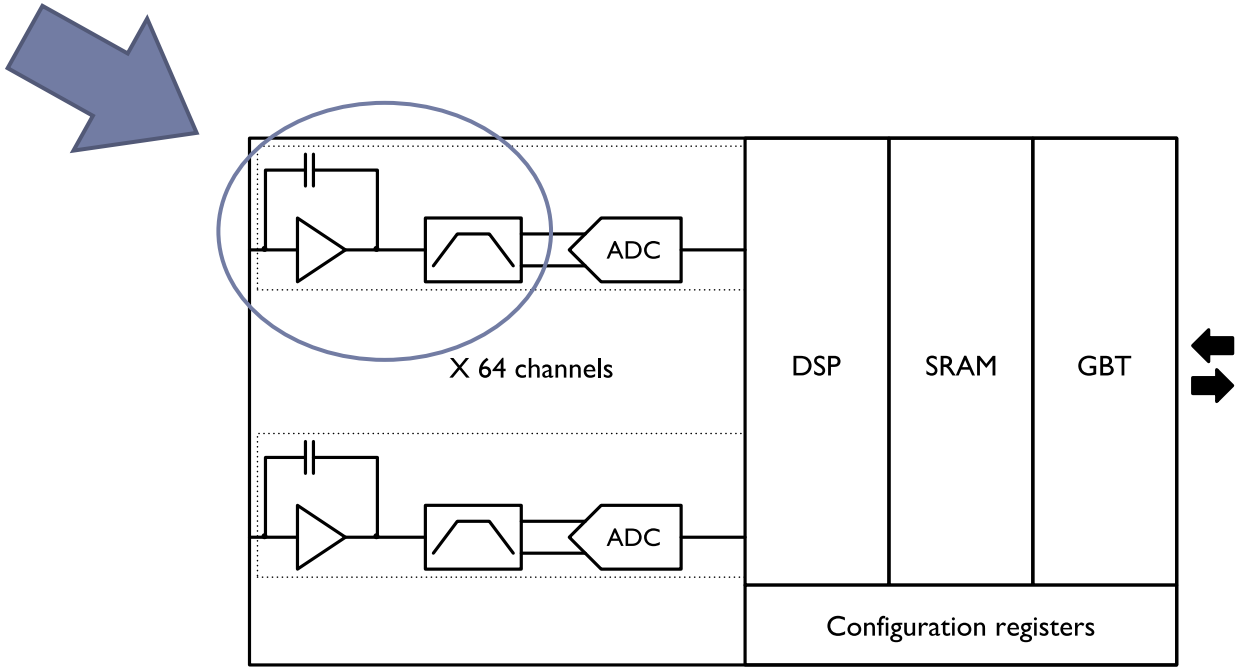
Stop ck

Reduce vdd to 0. Stop Ck.

Reduce vdd to reduce leakage while keeping the informations

GdSP ASIC

- Focus on front end



GdSP Front End specifications

- Technology :
  - CMOS 130nm ; Power supply 1.2V

From Paul Aspell

Parameter	VFAT2	SALTRO	VFAT3 / GdSP
Polarity	dual	dual	dual
Shaper peaking times (ns)	22	Programmable : 30, 60, 90, 120	Programmable : 25, 50, 100, 200, 400 ?, 600 ?
Gain (mV/fC)	60	Programmable : 12, 15, 19 & 27	Programmable: Values TBD

- Shaping times :
  - 25 ns ➔ Silicon Strip Detector (demanding for power)
  - 100 ns ➔ Gazeous Detector (optimum from our knowledge)
  - 500 ns ➔ Micromegas Detector with resistive layer (may be not necessary now)
  - Is it possible to reduce the set of shaping times by applying latter a digital filter to obtain longer shaping (yes according M. Dixit talk) ?
- (Shaper + Gain) programmable through slow control

GdSP Front End specifications

From Paul Aspell

Parameter	VFAT2 (IBM 0.25)	SALTRO (IBM 0.13)	VFAT3 / GdSP (IBM 0.13)
Linear range	+- 12fC	150fC	100fC, TBD
Input capacitance (pF)	20	0-20	15 – 20 – 30 – 60
Noise	~500e + 40-60e/pF @ 25ns	See previous talk	< SAltro /VFAT

Starting from data measured on ABCN (130nm design by Jan Kaplon for ATLAS SCT):

**** 800 e- @ 5pF, tp=22ns, 100µW***

**** assuming serie noise only***

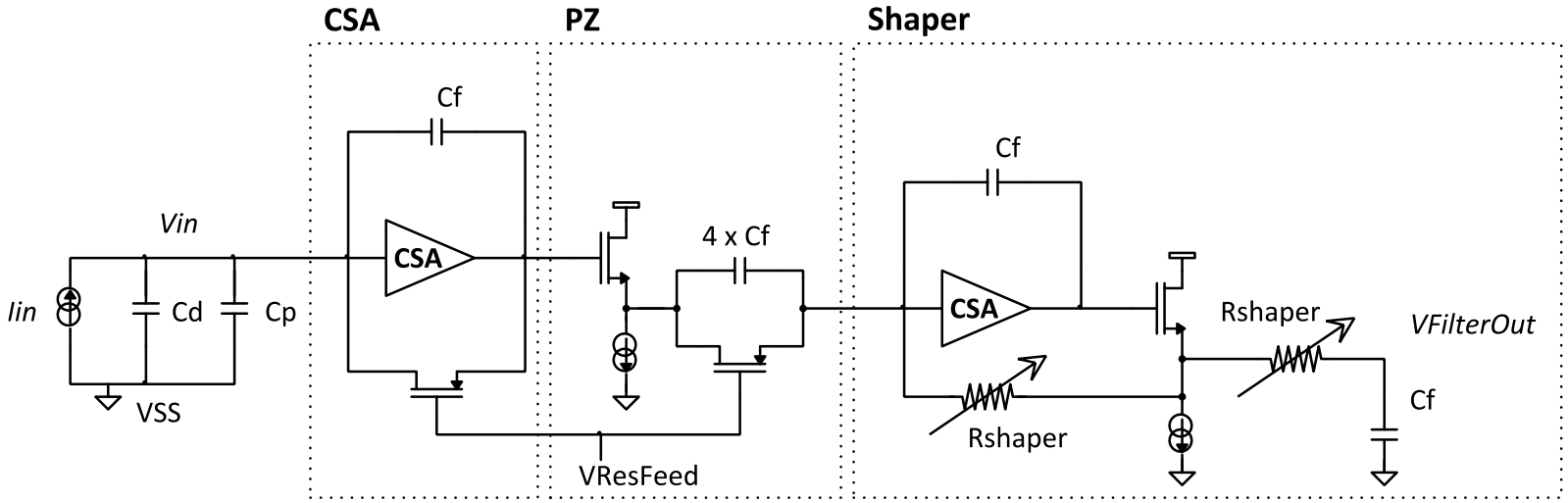
=> we can hope 530 e- @10pF, tp= 100ns, 200µW

=> Ultra Low power low noise design seems feasible

Parameter	VFAT2	SALTRO	VFAT3 / GdSP	This FE study
Power (mW/channel)	1.5 (IBM 250nm) (incl. comparator)	8	<< 1	< 0.24 (CSA only)

GdSP Front End:preamp pre-study

- Real pre-amp, real biasing, real shaper (still to be optimized).
- Preamp in CSA configuration (transimpedance should be optimized for a single Cin)
- Global Architecture not frozen yet
  - Two types of low frequency feedback + PZ cancellation schemes tested:
    - Current conveyor
    - MOS transistors

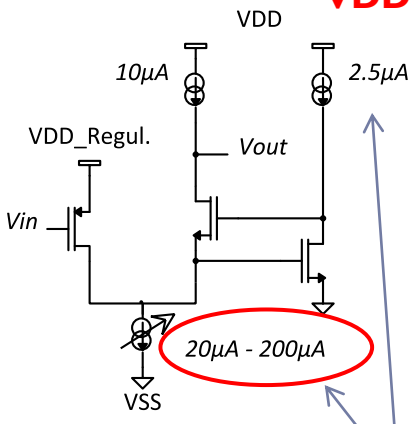


GdSP Preamp prelimiary study

- **CSA Structure: several architectures studied:**
  - Low gain from intrinsic transistor parameters
    - (1) Simple common source : G ~ 30dB
    - (2) Common source + cascode for the input : G ~ 39dB
    - (3) Common source + cascode for the input + cascode for the load : G ~ 47dB
    - (4) Common source + regulated cascode for the input + cascode for the load : G ~ 73dB
    - (5) Common source + regulated cascode for the input + regulated cascode for the load : G ~ 86dB
      (5) ➔ As in Jan Kaplon design

  - Chosen architecture : regulated folded cascode
    - Flexible architecture
    - Input transistor : weak inversion
      => At first order ENC proportional to $I^{-1/2}$
    - Gain – bandwidth – noise – power consumption tradeoff.

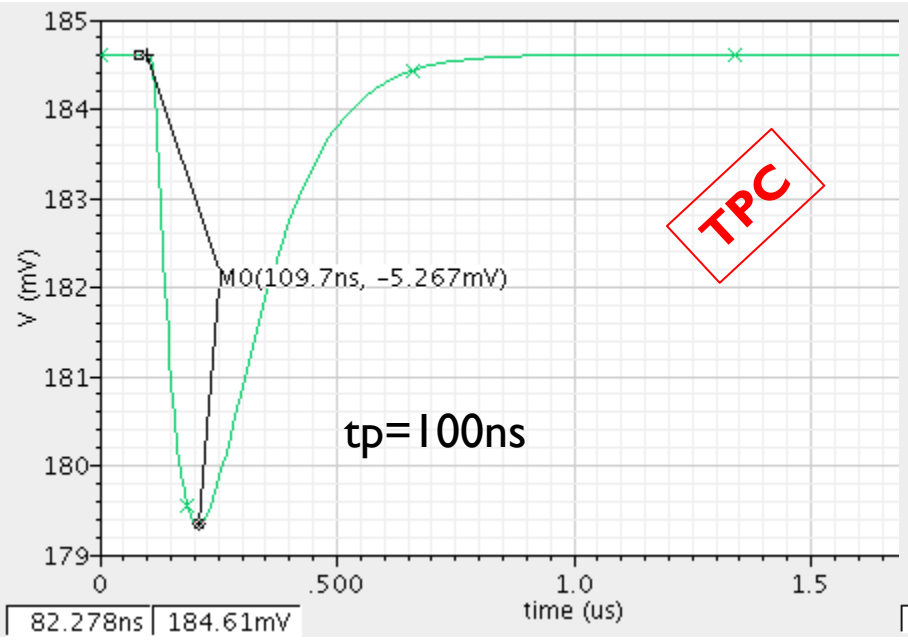
VDD =1.2V



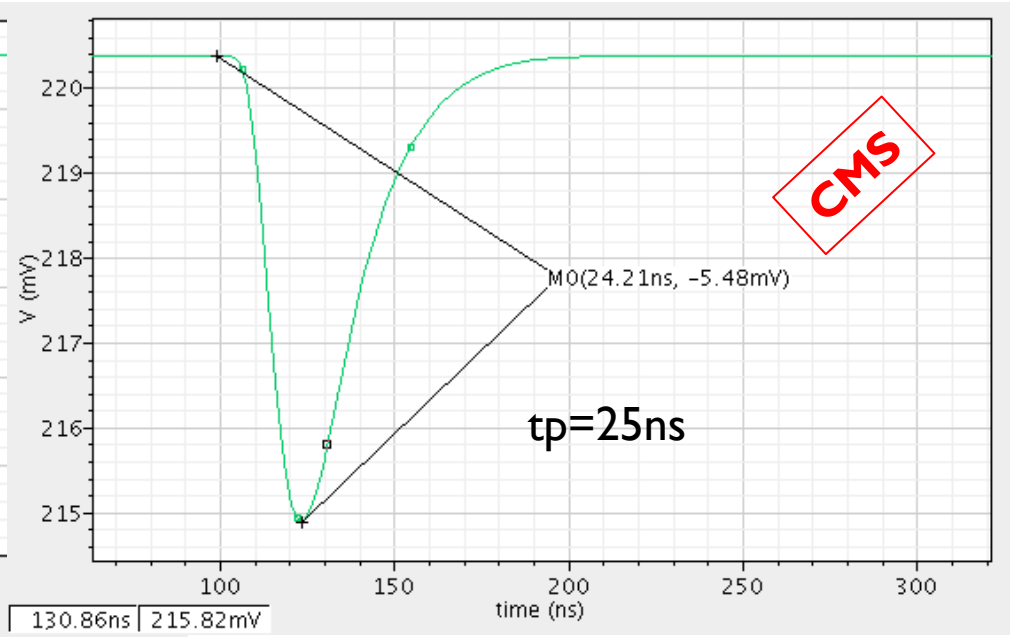
To multiply by 1.2 to obtain The CSA power consumption

GdSP Preliminay Front End study

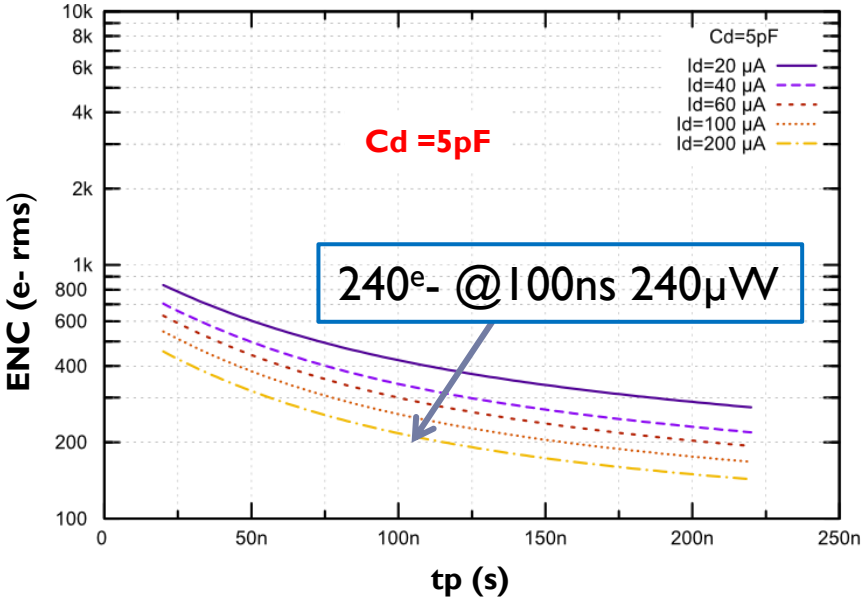
- Real pre-amp, real shaper, real biasing
  - Cd = 30pF
  - Cf = 200fF ; Rf ~50MΩ
  - Tp = 100ns
  - **Iin = 70µA => 90 µW**
  - ENC ~ 1330 e-

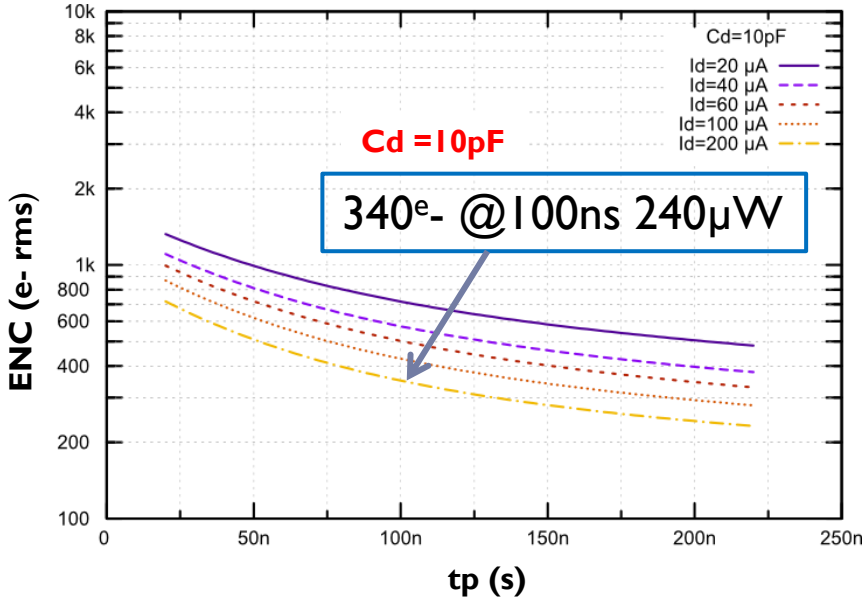


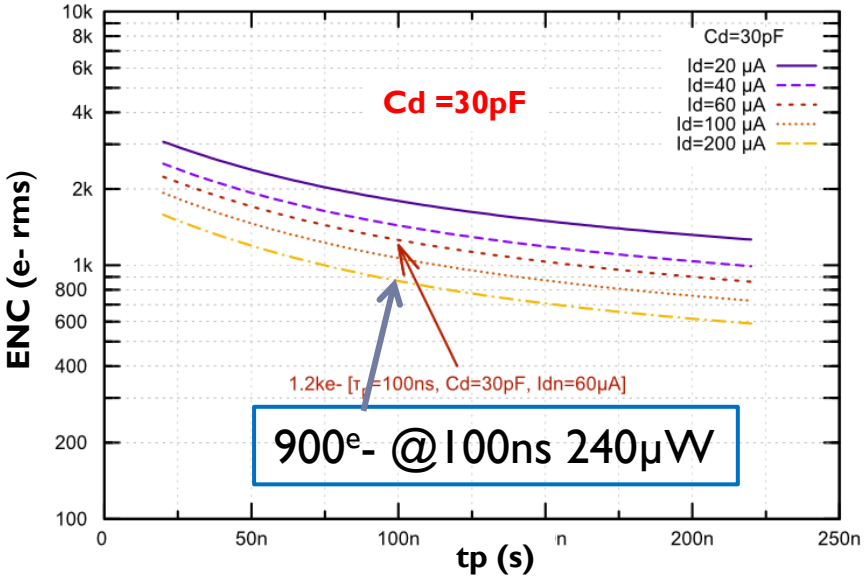
- Cd = 30pF
- Cf = 200fF ; Rf ~50MΩ
- Tp = 25ns
- **Iin = 200µA => 240µW**
- ENC ~ 2100 e-

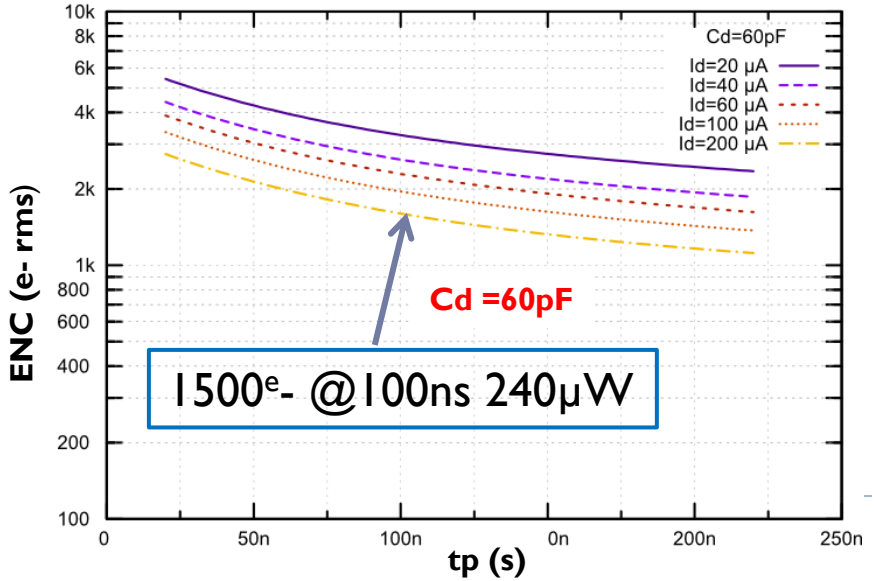


GdSP Preamp study ("Real" pre-amp, ideal shaper.)



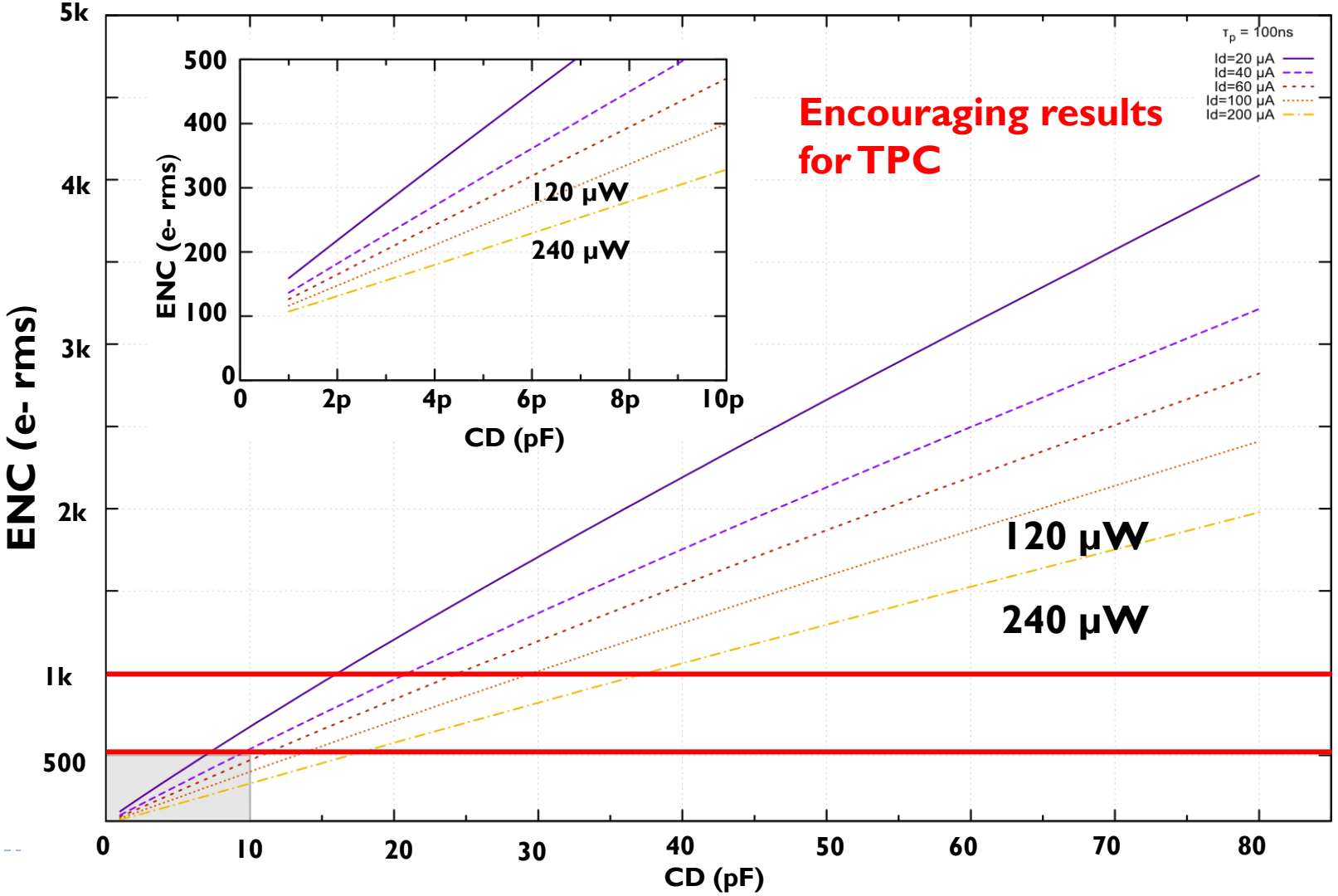






GdSP : preliminary simul of the preamp

- Simulation of pre-amp, ideal shaper (**tp=100ns**).

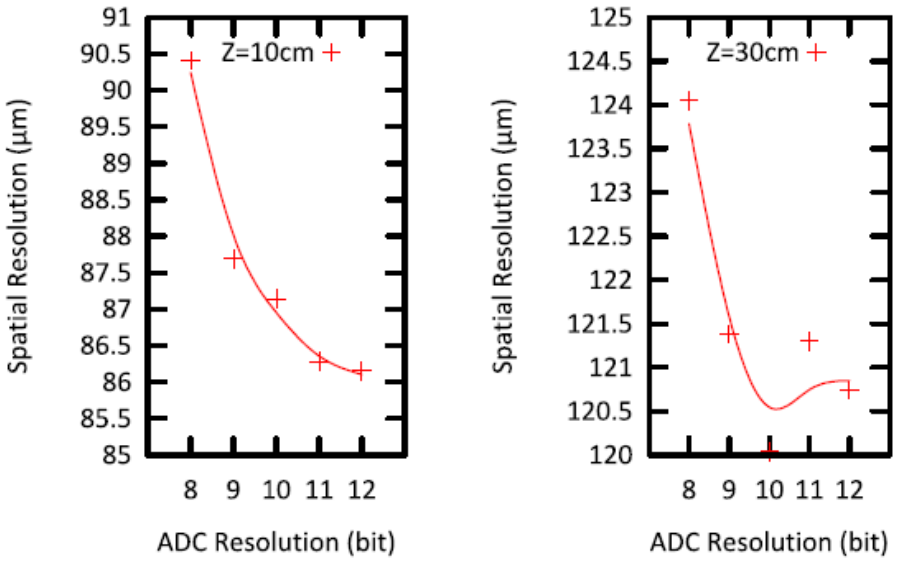


Question Marks about the ADC

- ADC frequency: power consumption scales as f: is 40 MSPS useful for LCTPC ?
- Nb of bits of the ADC: direct impact on
  - * power consumption (2^N)
  - * physical channel pitch => chip size => system integration
  - * size of the memories

Provocative question: are 10 bits really necessary ?

Degradation of spatial resolution if nb of bits <9 (from Micromégas Data with AFTER)



Conclusions & near future

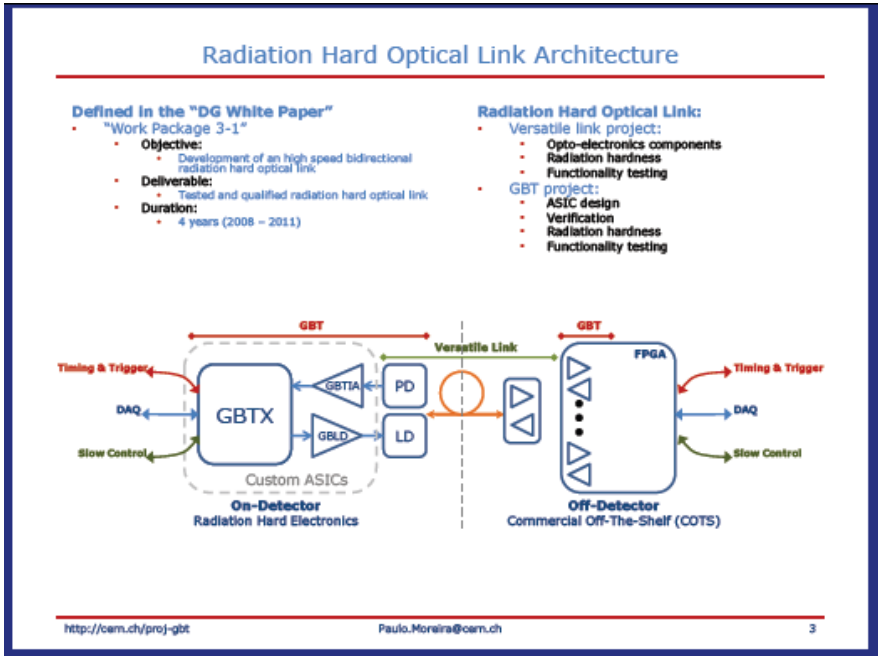
- A GDSP design common for CMS and LCTPC is seriously considered.
- Some blocks are already being studied, other not.
- A low noise front-end part seems to be designed for a power significantly lower than in PASA/SALTRO.
- First real design meeting: 15-18th may @ CERN.
- For this date: need to define specifications (TPC oriented, which will be merged with those from CMS) at least for the front-end :

Specifications (TPC mode)	My proposal
Peaking time after shaping	50ns,100ns,200ns
Range(s)	100fC, 200fC
Linearity	5%
Range for input capcitances	2 - 30 pF
Xtalk	<2 %

Suggestions for specs are welcome: send me an email (eric.delagnes@cea.fr)

Spare Slides

GBT +elink



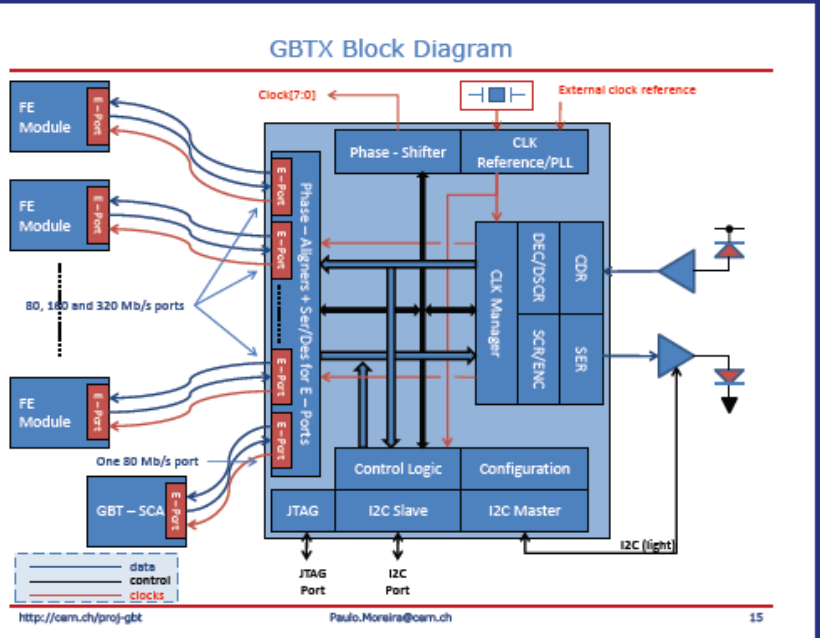
	Voltage (V)	Power (mW)
GBTIA	2.5	250
GBTX	1.5	1414
GBLD	2.5	400-500

Source : P. Moreira et al.

http://cern.ch/proj-gbt

Enables bi-directional optical communication between multiple FE chips and the counting room.

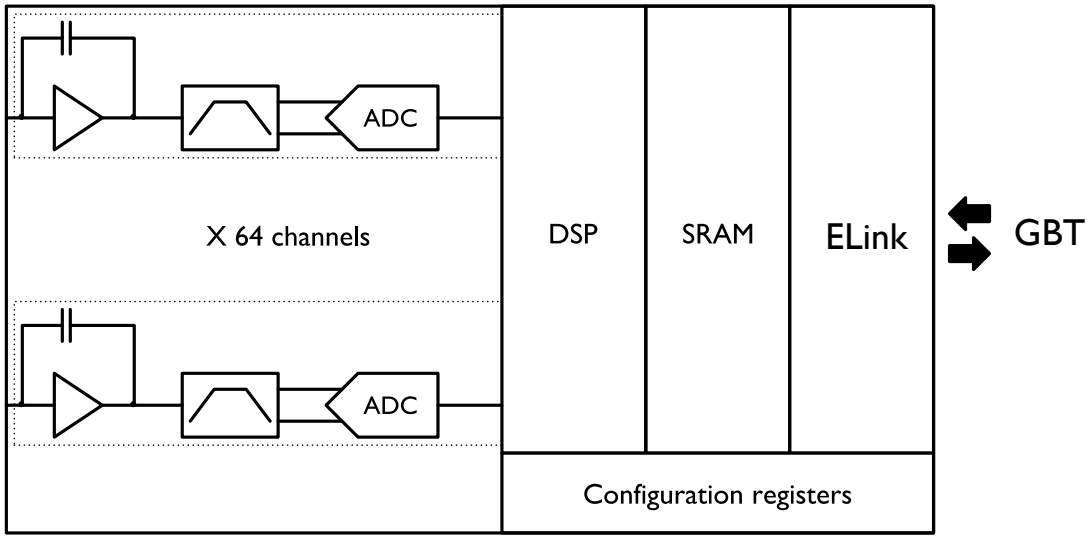
Max. number of FE chips / GBT	Bandwidth available per FE chip
10	320
20	160
40	80



GdSP ASIC

- Readout circuit for TPC
- Architecture based on SALTRO16 ASIC
  - Pre-amp / Shaper front end
  - Analogue to Digital Converter
  - Digital Signal Processing
  - Static Random Access Memory
  - *New interface :* GBT - E-link

developed by CERN



- Design optimization
  - Keep main specifications of SALTRO16 + extend capability on fast signal (cf. next slides)
  - Low power consumption driven design !