Minutes of WP-meeting 147

Attendance:
DESY: Leif Jönsson, Volker Prahl, Stefano Caiazza, Ralf Diener
Phone: Jan Timmermans, Ron Settles, Takeshi Matsuda, Fabrice Guilloux, Eric Delange, Lund, Jochen Kaminski

PCMAG/LP setup, test beam:
Ralf: - PCMAG arrived at DESY right after the collaboration meeting.
- The installation (cooling water pipes and electrical cables for the cooling compressors) are installed up to the beam area. The final meters into the beam area can only be completed during the next test beam shutdown in May.
- The lifting stage is quasi finished, only a few details are missing, but will be completed in time.
- There is a small change in the schedule: The two experts from KEK, Makita san and Kawai san, will arrive one week later and stay from the 19th of April to the 21st of April. In this time the box of PCMAG will be opened and the magnet will be inspected, whether any damaged occurred during the transport. Besides, the further schedule will be discussed.
- The setup will be done by the DESY-group after the meeting: The PCMAG will be placed in the lifting stage and connections prepared.

Takeshi: - Two young people who worked on PCMAG at Toshiba will arrive at DESY on May 20th to set up the cooling compressors. At the end of May the cooling will start, at the beginning of June the first excitation should take place. Then, they will do some tests and adjustments (resistors,..) and will finish mid of June, the latest end of June.

Ralf: - Investigation of the field cage still has to be done. Sparking of the ring close to the anode has to be studied. One of the HV-cables is, however, damaged and has to be replaced.
- Bernd realized that one of the dummy modules had no O-ring.

News from the groups:
Takeshi: He is investigating a modification of the SciEnergy GEMs. He has a new idea of placing the resistor on the GEMs. This idea will be tested at the beginning of May.

Discussion on electronics:
Leif: -Following the initial discussion during the collaboration meeting Leif, Takeshi, Stefano, Ulf and Akira discussed the mounting of the new MCM and BC for the SALTRO-16 chip.
A horizontal mounting of the MCM on the padplane would be preferable, since it is closer to the final solution and more appropriate for testing the final cooling system. Pads would have to be somewhat larger than in the current layout, since the maximum number of pads per padplane would be around 3456 instead of 5152. But if smaller pads should be necessary, the current PASA/ALTRO-based electronics could be used. Some question are still open:
i) How the cooling could be made. Currently, the proposal is that there are three layers of cooling plates, between the pad plane and the MCM-boards, between the MCM-boards and the Board controller-boards, between the BC-boards and the voltage regulators. The layers could be metallic sheets with openings for the connectors. The cooling pipes could be connected to these sheets.
ii) Between MCM and BC 2 64-pin connectors have to be placed. Currently connectors with a height of 1.5 mm are planned, which is too thin for cooling pipes. → Searching for higher ones. A 60 pin-connector with a height of 3 mm could be used, if some some pins are identified as irrelevant for standard operation (test pins).
iii) connection between BC and MCM has to be thought about: Kapton cable?

iv) pick up of noise/cross talk
v) grounding
vi) voltage regulation: How to bring voltage from one board to another.
vii) High speed connection to PC... A small FPGA exists, which could be fixed on the BC-board and works in the Gbit/s-region. It remains to be verified, if it can communicate with possible receivers such as the SRU of RD51 which works at a lower rate (input up to 200 Mbit/s, output 10 Gbits/s).

Takeshi: - He suggests to introduce a thermal conductor plane between padplane and MCM and/or MCM and BC to facilitate cooling. Copper would be the easiest choice, but has a very high material budget. There are better material:
Carbon-carbon plates (better thermal conductivity than copper)
TPG (a graphite) this is very fragile and is usually used in a sandwich structure with a metal plate. As a base material either Cu or Al is used. This material has a thermal conductivity 3 times higher than copper, but is lighter than aluminum. Further information could be gathered from the ATLAS-collaboration which is already using it. But also simulations are needed. In particular, the connection between the pipes and this plane has to be studied. Possibly the pipe could be made inside the plane.

For the current setup (LP) a copper plate should be used with temperature sensors connected to it, to study the temperature development. The cooling will be done with air.
Takeshi has placed some additional information and drawing on the indico page.

Eric and Fabrice summarized the status on GdSP again: Since LCTPC has currently neither the financial support nor the manpower to develop a readout chip on its own, it would be a practical approach to join with CMS. CMS needs a new chip for its muon-detector upgrade with GEM trackers. The rough timeline starts in 2 weeks, when CMS will give state its requirements on the chip. Within 2 years the individual parts of the detector (Font-End, DSP, ADC, ...) will be developed and tested on small test chips and then put together. To accomplish this, first test should start end of this year (September/October). Therefore, LCTPC should also state its requirements in a few weeks/months time. Important is:
Gain, number of bits of ADC, dynamic range, digitization frequency, input capacitance, rise time, shaping time.
The default values are: input capacitance = 30 pF, 10-bit ADC, 120 ns shaping time, 40 MHz readout frequency.

These, figures of merit were discussed in the following:
shaping time: Leif has done already some measurements (s. slides collaboration meeting) of the longitudinal spatial resolution depending on drift distance and shaping time. It seems that a shaping time of 60 ns gives the best results with the ALTRO-electronics (20 MHz). But Leif would like to redo the measurements for the full drift distance of the LP, since he could use only the data for the first 30 cm. Eric explains, that a faster shaping time will increase the power consumption of the chip a lot. A programmable shaping time like in the ALTRO will be implemented to gives the highest degree of flexibility. However, the designers still need 1 or 2 target operation points, for which they optimize the circuit. The general feeling tends towards a value between 50ns and 100ns.
CMS is likely to require a short shaping time, since they also want to use the signal for the trigger.
Bits of ADC: Eric and Fabrice explain that a lower number of bits would be appreciable, since 12 bits

is very difficult to implement, 10-11 bits need expertize, but is doable, whereas 8-9 bits is very easy. So, a lower number of bits would make the design considerably easier. For comparison, ALEPH had 8 bits, the ALTRO-electronics 10 bits and CMS will require only 5 bits. Leif did some charge measurements in Lund, in which he demonstrated, that a 7 bit ADC would be sufficient to do the dE/dx measurement. Stefano asked about the pedestal: the current ALTRO has 1024 counts, but a pedestal at ~100-200 counts leaving only 800-900 counts as a usable range. Eric and Fabrice confirmed, that the the ratio would roughly be the same, that is that the pedestal would be at about 10-20 % of the full range.
It was suggested, that one should look at old ALTRO-data and artificially decrease the number of bits to study the effect on charge and spatial resolution. The requirements (both shaping time and ADC-bits) for a Micromegas-module were unknown. Also, it was unknown if these parameters could be varied in the AFTER-electronics. Therefore, it was felt, that it would be helpful to try to connect a Micromegas module to the ALTRO-electronics and study the signals with the same readout electronics as the GEM-modules (in particular change the shaping time).
Readout-link: The first version of the GDSP is likely to be for CMS and the data transfer from chip to later readout-electronics (e.g. FPGA) could be done via an elink connection (a serial 250 MBits/s link) to a GBT-link, which is a 3.2 GBit/s serial link based on an optical fiber. This is a new radiation hard standard at CERN for reading out ASICs. It requires only a small pad on the ASIC. The layout can be copied from CERN-libraries and is therefore easy to implement.