

Hardware Architecture of LLRF System

The amplitude and phase stability requirements for the LLRF at ILC are 0.07% and 0.24°, respectively, as summarized in [Table 3.6.1](#). In order to satisfy these requirements, a digital feedback system is adopted. This digital system is used in FLASH [a], STF [b] and NML [c] and will be installed in XFEL [d]. In order to reduce the digital processing time, a field-programmable gate array (FPGA) is adopted for the digital signal processor.

The RF probe signals from cavities are down-converted to an intermediate frequency (IF) by down-converters. The IF signals are directly acquired by the ADCs. After feedback processing occurs inside the FPGA, the DACs drive the up-converter. The RF output is amplified by a klystron and drive cavities. The forward and reflected power signals are also processed for automated control of the resonant frequencies of the cavities. The resonant frequency controller drives slow motor-controlled tuners and fast piezoelectric actuators 30 channel DAC boards. An FPGA board with 30 ADCs and at-least two DACs will be used in the baseline configuration, which is the same as that for RDR. In total, three boards will be installed at each 26 cavities; the first will be used for cavity probes, and the second and third will be used for RF inputs and reflections, respectively.

The distributed LLRF system will be adopted in XFEL, where each FPGA calculates the local vector sum of 12 cavities, and the total vector sum (24 cavities) is summarized at the primary controller [d]. Distributed klystron scheme (DKS) will also adopt this llrf scheme especially for the future upgradability.

The IF mixture method has been demonstrated in STF [b]. The number of ADCs can be reduced to be 1/4 by combining the four intermediate frequency (IF) signals. This IF-mixture method can be used for an alternative digital LLRF system at DKS.

The digital LLRF system communicates with the servers via a Giga-bit Ethernet and the waveform data can be used for diagnostics such as quench detection and detuning control. Typical parameters for the ADCs and DACs are sample rates of ~100 MHz and 14–16-bit resolution. FPGAs with several million gates, including many fast multipliers are available. More complex algorithms can be implemented on slower digital signal processors (DSPs) or on software CPU inside an FPGA.

A down-converter module translates the 1.3GHz RF cavity probe signal to the IF by using local oscillator (LO) signals. The down-converter can be a source of degradation of the overall performance. The down-converter and LO should be carefully designed to have lower phase noise, non-linearity and thermal dependency.

The up-converter module translates a digitally generated IF signal back to the RF in a process similar to that of the down-converter. The stability issues are considerably fewer for the up-converter as this module is within the feedback loop.

Resonance control is accomplished via a fast piezoelectric actuator and slow motor-driven tuner. The resonance controller measures the frequency error of the cavity during and after the flattop. This error can be reduced by suitable excitation of the piezoelectric actuator.

The motor-driven tuner is only used to correct for long-term drifts.

The LLRF station must interface with the high level RF; beam transfer control; machine protection; sector, global energy and phase regulation; and control system. A control system IOC is built into the LLRF system to handle parameter and data collection.

Table 3.6.1.

Errors	Phase tolerance limiting luminosity loss (deg)	Phase tol. limiting increase in energy spread (deg)	Amplitude tolerance limiting luminosity loss (%)	Amplitude tolerance limiting increase in energy spread (%)
Uncorrelated BC phase	0.24	0.35		
Correlated BC phase	0.48	0.59		
Correlated BC amplitude			0.5	1.8
Uncorrelated BCamp.			1.6	2.8
Correlated linac phase	large	0.36		
Uncorrelated linac phase	large	5.6		
Correlated linac amplitude			large	0.07
Uncorr. linac amplitude			large	1.05

Summary of tolerances for phase and amplitude control. These tolerances limit the average luminosity loss to <2% and limit the increase in RMS center-of-mass energy spread to <10% of the nominal energy spread.

LLRF control for DKS

The schematic layout of the DKS LLRF system is shown in Fig. 5.3.1. LLRF controllers are located at every 26 cavities for future upgradability. This configuration is as same as the RDR and KCS. Since 1.5 RDR unit corresponds to one DKS unit, both primary llrf controller (pick up 26 cavities) and secondary controller are used. The secondary llrf controller pick-ups total 26 cavities and send the partial vector sum of each 13 cavities to adjacent primary controllers. Primary llrf control rack includes down-converters, clock distribution, timing receiver and a upconverter. Secondary llrf control rack is almost same as the primary but no upconverter. The number of components is summarized in Table 5.3.1.

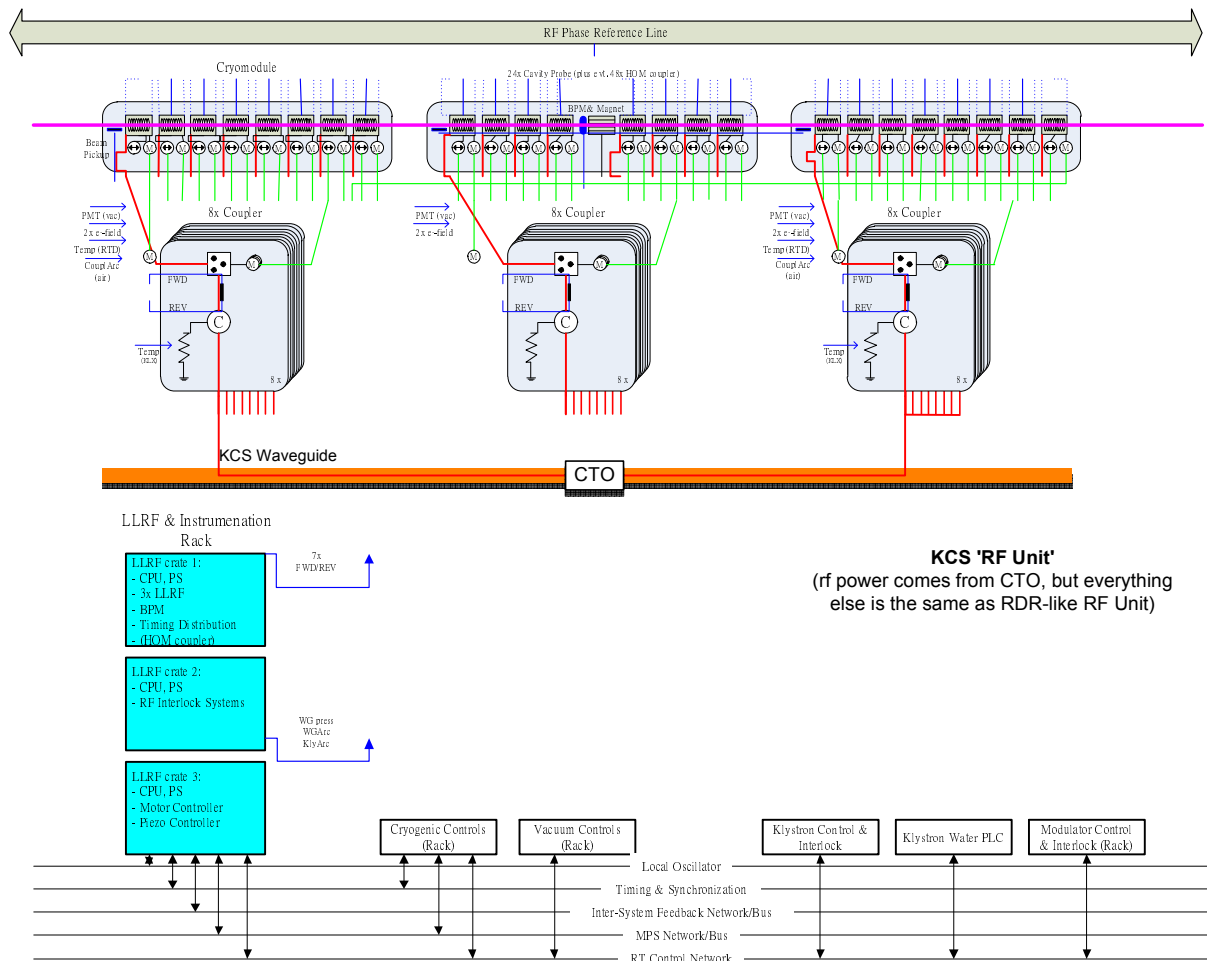


Fig. 5.3.1 Schematic of DKS rf unit. Total 39 cavity pick-ups are connected to primary (26 cavities) and slave (13 cavities) controllers.

Table 5.3.1. Number of llrf components at DKS

Components	per 26 cavities	per DKS unit
Downconverter	90	135
Vector modulator	2/3	1
30-Channel LLRF Board	3	4.5
30-Channel DAC Board	3	4.5
Clock Generator & Distribution	1	1.5
Timing Receiver	1	1.5