Plans for Timepix module

Towards a 100 chip module

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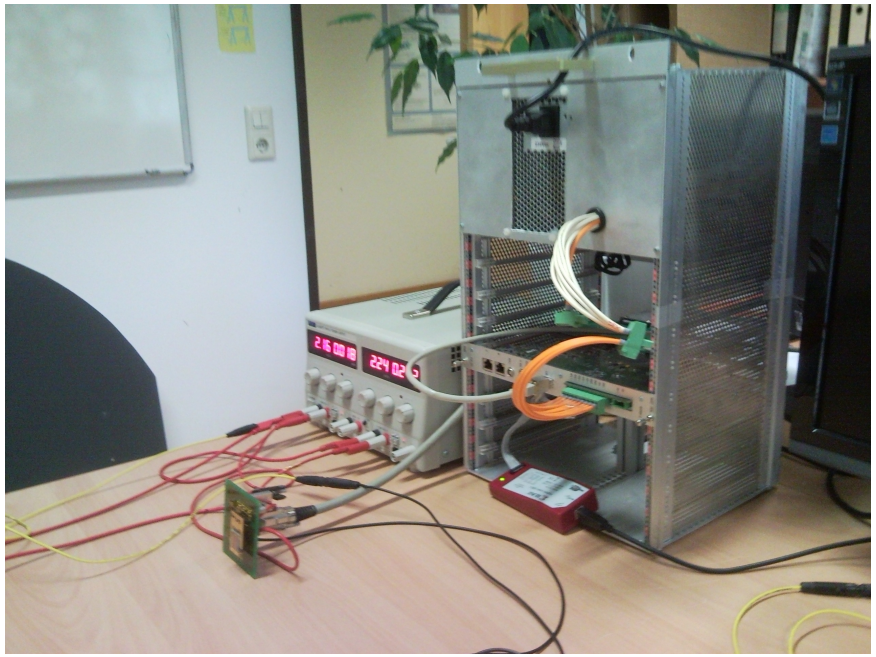
Status Timepix+SRS Readout

- Most of the functionality of the Muros+Pixelman system is implemented
  - Set matrix and DACs (FSR)
  - Read out matrix
  - Reset, start/stop measurement, measure with certain shutter length
  - DAC scan in Software + osci (no ADC jet)
  - Threshold equalisation
- Setup with one chip in operation



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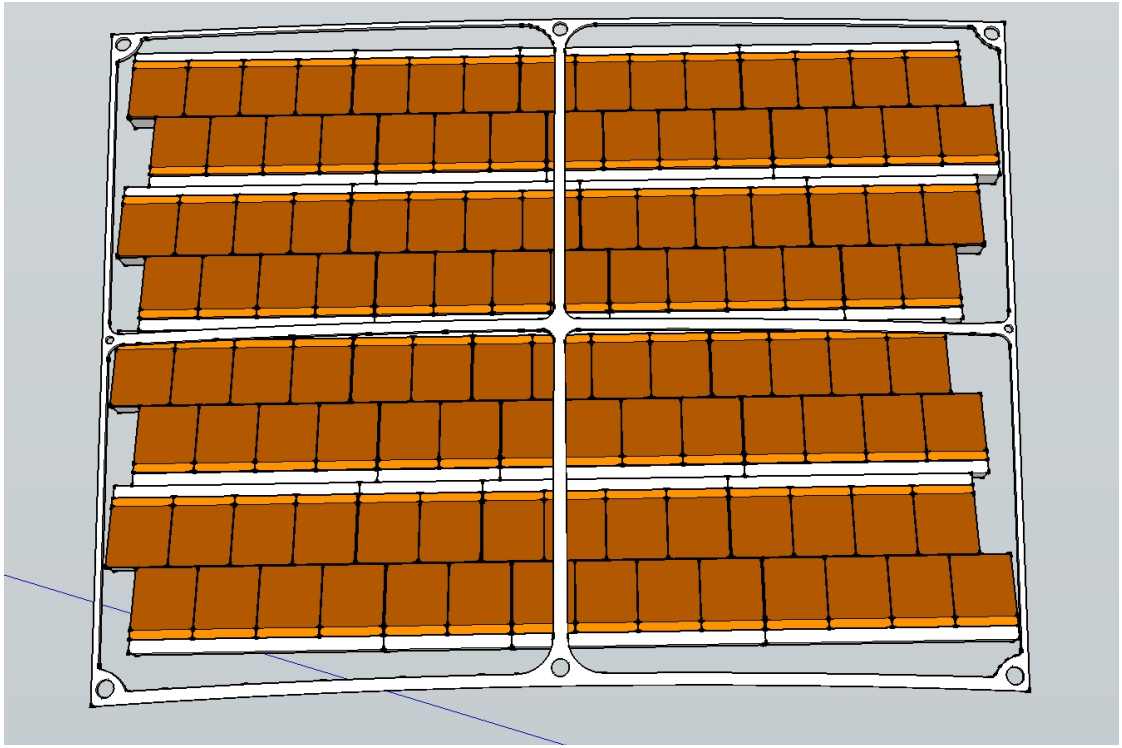
Outlook

- Far goal 1: LCTPC module with InGrids
  - Maybe later...
- Far goal 2: LCTPC module with DESY GEM and as many Timepix chips as possible (115 chips, staggerd chips), consisting of 16 submodules (different sizes, most of them octoboards)
  - Still to many problems to solve for a first try...



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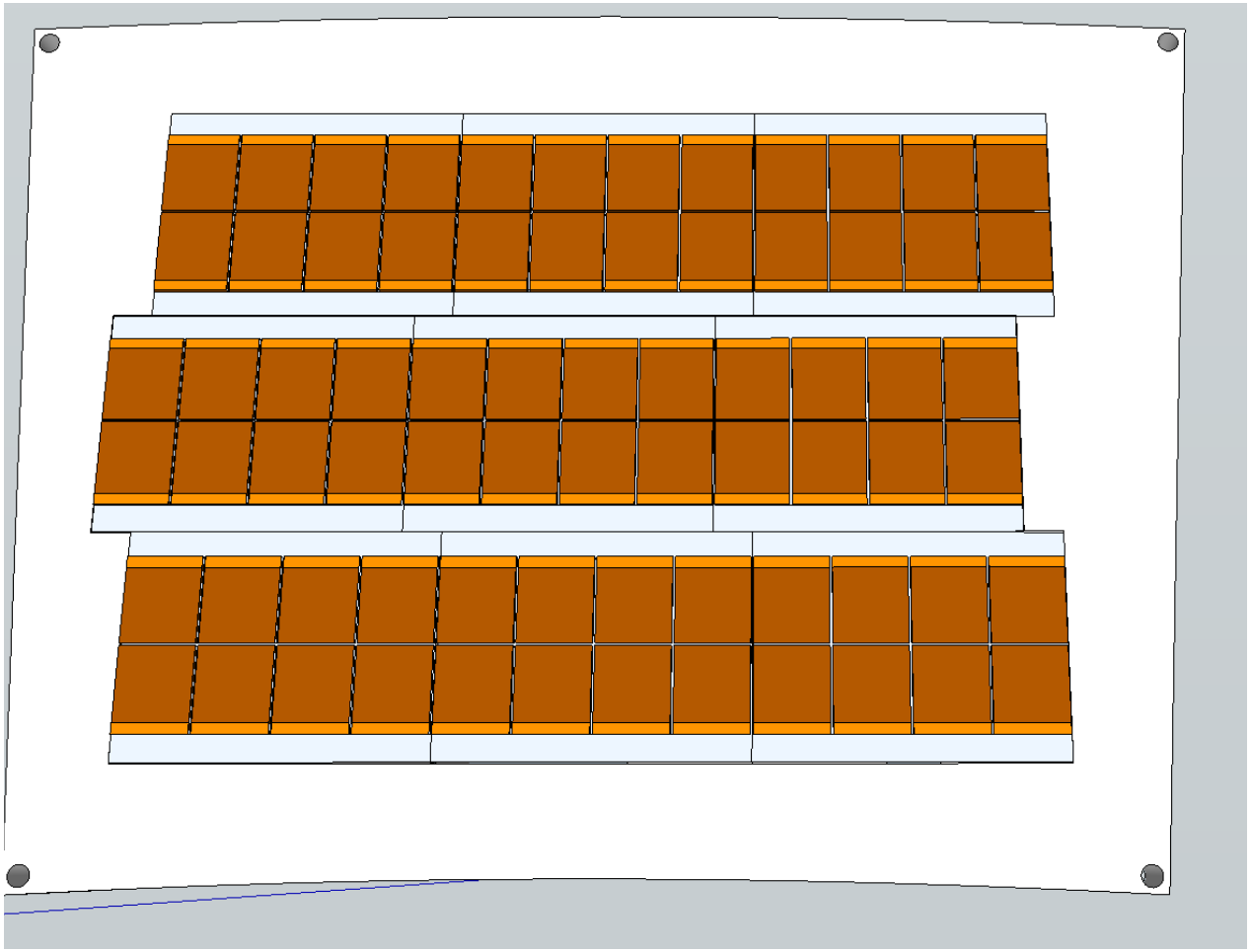
Next steps

- Near goal: LCTPC module with 3x3 submodules, each octoboards, staggered boards



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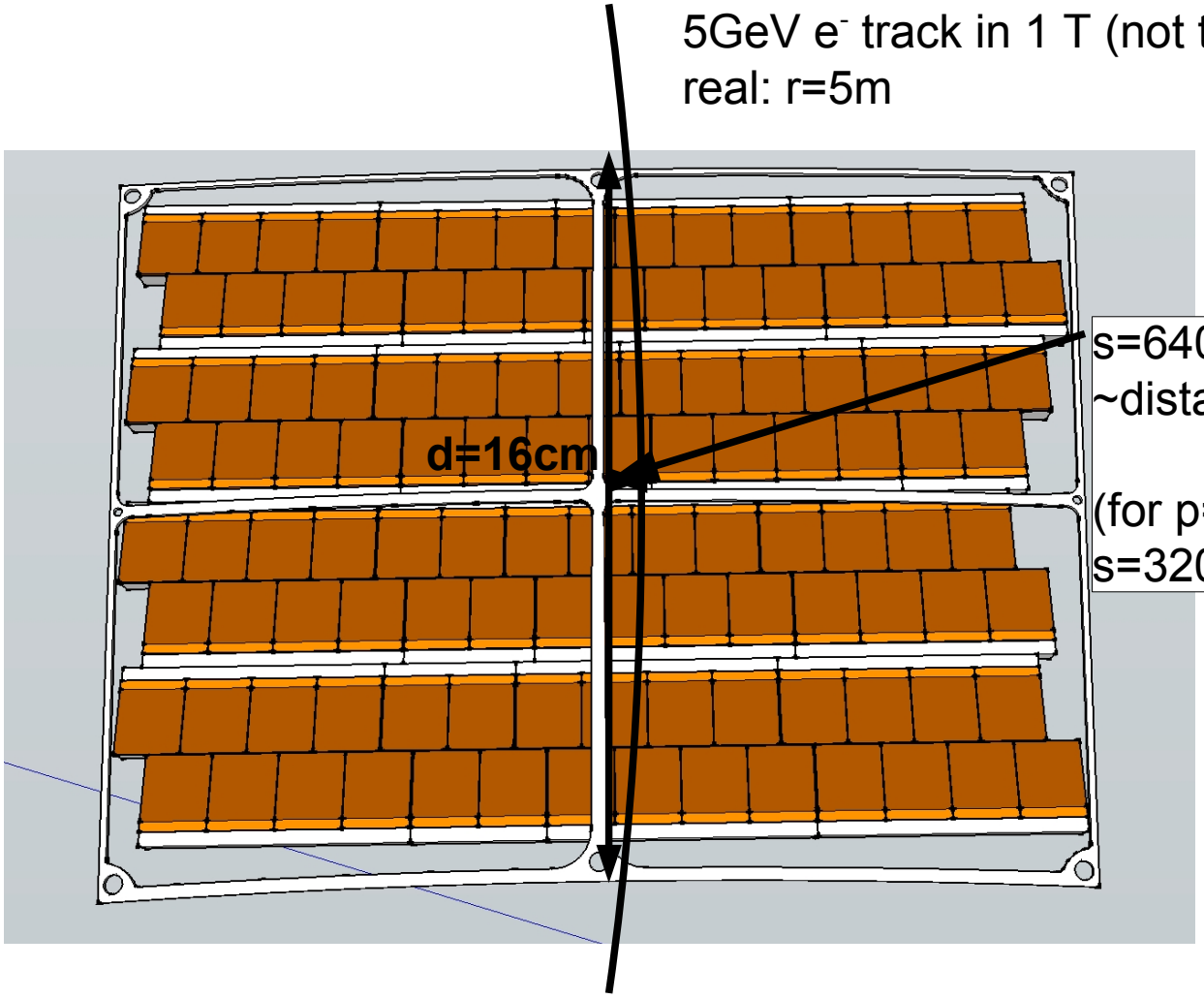
Why stagger chips?



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Steps to reach near goal

- 1 chip readout by SRS using HDMI cables, electronics as for 9 octoboard
  - Think about signalling → use I2C, CMOS → LVDS
  - Think about power supply → use power regulators on intermediate board, see if current (~8A/octoboard) can come through HDMI as in SRS+APV25
  - Think about cooling → water for the beginning
  - Design intermediate board and adapter card for SRS
- Construct mechanics (frame hosting octoboards, including cooling)
  - Test alignment of submodules
  - Test cooling → first put resistors instead of chips

Done

first idea

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first idea

Help, opinions, advice and experience welcome

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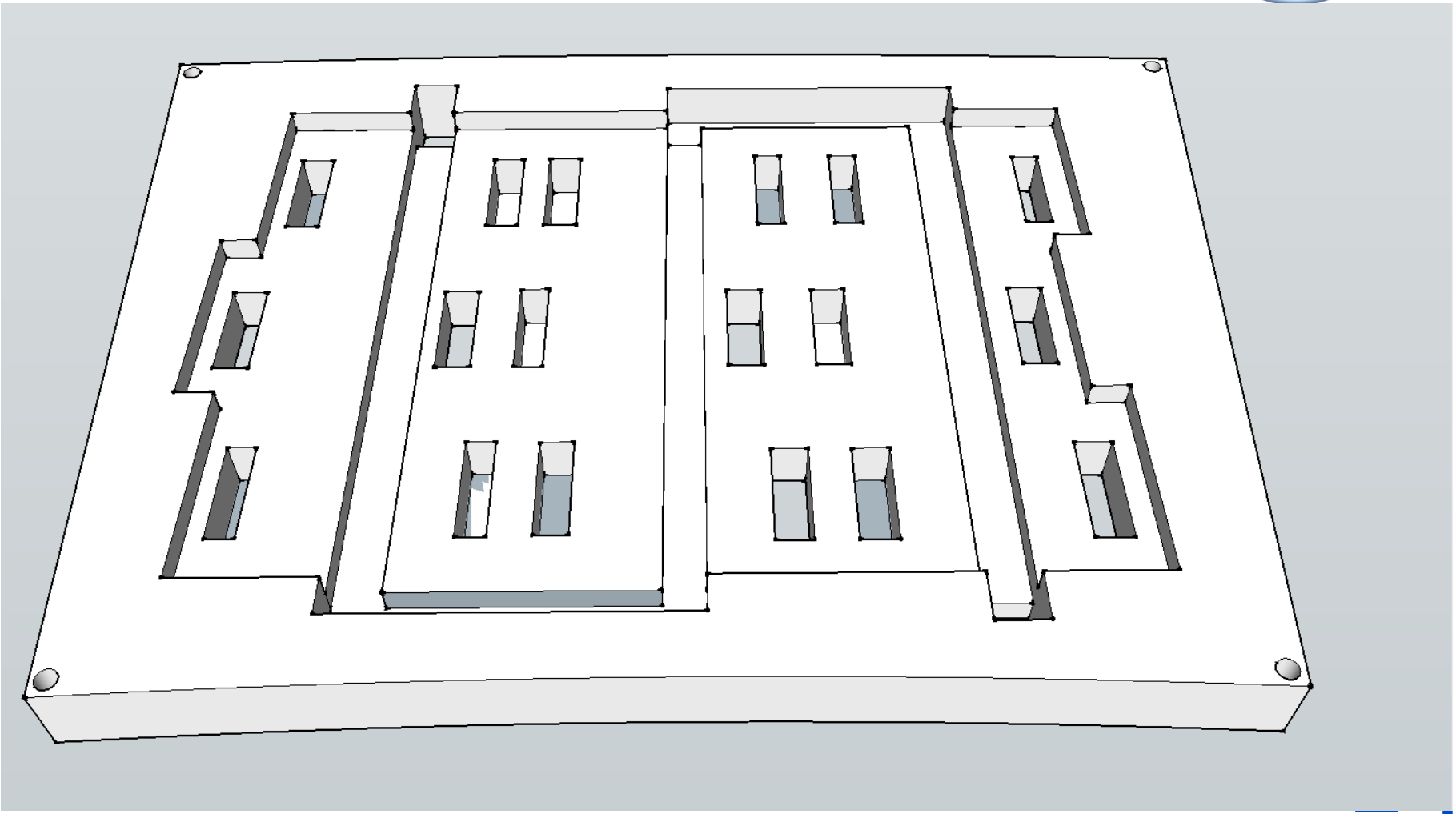
Endplate mechanics



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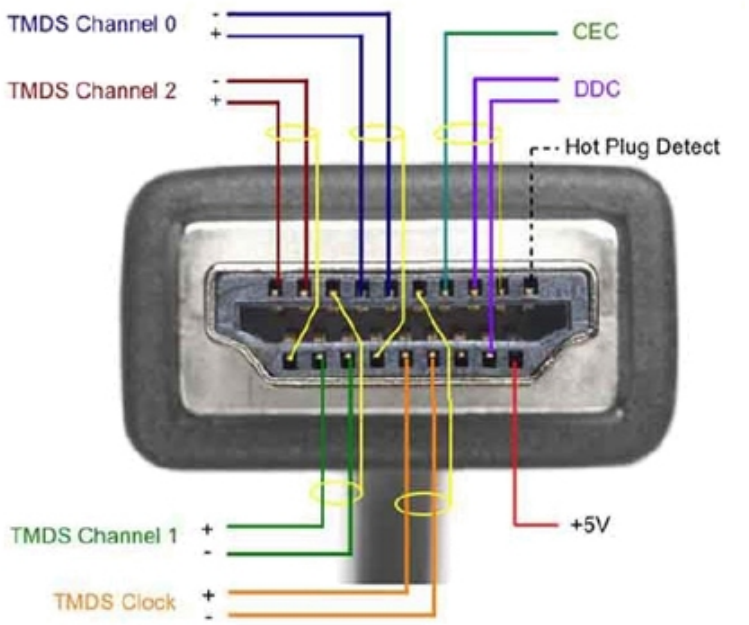
Backup: HDMI Cables

- 2 cables per ocotoboard
- 6 of 8 differential pairs for clock, data and enable (in and out)
- 2 other for shutter (in and out)
- 2 DDC on one cable: I2C
- 2 DDC on other cable: LVDS converted ANIN_N04
- 8 lines left for polatrity, Tpules_enable, power, ground



14 lines + 5 shields per cable
- 3 diff signals
- 1 diff clock
- 2 DDC (I2C SDA and SCL)
- 1 CEC
- 1 „Hot Plug detect“
- 1 5V
- 1 not specified

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Backup: signalling

- Floorplan for signalling
  - 4 Octoboards on 1 FEC
  - LVDS/CMOS drivers missing in sketch
  - DAC_out → ADC → I2C
  - Ext_DAC_in controlled by I2C DAC
  - M0,M1,TReset from I2C
  - Global part: Shutter, Polarity, Tpules_enable for whole interm. board
    - Shutter also possible to inject on intermediate board
    - Should go in both directions
    - Test pulse generation on intermediate board (levels ANIN_A1,ANIN_A2 from I2C DAC, switch ANIN_N04 from CMOS)

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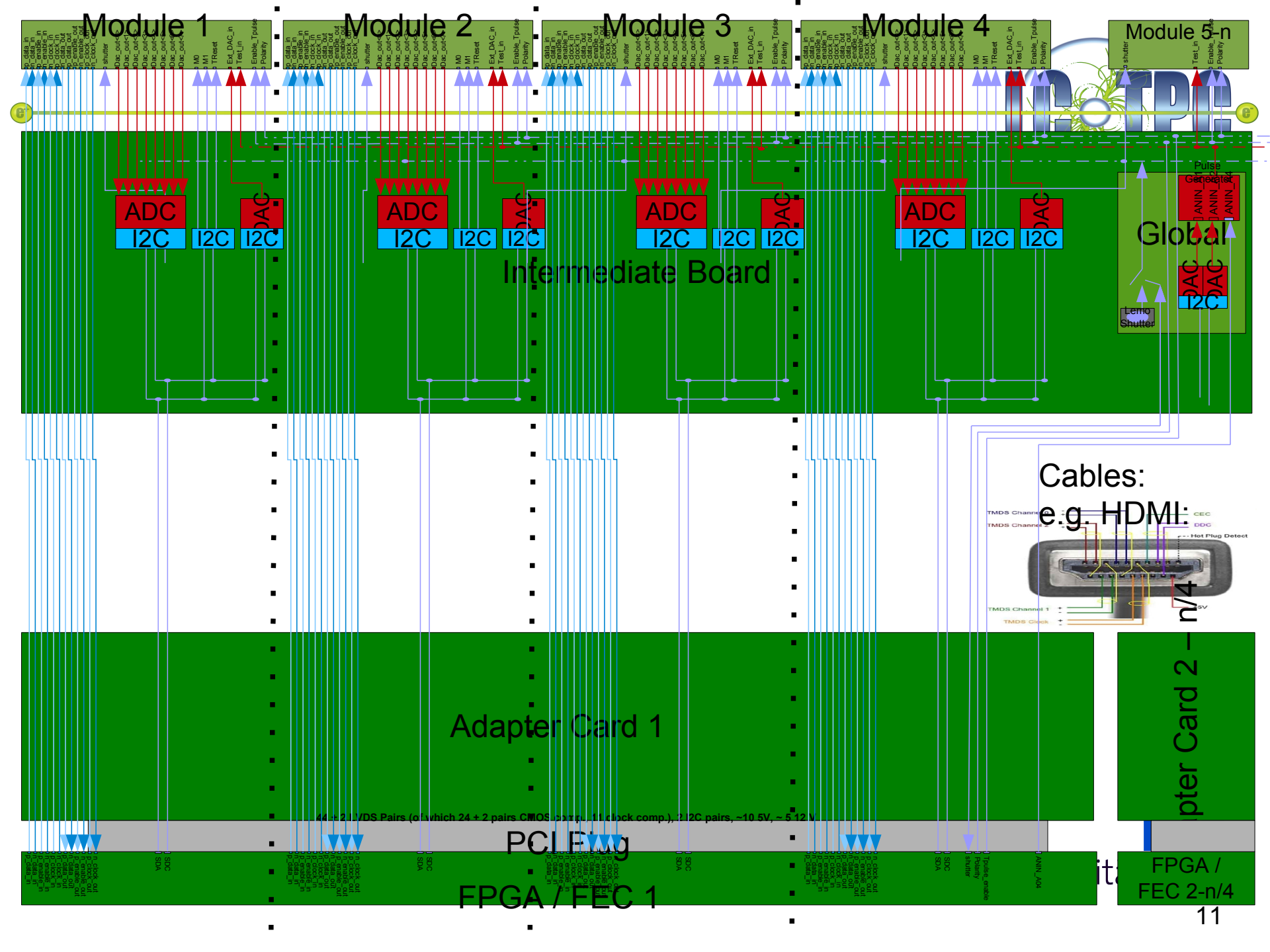
Module 1
Module 2
Module 3
Module 4
Module 5-n
ADC
I2C
DAC
Intermediate Board
Pulse Generator
Global
Lemo Shutter
Cables:
e.g. HDMI:
Adapter Card 1
Adapter Card 2 – n/4
PCI Bus
FPGA / FEC 1
FPGA / FEC 2-n/4