GDCC
“next replacement of the LDA”

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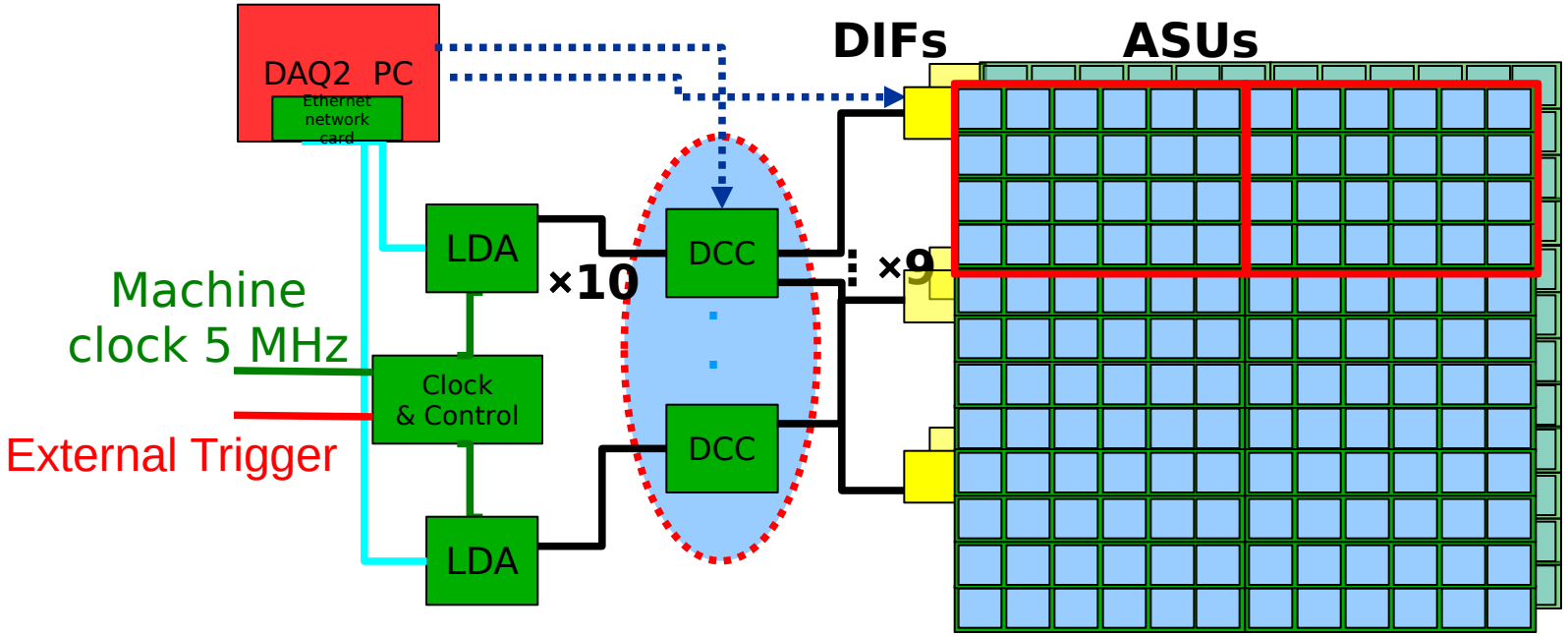
Outline

- Overview of the DAQ
- The story of the LDA
  - The Firmware
  - The Board
  - Feedback after the last test beam
- The GDCC project
  - Status of the current work
  - Planning
- Conclusion

Overview



Digital (Config, Control, Data, Trigger, Busy) over HDMI

Clock & Trig, Busy over HDMI

Optique GigE

Debug USB

DCC = Data Concentrator Card
LDA = Link Data Agregator
CCC = Clock & Control Card
DIF = Detector Interface

The story of the LDA

The Firmware

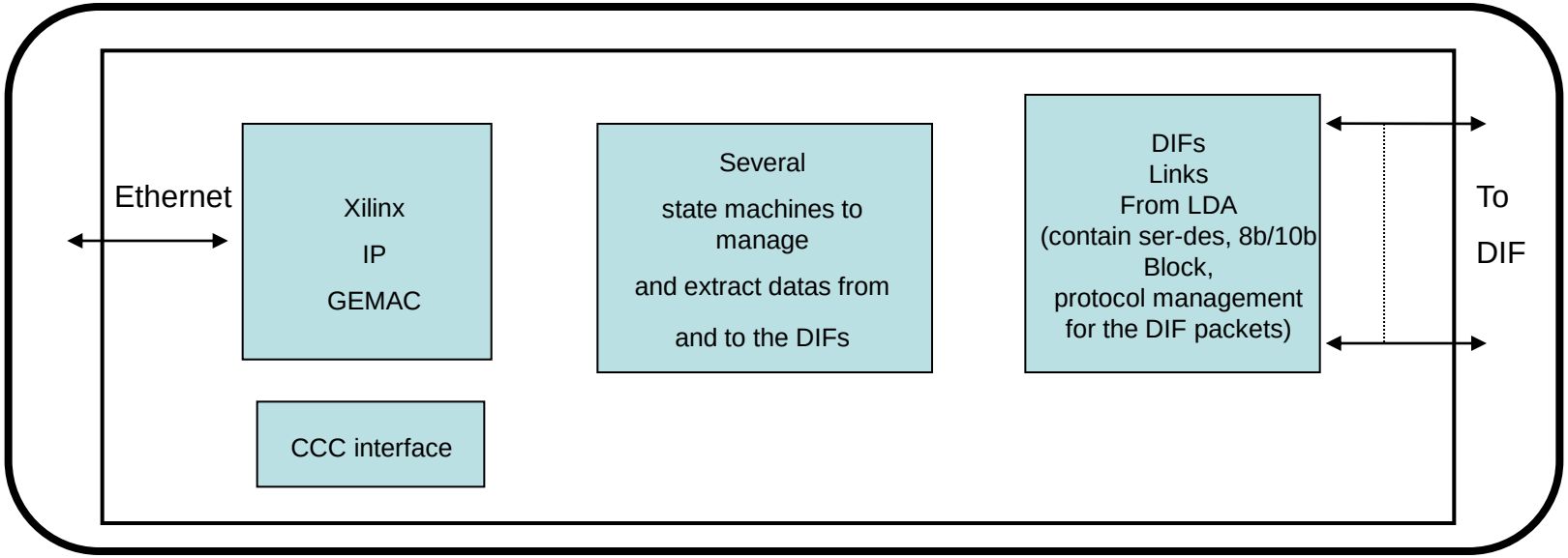
LDA is divided in 4 main functions

• Ethernet interface : Xilinx specific, black box for the user and cannot be maintained.

• Intermediate interface : Packets manager, can be re-used, but difficulty to do the reverse engineering.

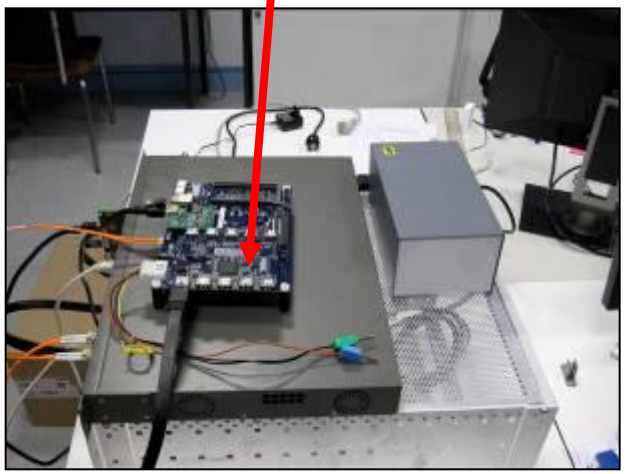
• DIFs interface : Protocol & Link management, “good enough” knowledge of code for re-use… but need for improvement for the next FPGA family.

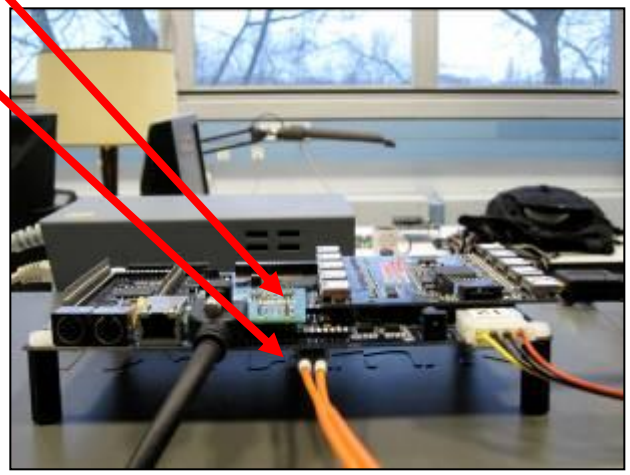
• CCC interface : Distribution of clock and trigger, detection of busy, RamFull, selection of some fast_commands



The Board

- LDA is a board with several mezzanines
  - Clock connection from the CCC
  - Ethernet connection
  - HDMI connection

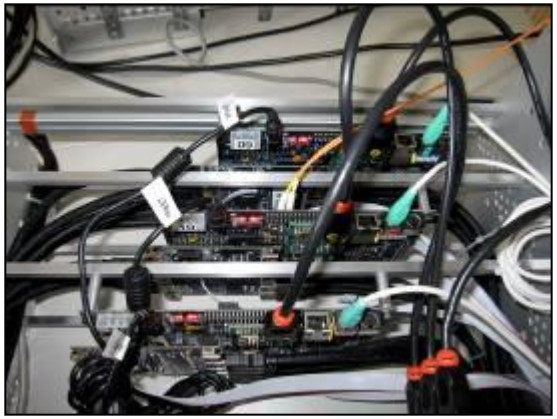




LDA on experimental site

example for DHCAL

Rails have been installed to maintain the LDA



example for ECAL

Put up on the chassis

Feedback after the last test beam and our experience of this board

- The board :
  - Not a standard size format
  - Problem with the grounding and shielding
  - Only few channels works correctly on each board (difference from a board to another one)
- The firmware :
  - GEMAC Xilinx IP core obsolete
    - Mandatory to use the old Xilinx software ISE11
  - Difficulty to maintain the main part of firmware

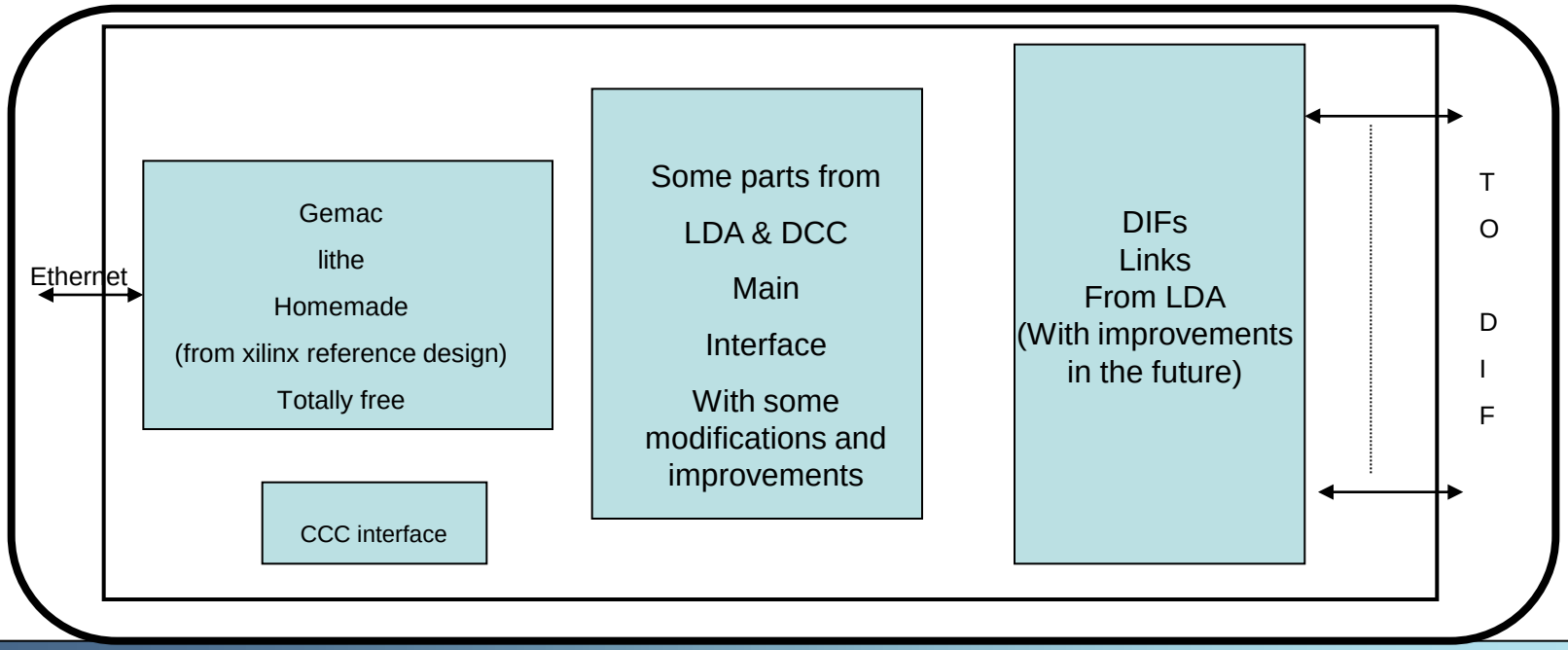
Towards a new board
The GDCC
(prototyping step)

GDCC firmware

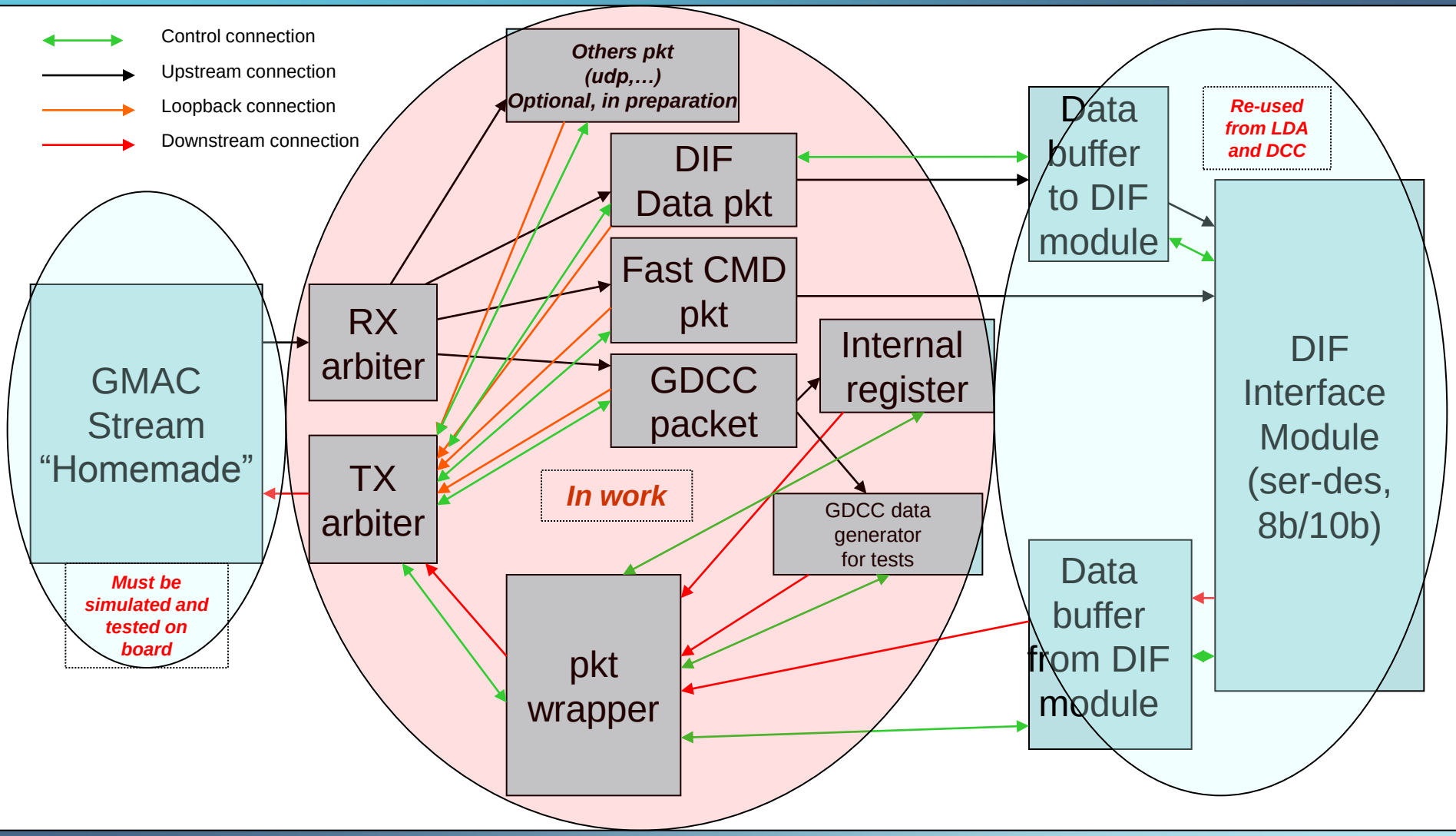
We do not change the main architecture compared with the LDA.

Only the code is slightly modified.

- Re-using some blocks from LDA and DCC
- Replace the GEMAC IP core by a free module with the same behavior
- Replace some blocks for an easiest maintenance and future evolution
- CCC function manages the fast command and busy, **clock and trigger are managed by the hardware**



Firmware architecture (In work)

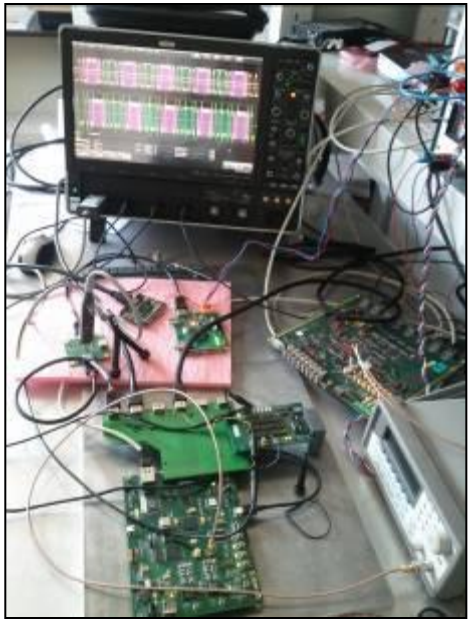


Firmware tests

The firmware is tested on Xilinx Spartan 6 evaluation board.

Setup put in place since June

- Commands have been received correctly
- The link to the DIF is locked
- The status can be read



GDCC hardware architecture

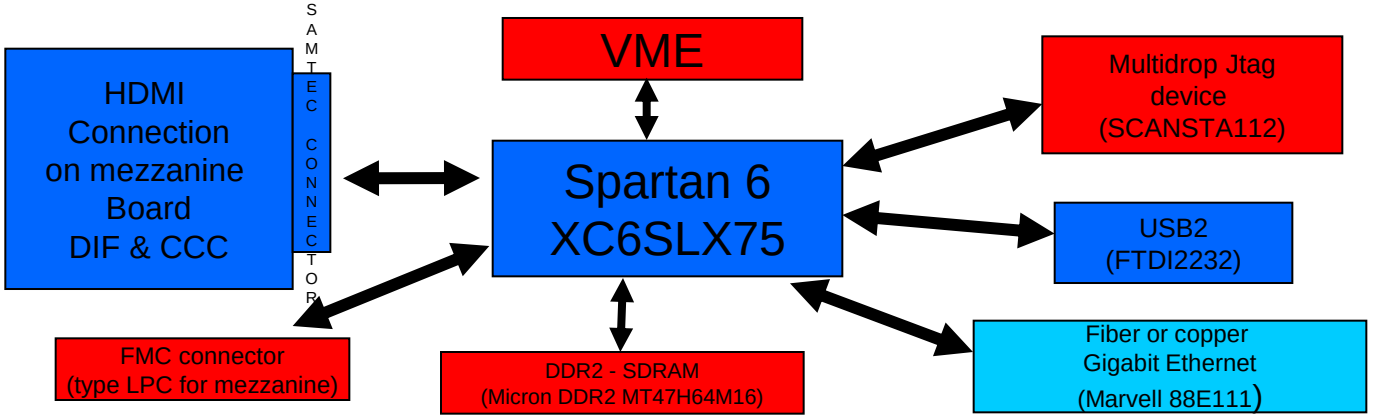
GDCC is powered by VME connector

Dark blue : design based on LDA and DCC but with a reliable connection for the mezzanine. Clock and trigger are distributed by the mezzanine.

Light blue : Physical layer device for Ethernet connection

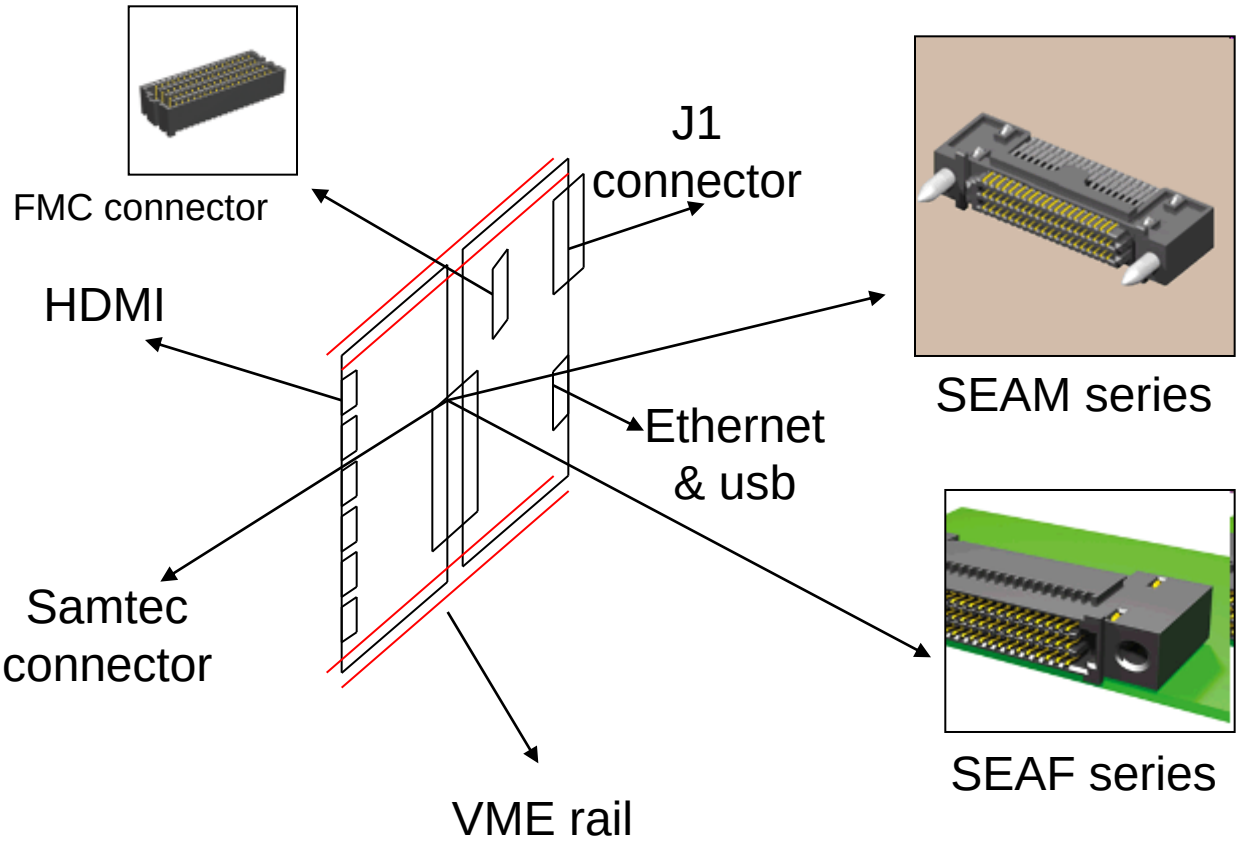
Red : new part, foreseen but optional

- VME : minimum access foreseen (8 bits data, 16 bits address, 1 IRQ, no arbitration)
- Jtag device for download FPGA : multidrop Jtag access (foreseen to access several boards in remote and the ability to remove a board from the system and retain access to the remaining boards).
- FMC connector : possibility to connect mezzanine board with FMC standard
- DDR2
- ***nota*** : USB device can be used to download the FPGA



GDCC Board integration

Design of a board with a VME size : Board to board solution



GDCC Layout

Mezzanine

12 layers

Size : 233 x 52.8 mm

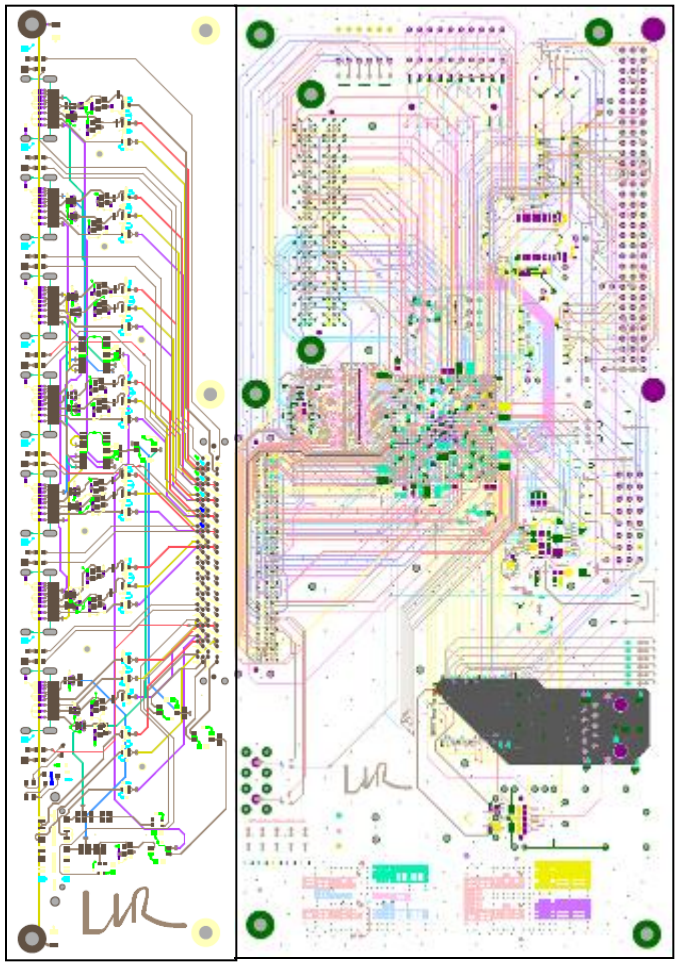
Thickness : 1.81 mm

DIF HDMI * 6

CCC HDMI

Additional Samtec connector

Foreseen to plug mini-mezzanine board and to test different kind of connectors



GDCC

12 layers

Size : 233 x 106.66 mm

Thickness : 1.81 mm

Cost estimation (for 3 boards : prototype part)

- Estimated time of manufacture : 20 days for the PCB, 5 days for the cabling, 20 days for supplying of components.

  The production of prototypes takes 2 months maximum
  - Per board (GDCC main)
    - Board :430 €
    - Cabling : 600 €
    - Tools : 310 €
    - Component : ~293 €
    - Total : 1633 €
  - Per board (mezzanine)
    - Board : 385 €
    - Cabling : 465€
    - Tools : 310 €
    - Component : ~178 €
    - Total : 1338 €

- **TOTAL GDCC** : 2971 € /board

Conclusion

- 3 boards will be launch in production this week
  - We hope to receive the boards in November
- Tests will be organized in several steps
  - Check the hardware part : FPGA download, clock and trigger distribution, etc…
  - Firmware tests in LDA mode
    - Long term tests
  - Tests of USB and Jtag devices
  - Less priority : VME, DDR2 (no written vhdl code for now)
- GDCC will not available before April 2013
  - If there is not a significant problem