# Status of the SDHCAL DAQ

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Cambridge CALICE meeting

# Overview

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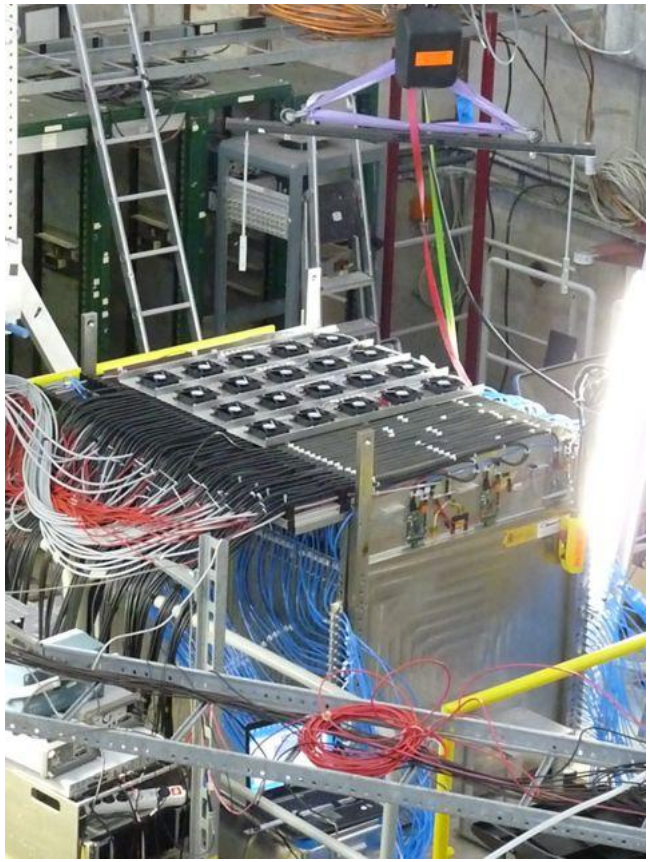
3. Collaboration LAPP - IPNL
4. Software
5. DAQ System
6. DAQ Features
7. Futur DAQ Features
8. Beam Test
9. Conclusion



Or how to build a DAQ in less than 6 months…

- November 2011 : The CALICE DAQ is postponed …
  DAQ no stable and not ready to take data for a huge number of detectors in 2012

-December 2011 : beginning of the work on the SDHCAL DAQ

*Happy new Year !!*

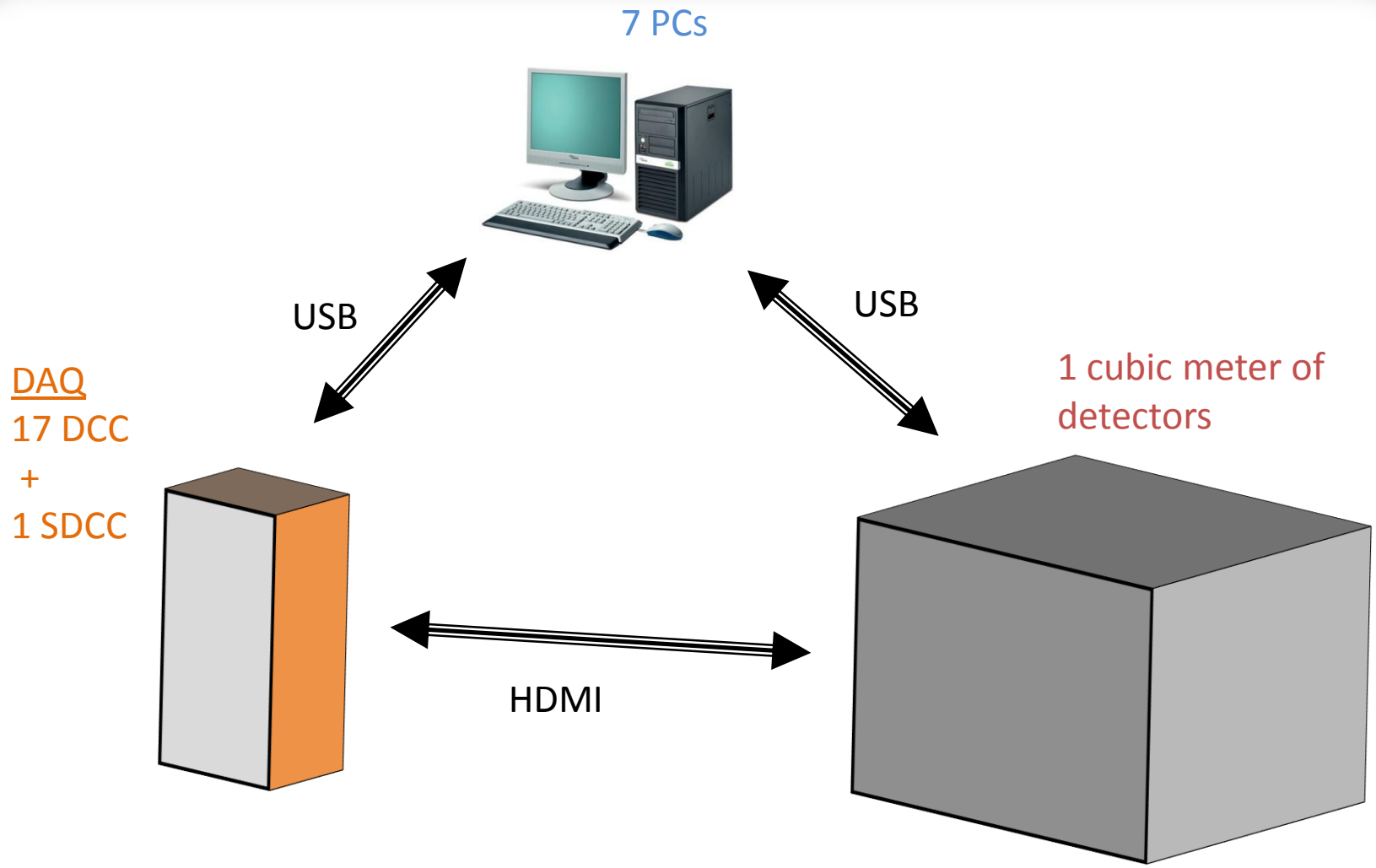
- January and February 2012 : development and test on a few number of detectors

- March and April 2012 : huge work in common on the Cubic meter to be ready to the 1st Beam Test

- mi-April 2012 : 1st Beam Test, the DAQ is working well ☺

# 2. Architecture



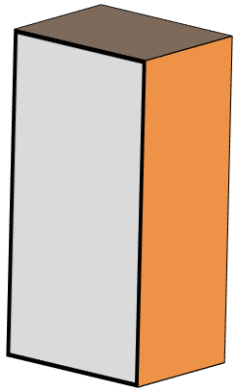


# 3. Collaboration LAPP - IPNL

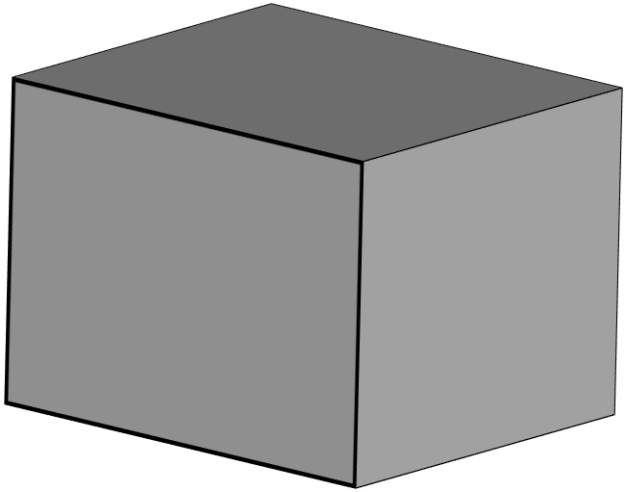


Software : XDAQ
Christophe Combaret (IPNL)
Laurent Mirabito (IPNL)

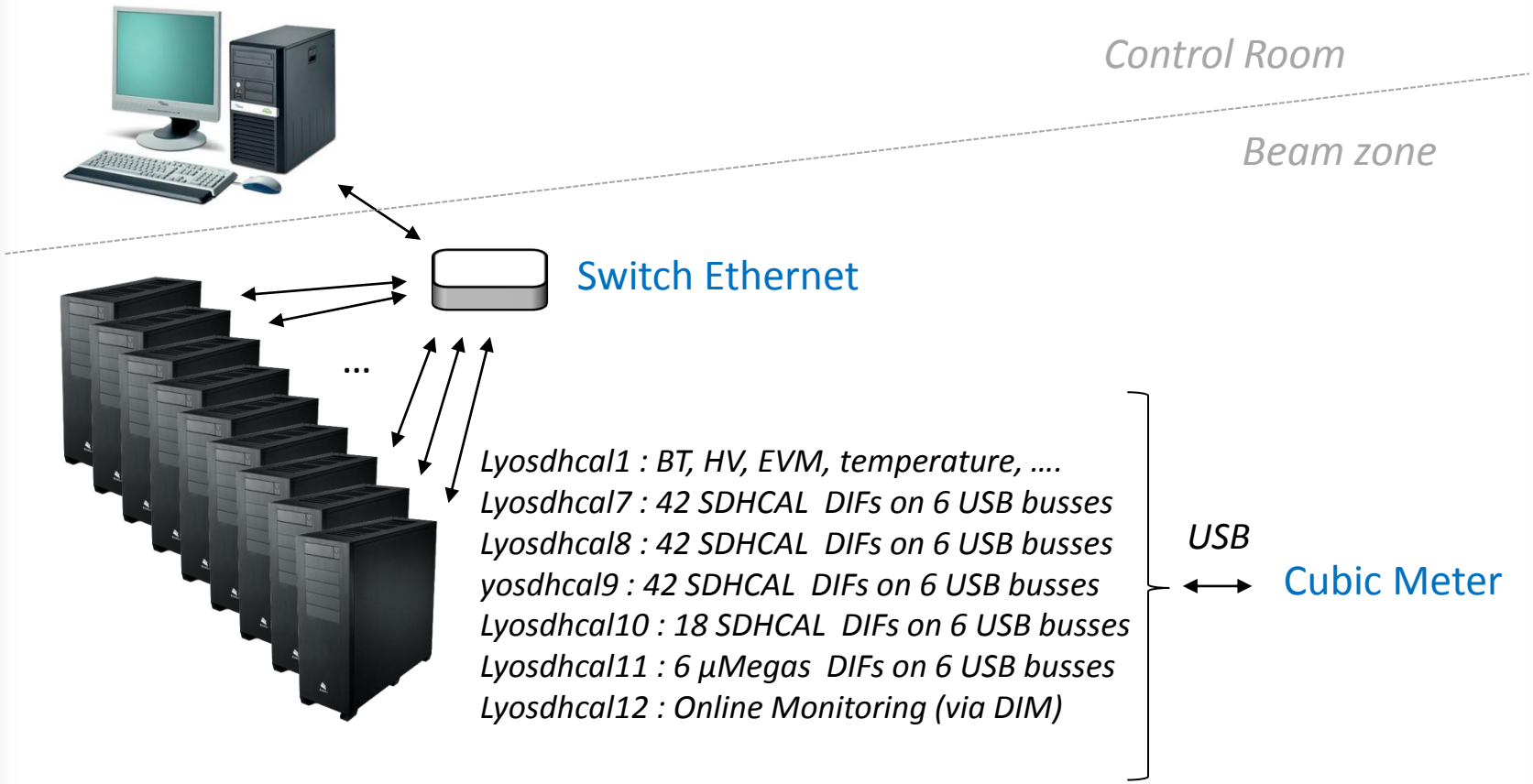
Detectors :
- 48 plans RPC (IPNL)
- 2 plans µMEGAS (LAPP)



DAQ system:
(DCC + DIF) Firmware
Guillaume Vouters (LAPP)



## Multi PC's acquisition



## DAQ Software

Using Xdaq Framework (CMS DAQ)

- Distributed readout and computing
- CMS Event builder
- Executives : web server dynamically loading applications

Configuration database (located at CC in2p3)

- Storage and history of configuration parameter

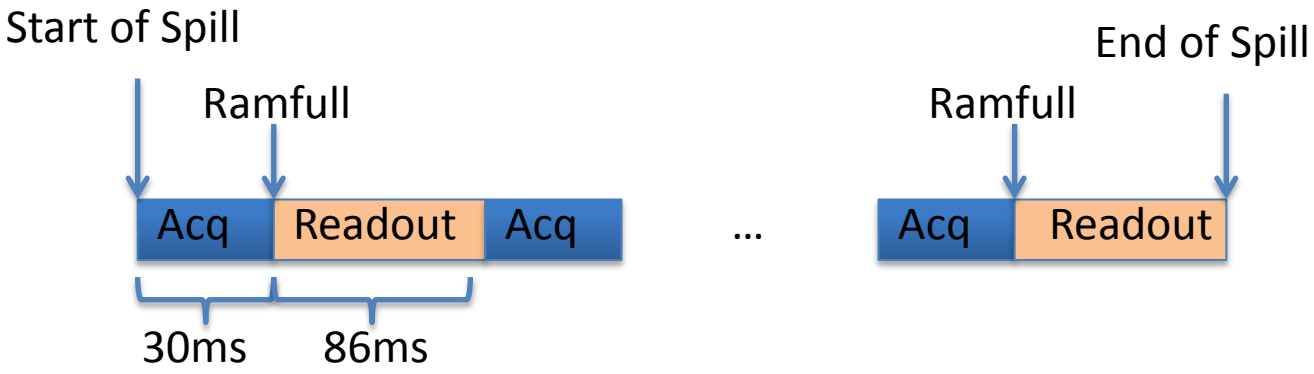
DB model and interface library (C or C++)

ILCCONFDB developped by G.Baulieu

- DBManager to access DB and make appropriate downloads

Online Monitoring (running independently from DAQ). Data exchanged using DIM.

## Performances

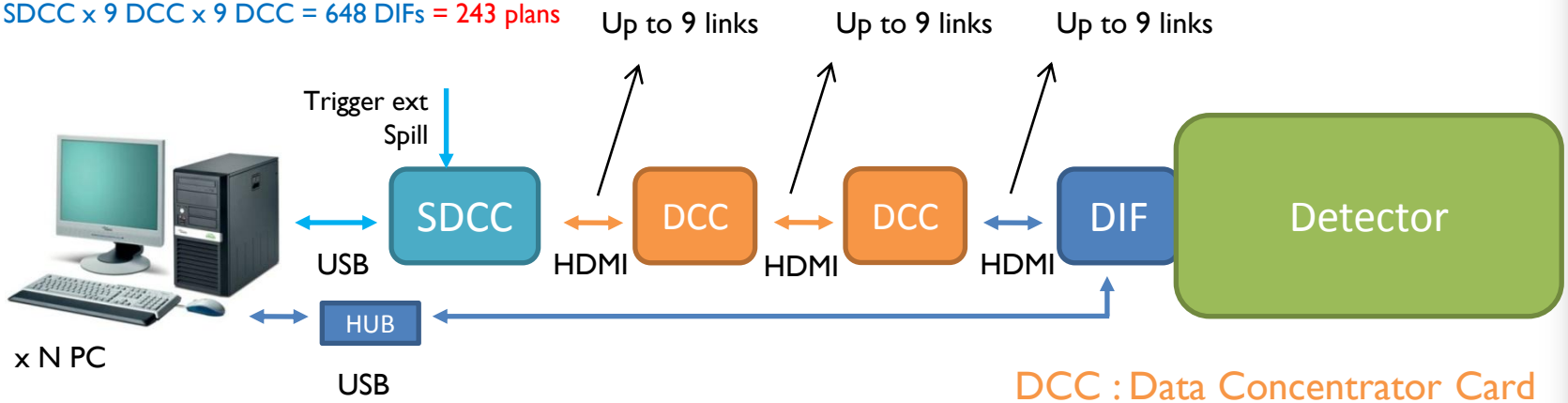



- Acquisition time = 150E3 clocks = 30 ms
- 1 spill (SPS) = 9,3s
- Collected : 80 Evts / spill
- 1 evt = 8kB per DIF (average)
- Events are buffered in PC RAM (4GB available) -> 12 K events can be buffered.

No DAQ crash for 2012 beam tests . Only observed instabilities came from pc excessive temperature (bad cooling of these machines)

## DAQ Architecture

9 SDCC x 9 DCC = 81 DIFs = 27 plans
9 SDCC x 9 DCC x 9 DCC = 648 DIFs = 243 plans




DCC : Data Concentrator Card
SDCC : Synchronous DCC
DIF : Detector InterFace

| HDMI pin | CCC name | DIF name | use |
|---|---|---|---|
| **1-3** | LCK_OUT | LDA_CLK (in) | 5MHz CLK |
| **4-6** | LCONT_OUT | LDA_DL2D (in) | command |
| **7-9** | LBUSY_IN | LDA_DD2L (out) | BUSY |
| **10-12** | LSPAREIN | LDA_SPD2L (out) | Ramfull |
| **15-16** | LFTRIGOUT | LDA_SPL2D (in) | Not used |
| **2-5-8-11-17** | ground | ground | ground |
| **13-14-18-19** | Connected through 0 ohm R | 3.3 V | NC |

## The intelligence of the system

SDCC

*SDCC : Synchronous DCC*

-Interface between the PC and the DAQ

*DCC with the SDCC firmware*

- Synchronization of the system

*Deal with the busy, etc …*

- Automatism of the system

*make the system working by itself*

- Received command from the PC
- Send command to the DIFs

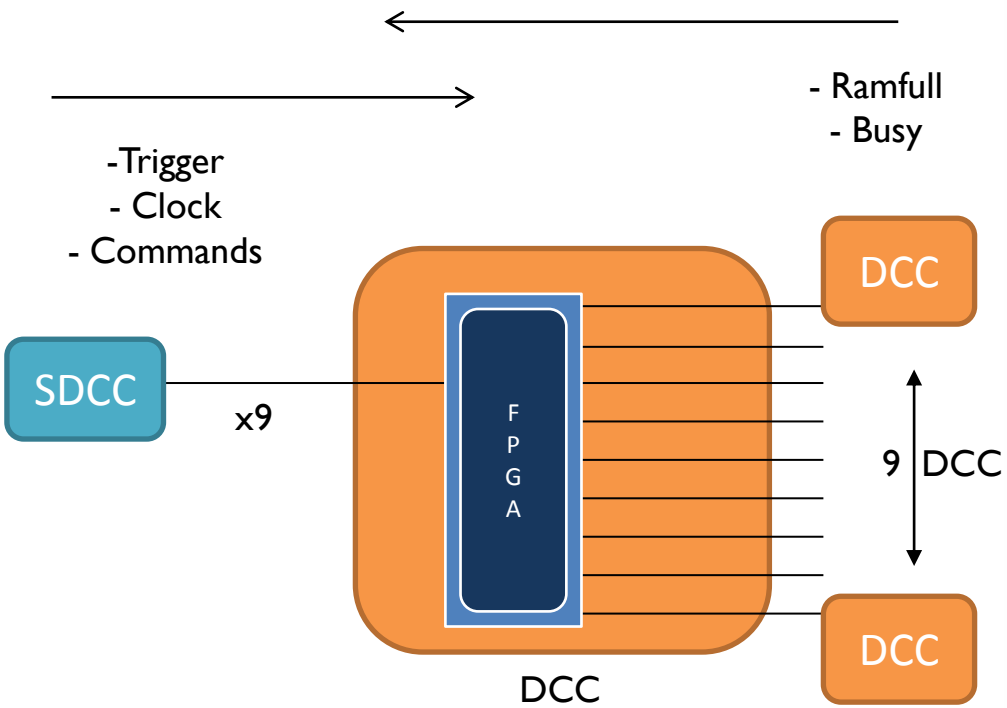
*Made in LLR (Paris)*

## Used like a switch

*DCC with the DCC switch firmware*

DCC

*DCC : Data Concentrator Card*




*Made in LLR (Paris)*

## The heart of the system

DIF

*DIF : Detector InterFace*


- Interface between the detector and the DAQ
  *RPC or MicroMEGAS detectors*

- Same DIF used for RPC or MicroMegas
  *2 similar codes (but different) for RPC and Micromegas*

- Communication with PC through USB and HDMI
  *HDMI via DCC*

- Perform all the features
  *See the next slide*

*Made in LAPP (Annecy)*

# 6. DAQ Features

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## RPC

- USB and HDMI interface
- ASICs configuration
- Digital Readout (Trigger mode)
- Digital Readout (ILC mode)
- Power Pulsing
- Temperature DIF

## MicroMegas

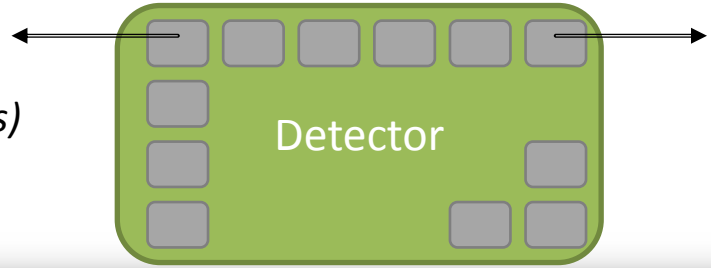
- USB and HDMI interface
- ASICs configuration
- Digital Readout (Trigger mode)
- Digital Readout (ILC mode)
- Power Pulsing
- Temperature DIF
- Analog Readout
- Calibration
- 4 independent lines
- Temperature ASU

Everything is stable and reliable !!

This DAQ runned severeal weeks without any crash and with Power Pulsing

HARDROC *pour RPC*

*Made in LAL/Omega (Paris)*




MICROROC *pour MICROMEGAS*

*Made in LAL and LAPP*

# 7. Futur DAQ Features



## RPC

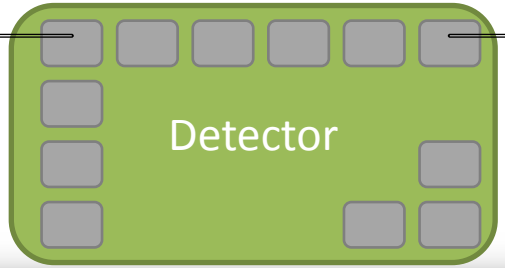
- Slow Control monitoring
- Data Compression

## MicroMegas

- Slow Control monitoring
- Data Compression

HARDROC *pour RPC*

*Made in LAL/Omega (Paris)*



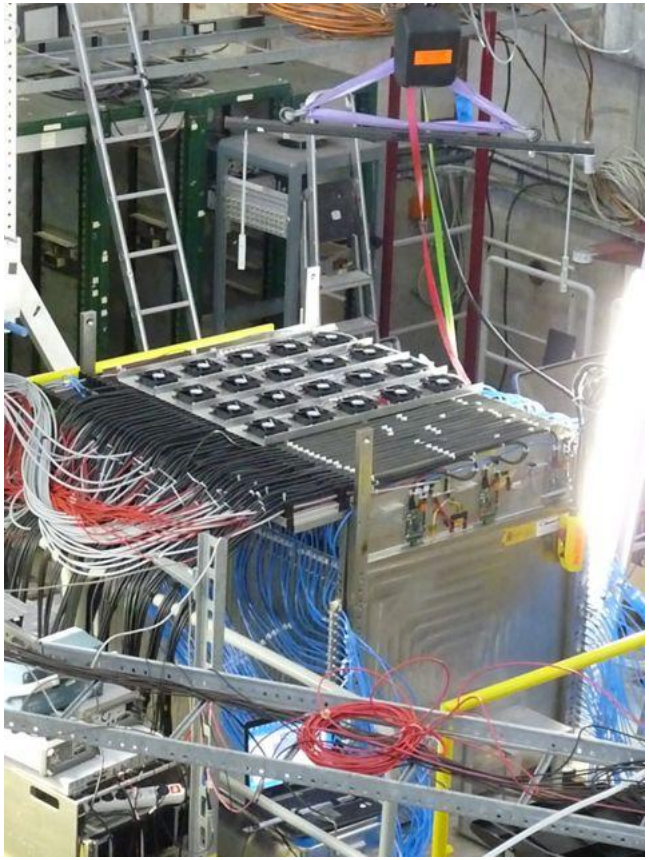

MICROROC *pour MICROMEGAS*

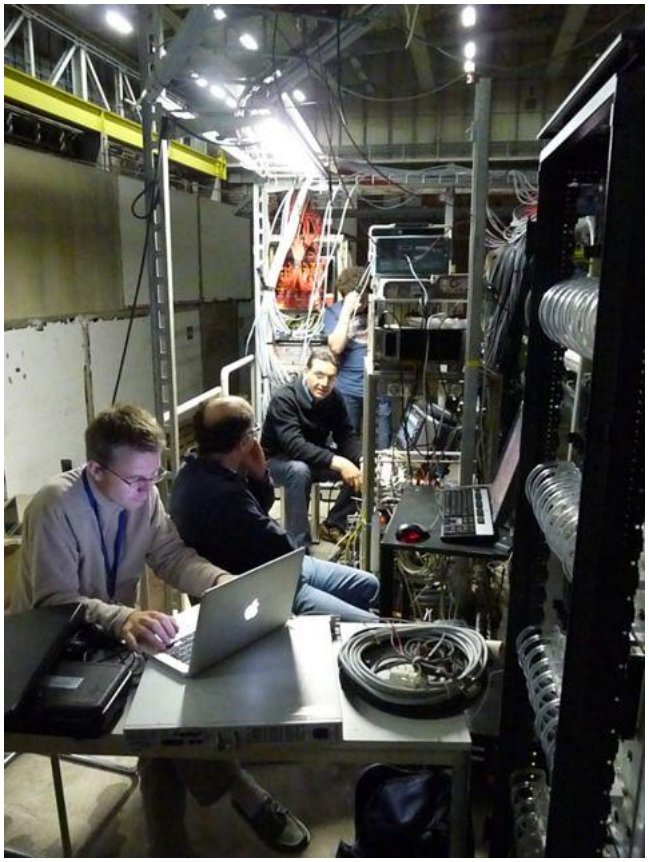
*Made in LAL and LAPP*

# 8. Beam Test



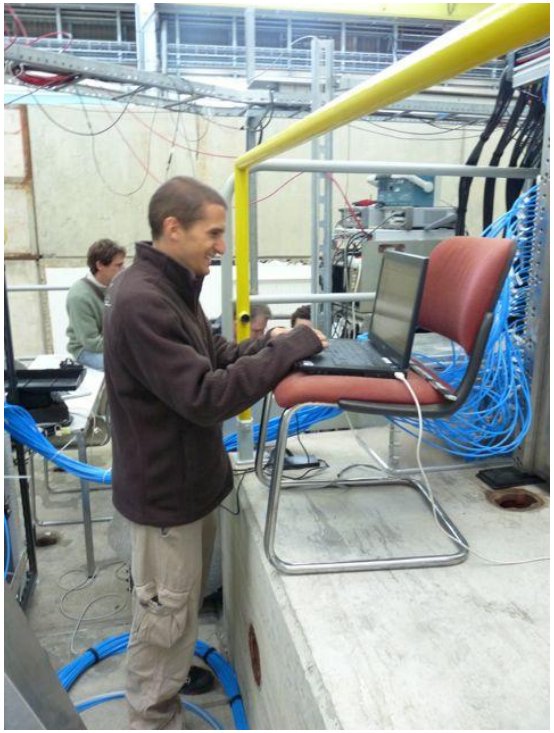
→ PS





Everybody is working
Even me !!

→ PS



Flyyyyy !!

→ SPS

# 9. Conclusion

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A great job has been done until now !

Spring 2012
- 2 weeks at PS (RPC + MicroMEGAS)
- 2 weeks at SPS (RPC + MicroMEGAS)

Summer 2012
- 2 weeks at SPS (RPC only)

Automn 2012
- 1 weeks RD51 at SPS (MicroMEGAS only)
- 2 weeks at SPS (RPC + MicroMEGAS)

There was a good collaboration and really a lot of work for building the SDHCAL DAQ in only 4/5 months to be ready for the 1st 2012 Beam Test !!

It allowed and will allow us to take a lot of data in 2012

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# Thank you for your attention

Do not miss Max Chefdeville talk about « MicroMEGAS status and perspectives » this afternoon

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# Backup Slides

## Beam Zone