Pipelined SAR ADC for SiPM readout

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Outline

- Motivation & Requirements of the ADC
- ADC structure

  Track / Hold, SAR ADC, etc...
- Parameter Calculation and Estimation
- Summary & Time Plan

Motivation and Requirements

- Quatization (one ADC per channel):
  - charge integration
  - timing voltage ramp
- Resolution - **12** bits ? - **SiPM Optimization**

  3 different types of signal to quantize:
  - calibration signal, only a few pixel fired
  - physical MIP-like signal, large fluctuation
  - timing voltage ramp

Resolution Requirements

- **Calibration signal**

i. clearly seperated peak - **1 mV** electronic noise - **12** bits

ii. up to **10** pixels, range of ~300mV (small range)

iii. only a small portion of the total signals

- **Physical signal - Much larger uncertainty - Less resolution**

i. large fluctuation due to Landau Distribution

ii. signal uncertainty due to the detector pixel uniformity
4-5mV (15 pxls , MPPC 50um pitch device)

iii. most time, **8 bits** sufficient - Quantization noise (**3.7mV**)

- **TAC ramp signal**

i. same ramp speed by SPIROC

ii. 10 bits - 400ps bin size - <100ps quantization error

iii. if **ns** resolution sufficient, only **8 bits** required

Requirements

- Resolution : **8 bits** for most of time
  12 bits for calibration only (shortly)
  10 bits necessary for precise timing

Other Requirements

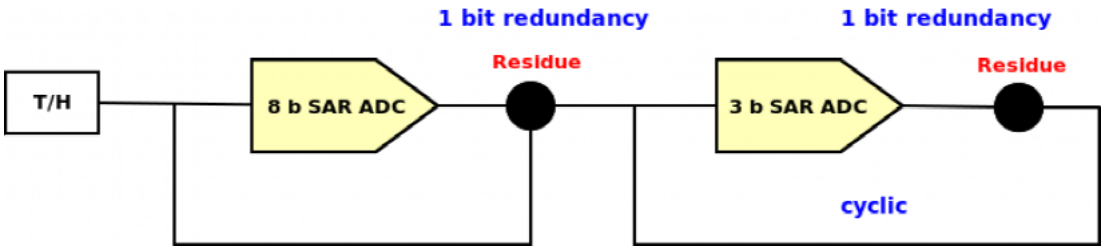
Performance	*Parameter*
Area	~ 100μm * 700 μm
Sampling Rate	> 1 MHz
power	μW w/ pulsing
SNDR, SFDR	descent

ADC Structure

- 8 bits low power (!) , small size ADC, **SAR** is the perfect choice
- sampling rate easily exceeds **1 Mhz.**

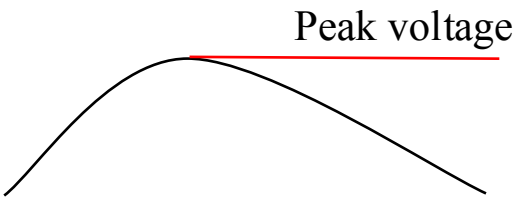
  only **µs** needed for analog memory, less distorsion
- the **extra 2 bits (10bits)** required by timing can be **pipelined**
- the additional **2 bits (12bits)** can be **cyclic**

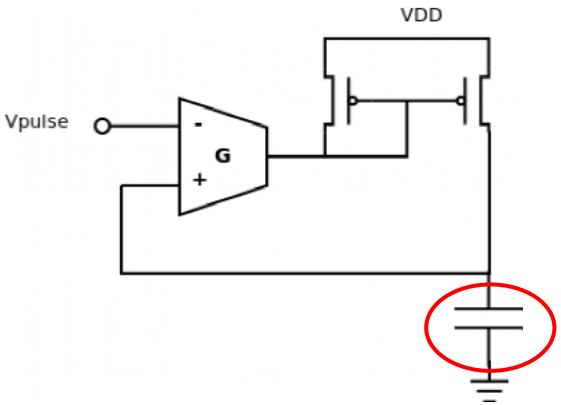
  (only shortly)



Peak Sensing - Track/ Hold

Peak sensing using a **peak detector and holder (PDH)**

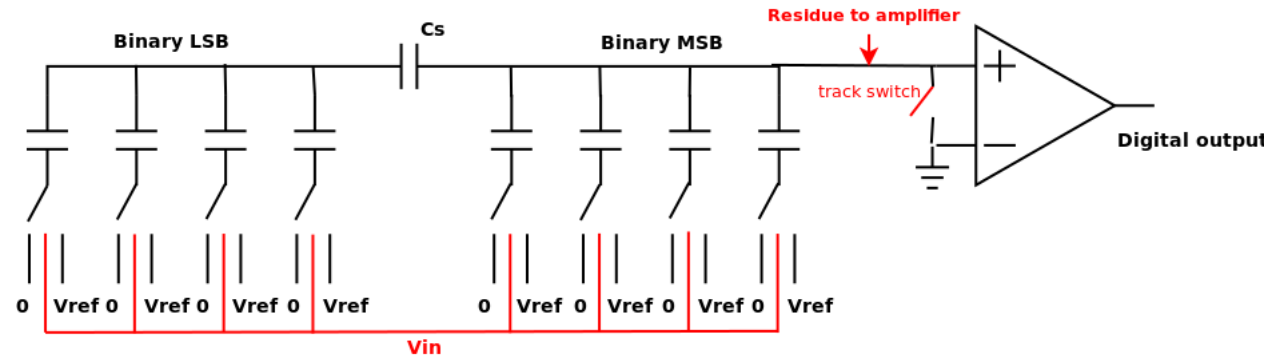




Peaking time is input pulse shape dependent, easier to control with PDH

Memory capa can be merged to SAR capa

Succussive Approximation Register ADC

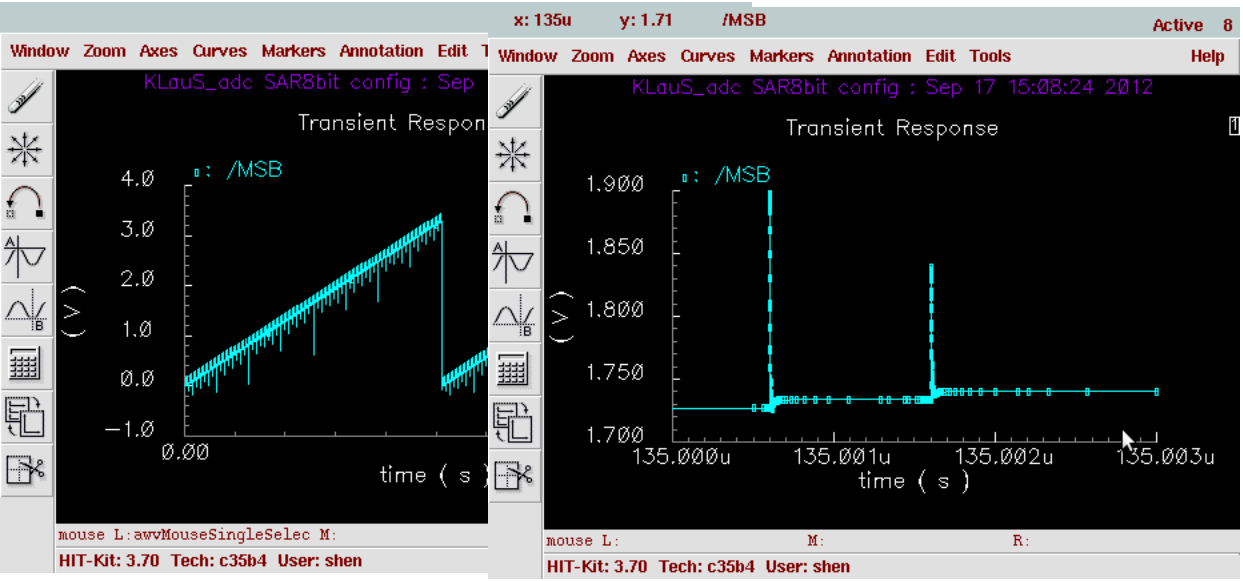


In order to counteract the Mismatch Error and Nonlinearity

According to the AMS datasheet, the minimum of unit capa is 7µm*7µm, at the moment 10µm*10µm is chosen

The capa total size is 100µm * 32µm,
Memory Depth of 4, 100µm * 150µm, very small in size

Simulation for the 8b SAR



8 bits Scan MC
DNL/INL < 0.5 LSB

Zoom of each step,
response fast enough

Summary

- SAR ADC structure chosen
- 8 bits for physical signal, 10 & 12 bits can be pipelined
- Size estimation 100μm * 600μm
- Pulsed power consumption μW

- Design started, Tapeout estimation Apr. 2013