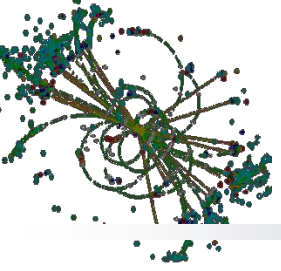# Status of the Chronopixel Project

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In collaboration with J.E.Brau, D.M.Strom (University of Oregon, Eugene, OR), C.Baltay, H.Neal, D.Rabinovitz (Yale University, New Haven, CT)
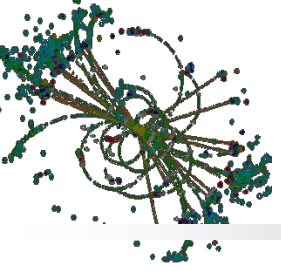
EE work is contracted to Sarnoff Corporation

Outline of the talk

- **What is chronopixel?**
- **Project timeline**
- **First prototype design**
- **First prototype test results**
- **Design of the second prototype**
- **Simulations of expected performance.**
- **Preliminary results of the second prototype tests.**
- **Conclusions and plans**

What is chronopixel?

- Need for pixel detector with good time resolution:
    - Background hits density in ILC environment is of the order of 0.03 hits/mm² per bunch.
    - Bunch train at ILC, which lasts only 1 ms, has about 3000 bunches ⇒ 100 hits/mm² – too high for comfortable track reconstruction.
    - So we need to slice this array of hits into at least 100 time slices, and reconstruct tracks from hits belonging to the same slice. To do this, we need to know time of each hit with at least 10 μs accuracy.
- CCDs, often used as pixel detectors, by the nature of their readout, are very slow. Row by row readout takes tens if not hundreds of ms to read image. So we would integrate the entire bunch train in one readout frame.
- There is a number of pixel sensor R&D addressing this problem – CPCCD, different types of monolithic designs (readout electronics on the same chip as sensor), 3D technology. Neither of them (except, may be 3D) allows assigning time stamp to each hit.
- Chronopixel project was conceived to provide such ability.
- Chronopixel is a monolithic CMOS pixel sensor with enough electronics in each pixel to detect charge particle hit in the pixel, and record the time (time stamp) of each hit.
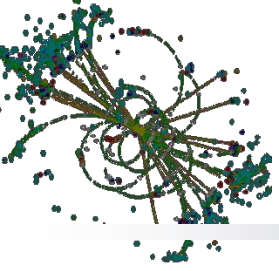
Timeline

- **2004 – talks with Sarnoff Corporation started.**
  - Oregon University, Yale University and Sarnoff Corporation collaboration formed.
- **January, 2007**
  - Completed design – Chronopixel
    - **2 buffers, with calibration**
- **May 2008**
  - Fabricated 80 5x5 mm chips, containing 80x80 50 μm Chronopixels array (+ 2 single pixels) each
  - TSMC 0.18 μm $\Rightarrow$ ~50 μm pixel
    - Epi-layer only 7 μm
    - Low resistivity (~10 ohm*cm) silicon
- **October 2008**
  - Design of test boards started at SLAC
- **June 2009**
  - Test boards fabrication. FPGA code development started.
- **August 2009**
  - Debugging and calibration of test boards
- **September 2009**
  - Chronopixel chip tests started
- **March 2010**
  - Tests completed, report written

- **May 2010**
  - Second prototype design started
- **September 2010**
  - contract with Sarnoff for developing of second prototype signed.
- **October 2010**
  - Sarnoff works stalled
- **September 2011**
  - Sarnoff resumed work.
- **February 2012**
  - Submitted to MOSIS for production at TSMC.
  - Modification of the test stand started as all signal specifications were defined.
- **June 6, 2012**
  - 11 packaged chips delivered to SLAC (+ 9 left at SARNOFF, +80 unpackaged.)
  - Tests at SLAC started
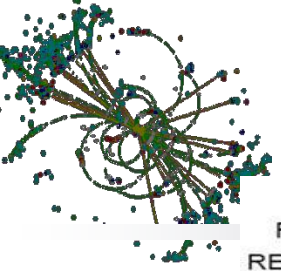
First prototype design
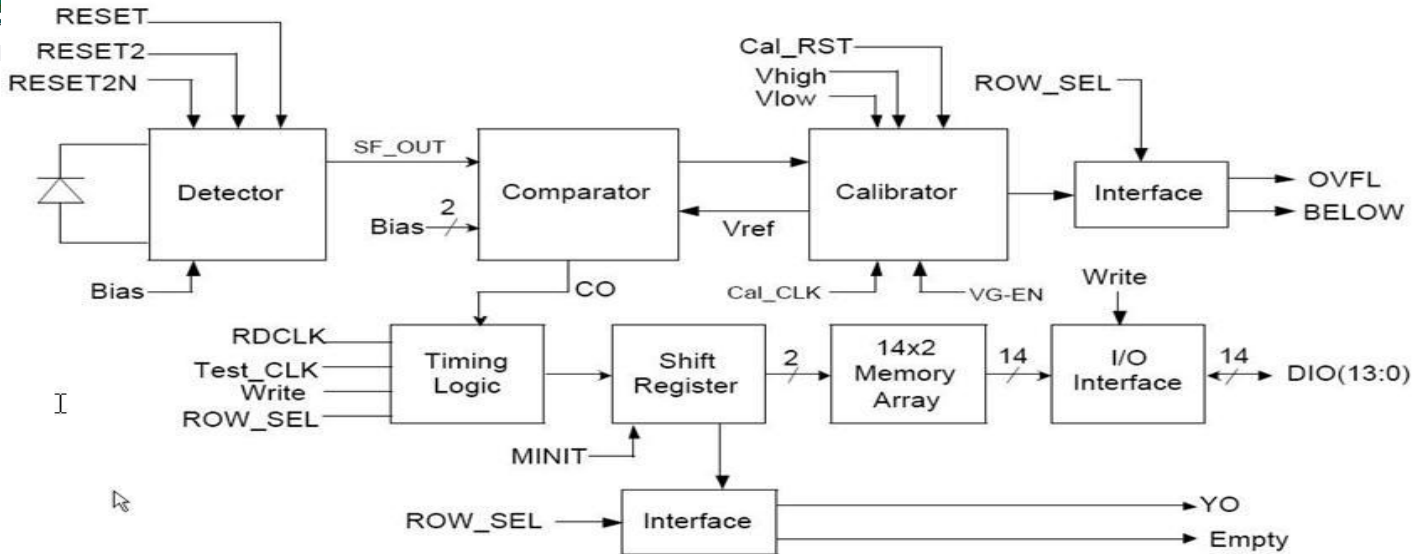
- Monolithic CMOS pixel detector design with time stamping capability was developed in collaboration with Sarnoff company.
- When signal generated by particle crossing sensitive layer exceeds threshold, snapshot of the time stamp, provided by 14 bits bus is recorded into pixel memory, and memory pointer is advanced.
- If another particle hits the same pixel during the same bunch train, second memory cell is used for this event time stamp.
- During readout, which happens between bunch trains, pixels which do not have any time stamp records, generate EMPTY signal, which advances IO-MUX circuit to next pixel without wasting any time. This speeds up readout by factor of about 100.
- Comparator offsets of individual pixels are determined in the calibration cycle, stored in digital form, and reference voltage, which sets the comparator threshold, is shifted to adjust thresholds in all pixels to the same signal level.
- To achieve required noise level (about 25 e r.m.s.) special reset circuit (soft reset with feedback) was developed by Sarnoff designers. They claim it reduces reset noise by factor of 2.
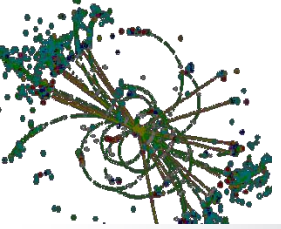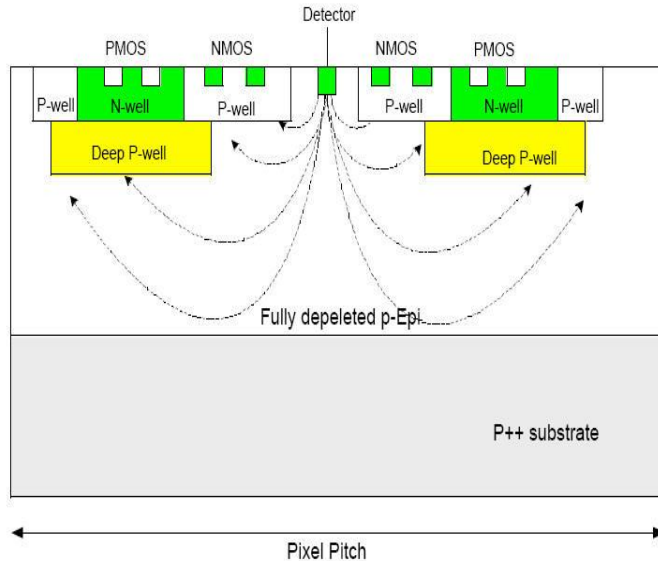
Sensor design

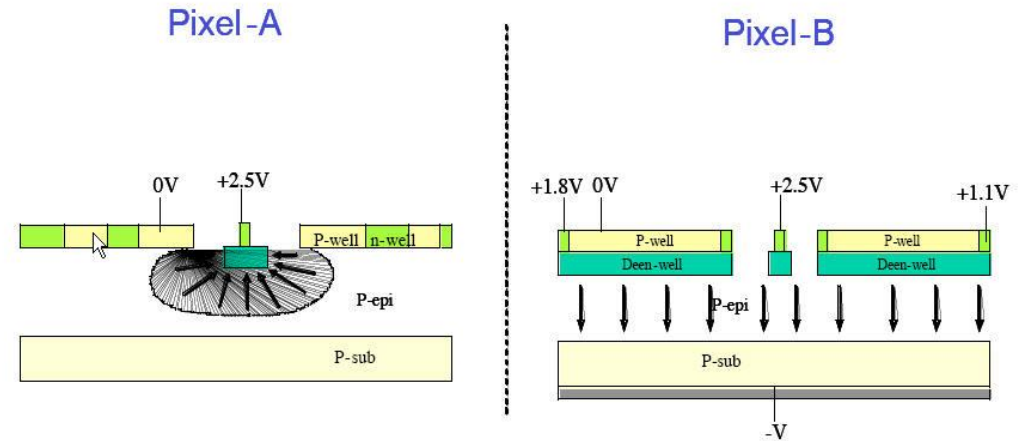Figure 11.1 Proposed pixel architecture employing the deep p-well layer

Figure 6.3 Comparison of the vertical cross section views of two pixels

**Ultimate design, as was envisioned   Two sensor options in the fabricated chips**

- **TSMC process does not allow for creation of deep P-wells. Moreover, the test chronopixel devices were fabricated using low resistivity (~ 10 ohm*cm) epi layer. To be able to achieve comfortable depletion depth, Pixel-B employs deep n-well, encapsulating all p-wells in the NMOS gates. This allow application of negative (up to -10 V) bias on substrate.**
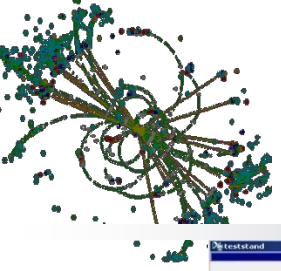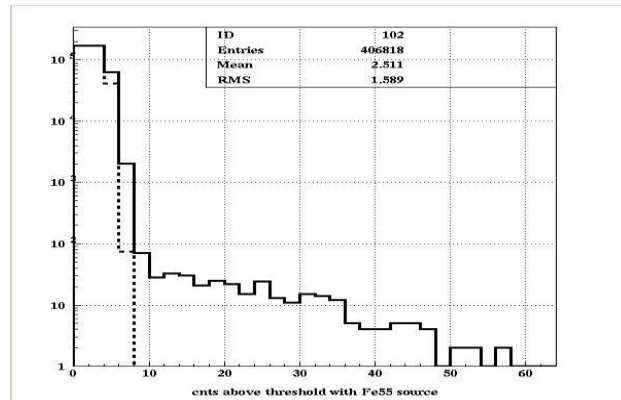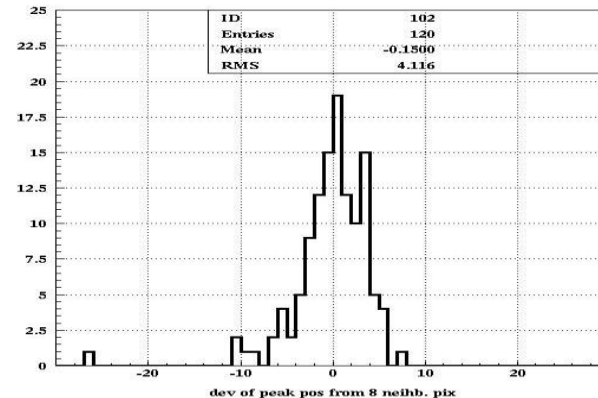
First prototype test results
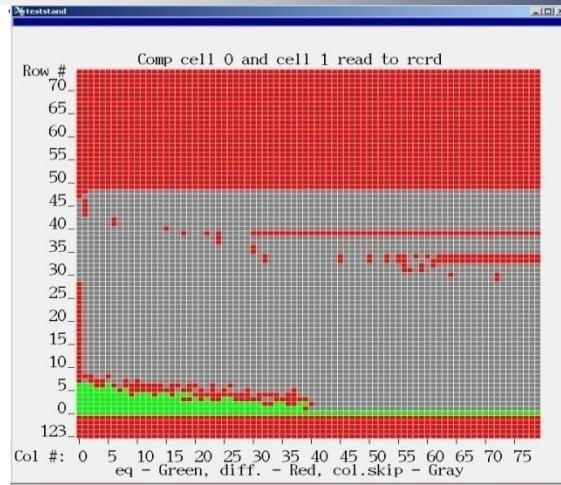
Correctly working pixels are shown in green
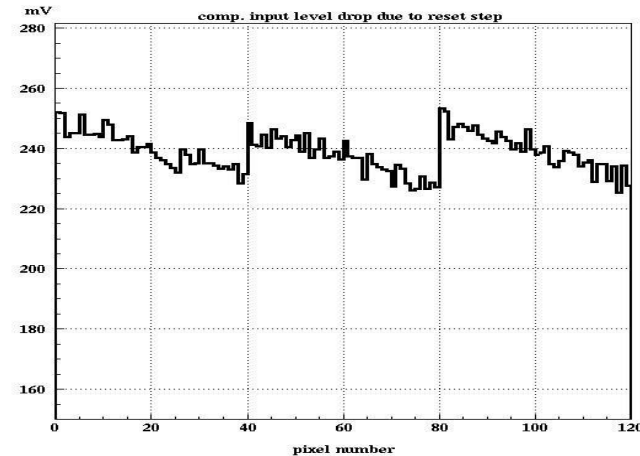
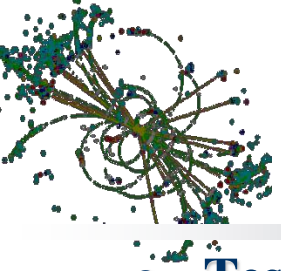Change of power supply V depending value along rows

Signal from Fe55 distribution (dotted – without source)


Distribution of comparator offsets

Mistake in power distribution in the layout led to only small portion of pixels (shown green) worked
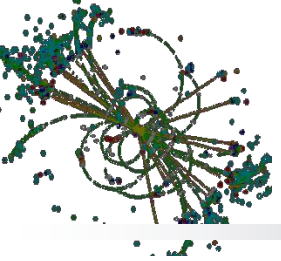
Conclusions from prototype 1 tests

○ **Tests of the first chronopixel prototypes are now completed.**

○ **Tests show that general concept is working.**

○ **Mistake was made in the power distribution net on the chip, which led to only small portion of it is operational.**

○ **Calibration circuit works as expected in test pixels, but for unknown reason does not work in pixels array.**

○ **Noise figure with "soft reset" is within specifications (0.86 mV/35.7μV/e = 24 e, specification is 25 e).**

○ **Comparator offsets spread 24.6 mV expressed in input charge (690 e) is 2.7 times larger required (250 e). Reduction of sensor capacitance (increasing sensitivity) may help in bringing it within specs.**

○ **Sensors leakage currents ($1.8 \cdot 10^{-8} A/cm^2$) is not a problem.**

○ **Sensors timestamp maximum recording speed (7.27 MHz) is exceeding required 3.3 MHz.**

○ **No problems with pulsing analog power.**
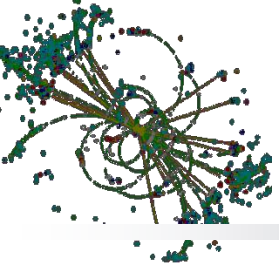
Prototype 2 features

- Design of the next **prototype** was extensively discussed with Sarnoff engineers. In addition to fixing found problems, we would like to test new approach, suggested by SARNOFF – build all **electronics inside pixels** only from **NMOS** transistors. It can allow us to have **100% charge** collection **without** use of **deep P-well** technology, which is expensive and rare. To reduce all NMOS logics power consumption, **dynamic memory cells design** was proposed by SARNOFF.

- **New** comparator offset compensation ("**calibration**") scheme was suggested, which **does not have limitation in the range** of the offset voltages it can compensate.

- We agreed **not to implement sparse readout** in prototype 2. It was already successfully tested in prototype 1, however removing it from prototype 2 will save some engineering efforts.

- In September of 2011 Sarnoff suggested to build next prototype on **90 nm** technology, which will allow to reduce pixel size to **25μ x 25μ**

- We agreed to have **small fraction** of the electronics **inside pixel** to have **PMOS** transistors. Though it will reduce charge collection efficiency, but will **simplify comparator** design. It is very **difficult** to build good comparator with **low power** consumption on **NMOS only** transistors.

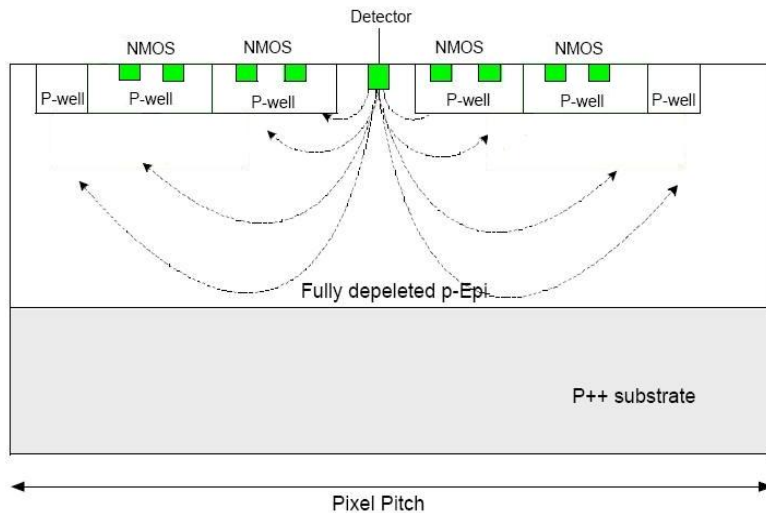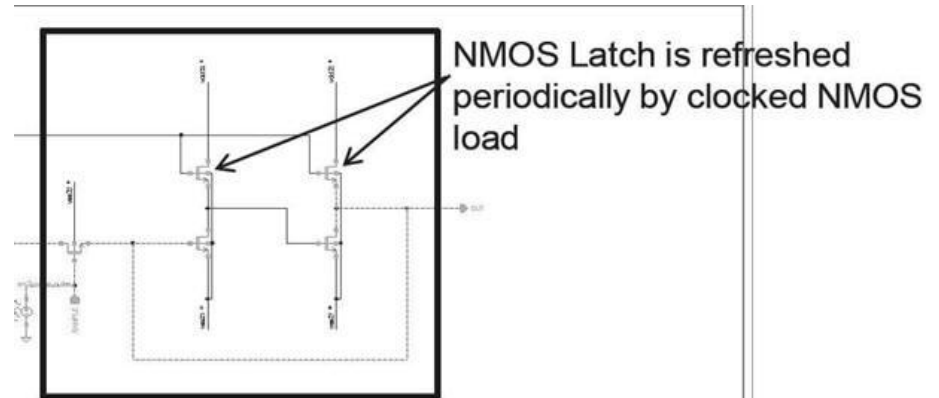NMOS   NMOS   Detector   NMOS   NMOS

P-well | P-well | P-well | P-well | P-well | P-well | P-well

Fully depleted p-Epi

P++ substrate

Pixel Pitch

Figure 11.1   Proposed pixel architecture

NMOS Latch is refreshed periodically by clocked NMOS load

Clocked Dynamic NMOS Latch is a very efficient memory element. NMOS inverters and NOR gates can also be clocked to save on static power consumption.
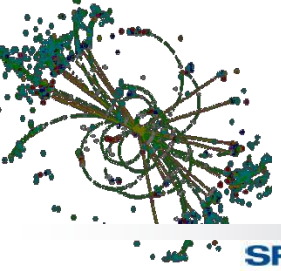
Proposed dynamic latch (memory cell) has technical problem in achieving very low power consumption. The problem is in the fact, that NMOS loads can't have very low current in conducting state – lower practical limit is 3-5µA. This necessitate in the use of very short pulses for refreshing to keep power within specified limit. However, we have suggested solution to this problem, which allows to reduce average current to required value without need for short pulses.
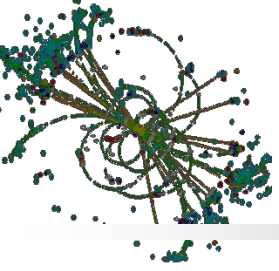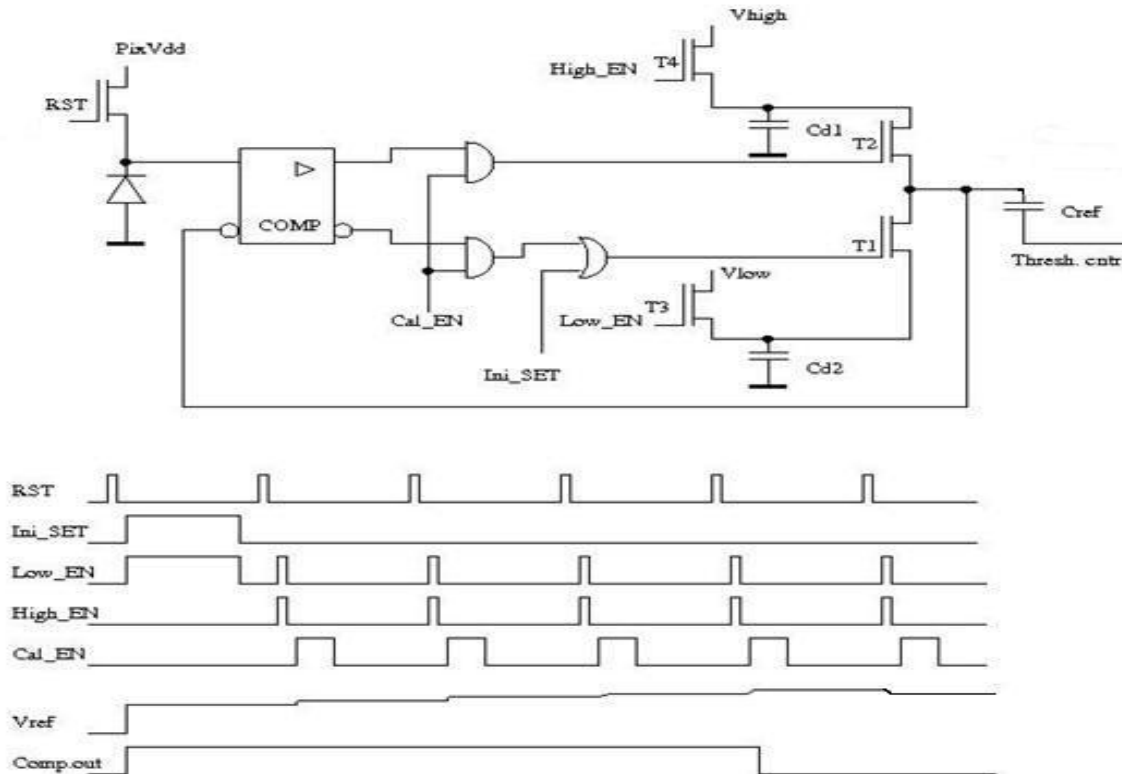
- Next idea was to replace calibration circuit from digital where offset is kept as a state of calibration register with analog circuit in which offset is kept as a voltage on a capacitor. This eliminates the problem of the limited by number of bits in calibration register range of offsets circuit is able to compensate. Sarnoff engineer farther simplified this schematics by eliminating part of circuit connected to inverting output of comparator.
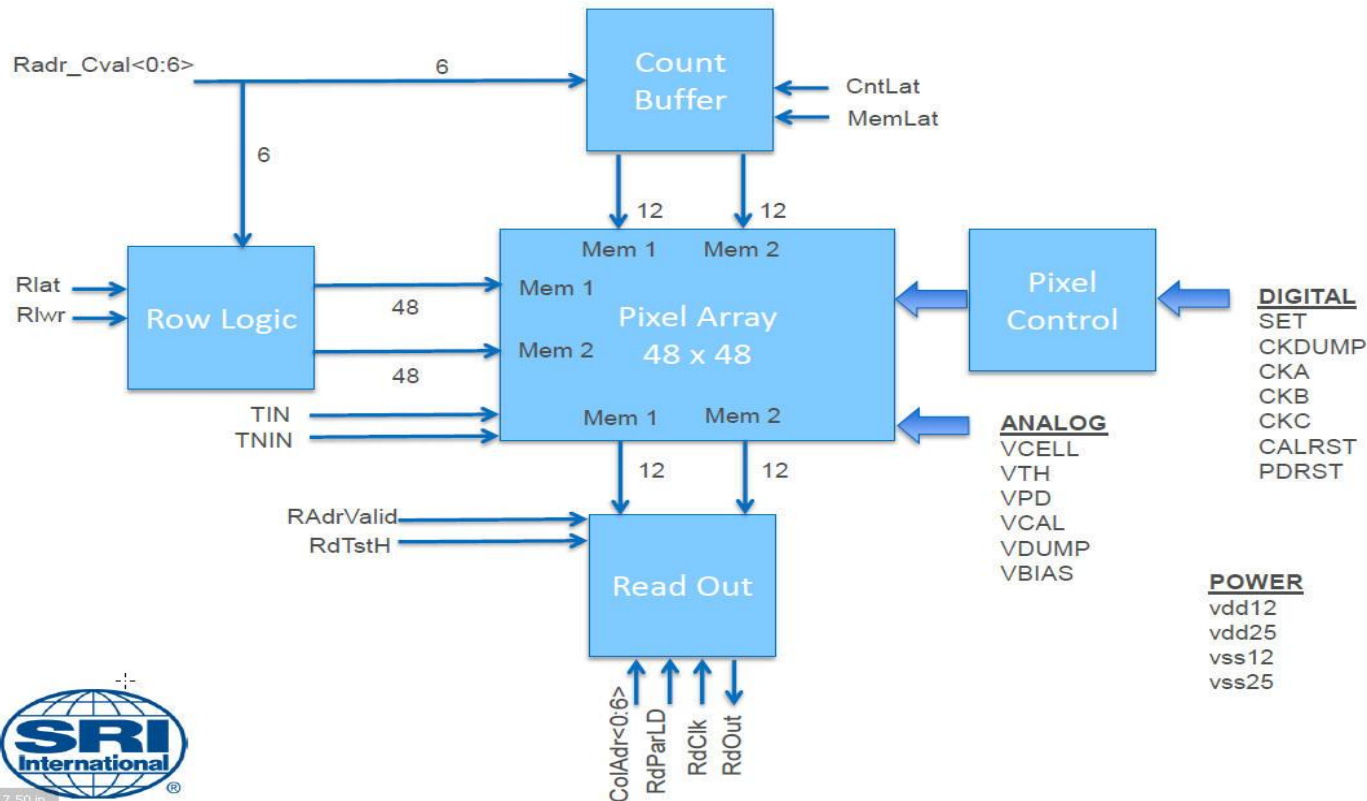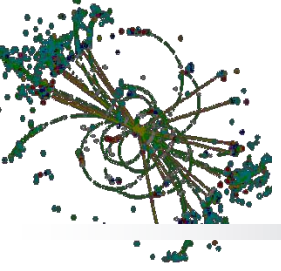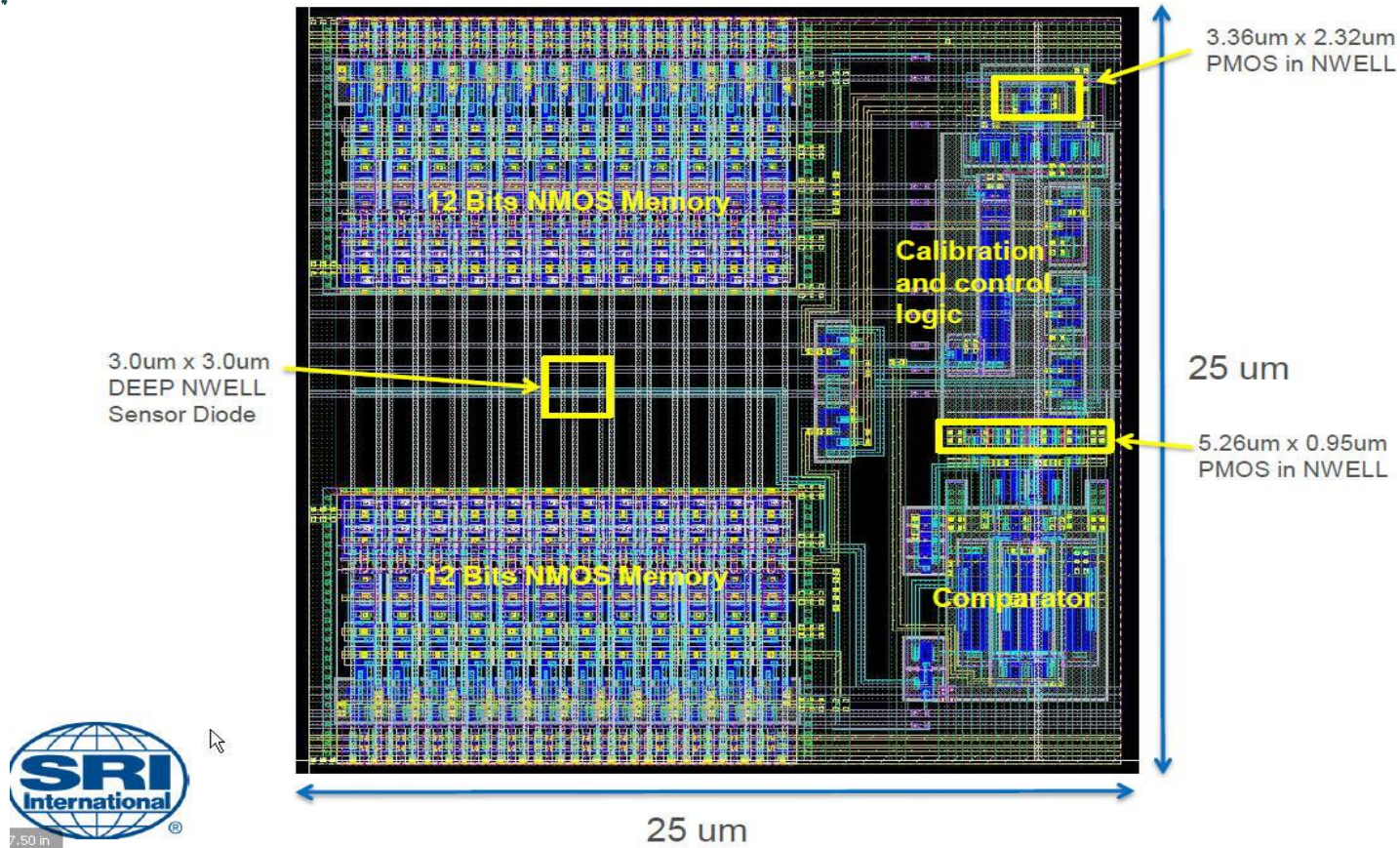
Prototype 2 chip

Chronopixel 2 Block Diagram Detail

Radr_Cval<0:6> — 6 → **Count Buffer** ← CntLat, MemLat

6 →

Row Logic — Rlat, Rlwr

48 → Mem 1
48 → Mem 2

Pixel Array 48 x 48 — Mem 1 / Mem 2 (top), Mem 1 / Mem 2 (bottom)

12, 12 (top)
12, 12 (bottom)

TIN, TNIN →

Pixel Control ← DIGITAL

DIGITAL
SET
CKDUMP
CKA
CKB
CKC
CALRST
PDRST

ANALOG
VCELL
VTH
VPD
VCAL
VDUMP
VBIAS

POWER
vdd12
vdd25
vss12
vss25

Read Out — RAdrValid, RdTstH

ColAdr<0:6>, RdParLD, RdClk, RdOut

One of the **technical problems** was in the **size of the chip** – to make production **cheaper** we agreed to limit chip size to **1.2x1.2 mm^2** . This limits the **number of pads** on the chip to not more than **40**. And that leads to the need of **multiplexing some signals** – for example, **12 bit** time stamp is provided via **6 bit** Radr_Cval **bus** with most significant bits on the high phase of CntLat signal and least significant – on low, with **de-multiplexing** in Count Buffer.

Prototype 2 pixel layout

3.36um x 2.32um
PMOS in NWELL

12 Bits NMOS Memory

Calibration
and control
logic

3.0um x 3.0um
DEEP NWELL
Sensor Diode

25 um

5.26um x 0.95um
PMOS in NWELL

12 Bits NMOS Memory

Comparator

25 um

12

All N-wells (shown by yellow rectangles) are competing for signal charge collection. To increase fraction of charge, collected by signal electrode (DEEP NWELL), half of the pixels have it's size increased to 4x5.5 μ^2 .
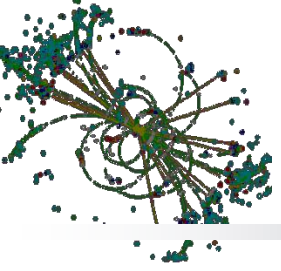
Price for allowing PMOS in pixels

- Because of shorter channels and lower voltage in 90 nm technology, it is very difficult to build comparator with large gain and low power consumption, using only NMOS transistors.

- So, we decided to allow use of PMOS transistors inside pixels, but minimize their use only to comparators.

- It will reduce charge collection efficiency to $S_{se}/(S_{pm}+S_{se})$, where S_{se} is sensor electrode area and S_{pm} is the area of all PMOS transistors in the pixel. We hoped to have the S_{pm} to be around $1\mu^2$. However in the final Sarnoff design this area appeared to be close to $12\ \mu^2$. To reduce noise we want to reduce S_{se} from about $100\ \mu^2$ as it was in the first prototype to something like $25\ \mu^2$.

- From this, we can expect our charge collection efficiency be only about 67.5%.

- However, we need to add width of depleted layer to electrode areas. It will reduce area ratio and reduce charge collection efficiency. But taking into account larger depth of the signal charge collection electrode will increase efficiency.

- Next slides show simulation of prototype 2 performance
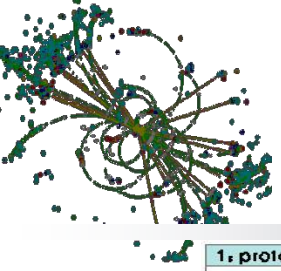
Prototype 2 simulations
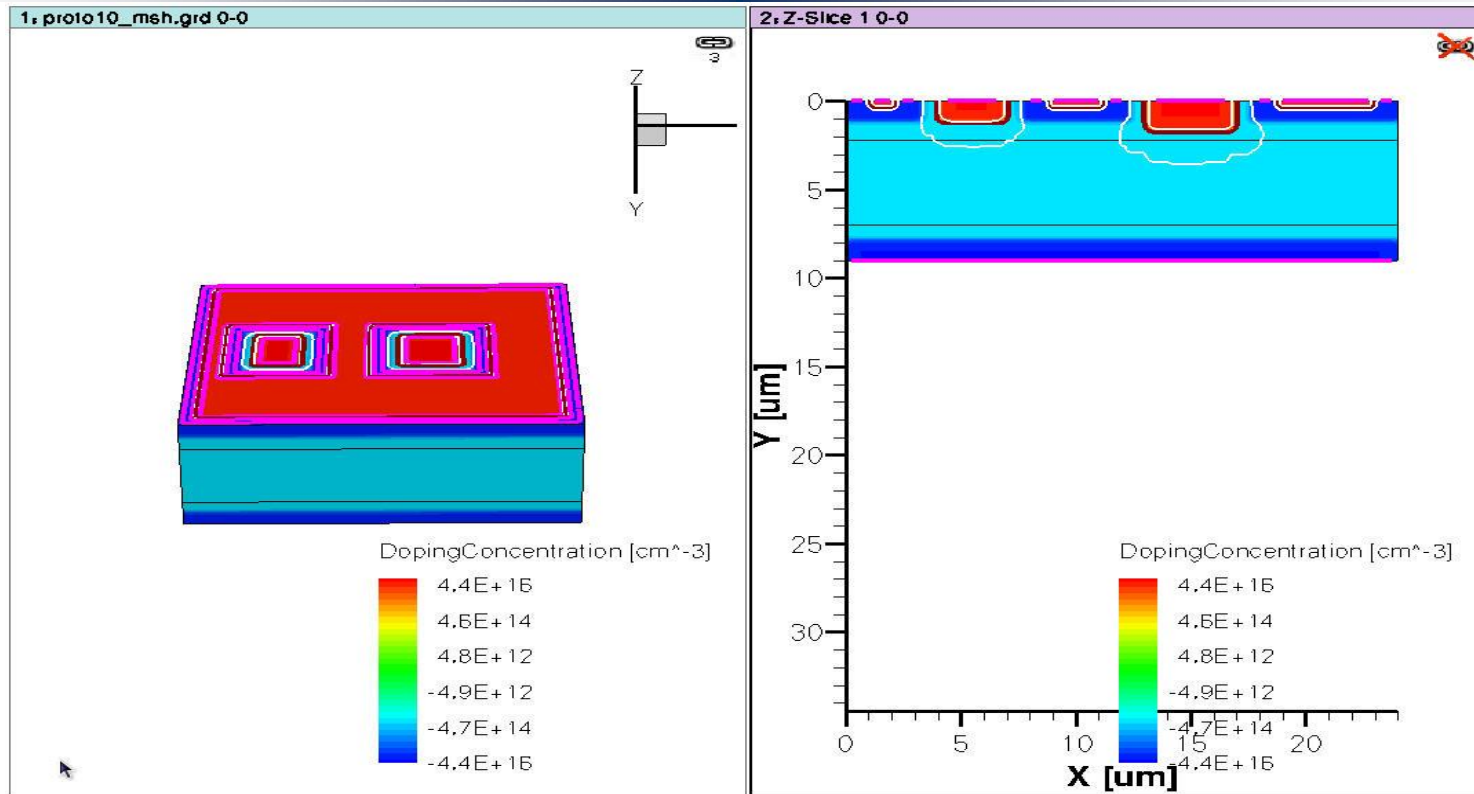
Here you can see **simplified** pixel model I used to **simulate** charge collection.
Large red squire in the center – **signal collecting** electrode, smaller red squire at the
left – **area taken by pmos** transistors, the rest of the red on left picture shows n-wells
of electronics , which are sitting on the **top of p++** doped areas (NMOS transistors).
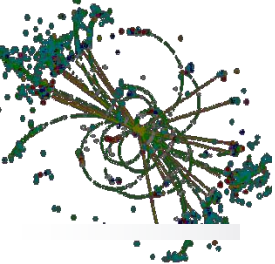White line outlines depleted region.

Prototype 2 simulations
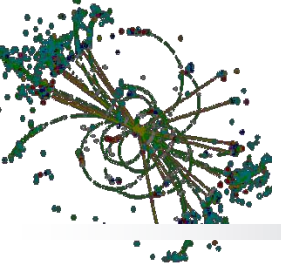
Charge generated by track
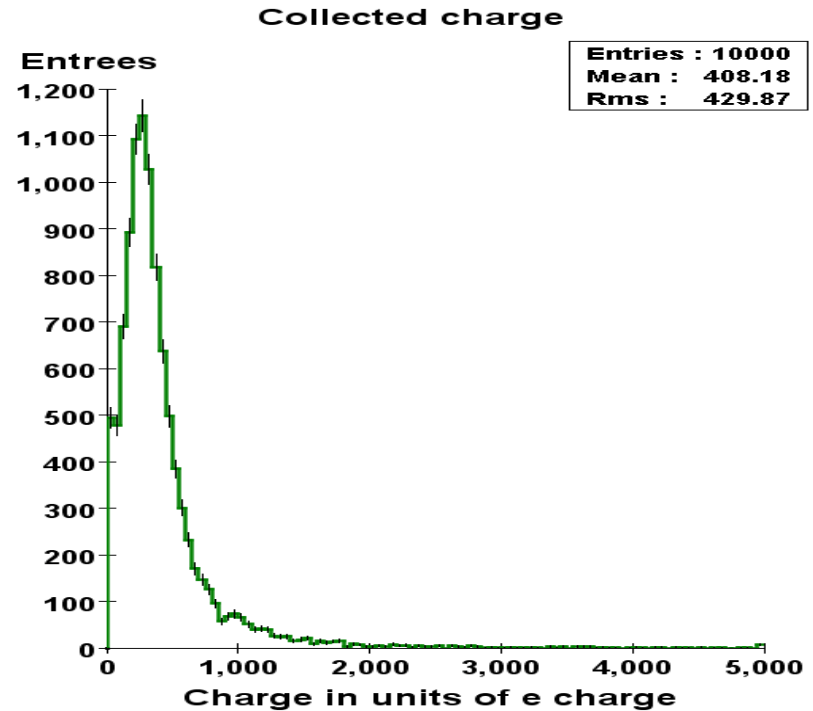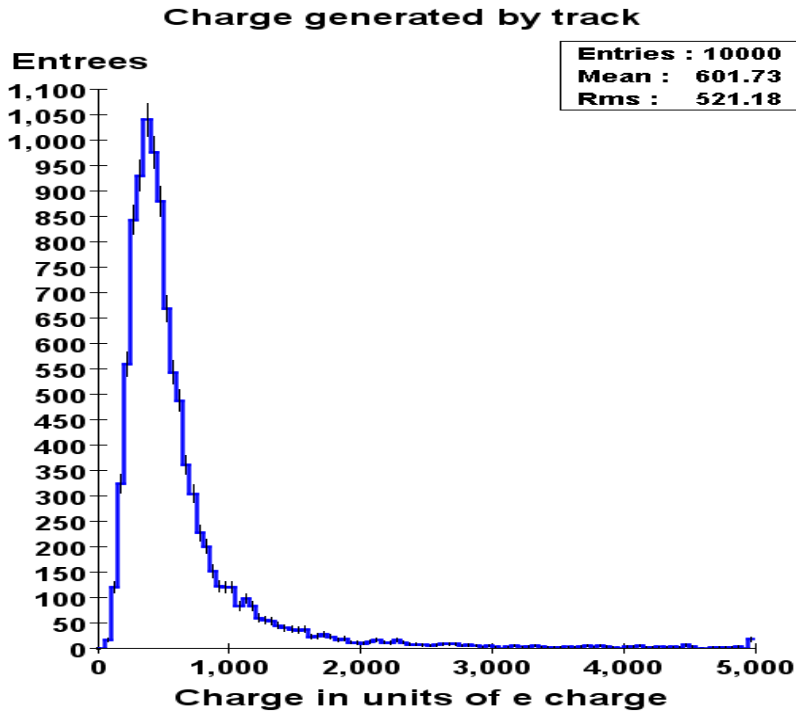
Collected charge

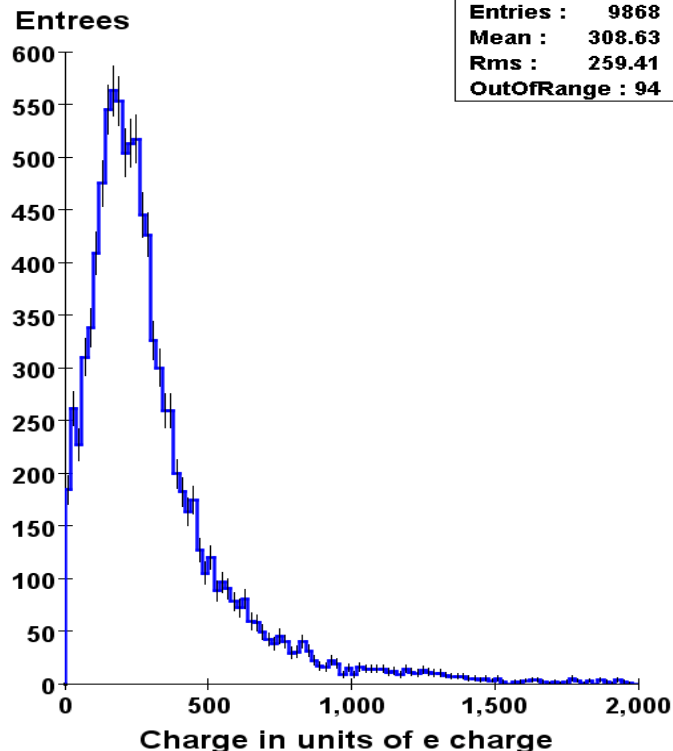Here are **results** of charge collection **simulation.**
On the left is the distribution of number of electron-hole pairs, **generated by track** in the sensor (generated charge). On the left - amount of **collected** by all nearby pixels charge. From the numbers charge collection efficiency is **67.8 %**
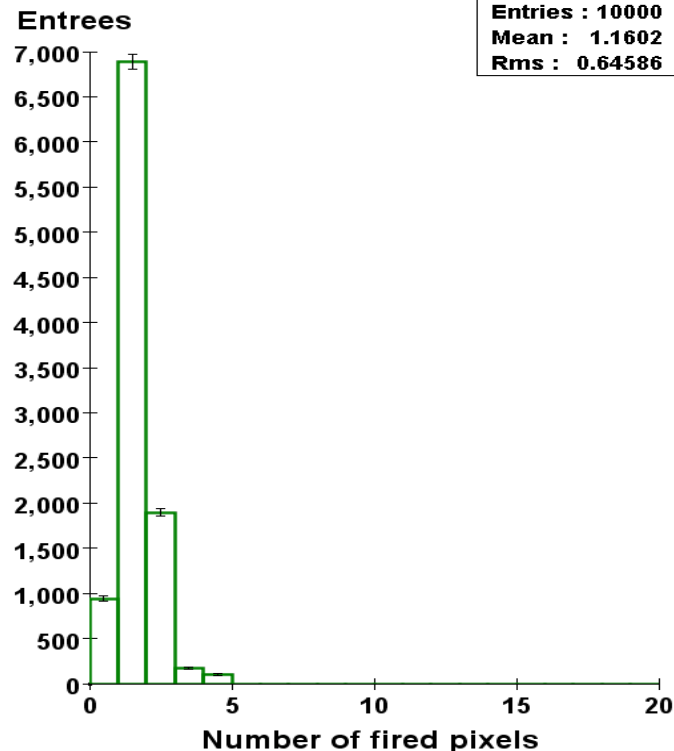
Prototype 2 simulations
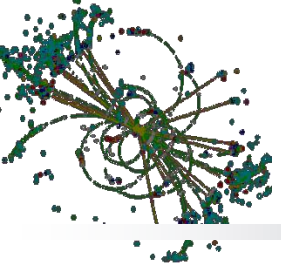

Charge collected by central pixel

Entries :	9868
Mean :	308.63
Rms :	259.41
OutOfRange :	94

Number of pixels above threshold

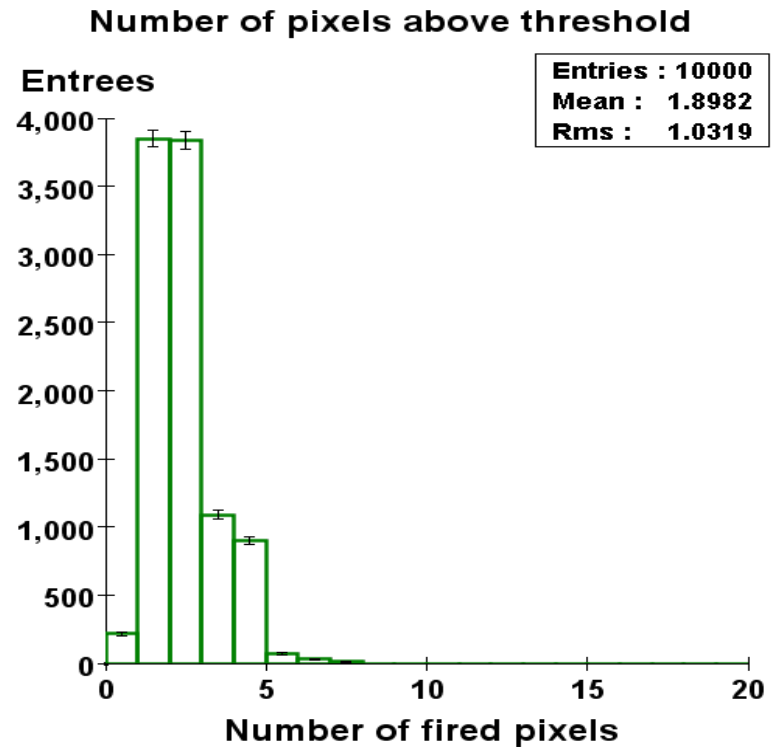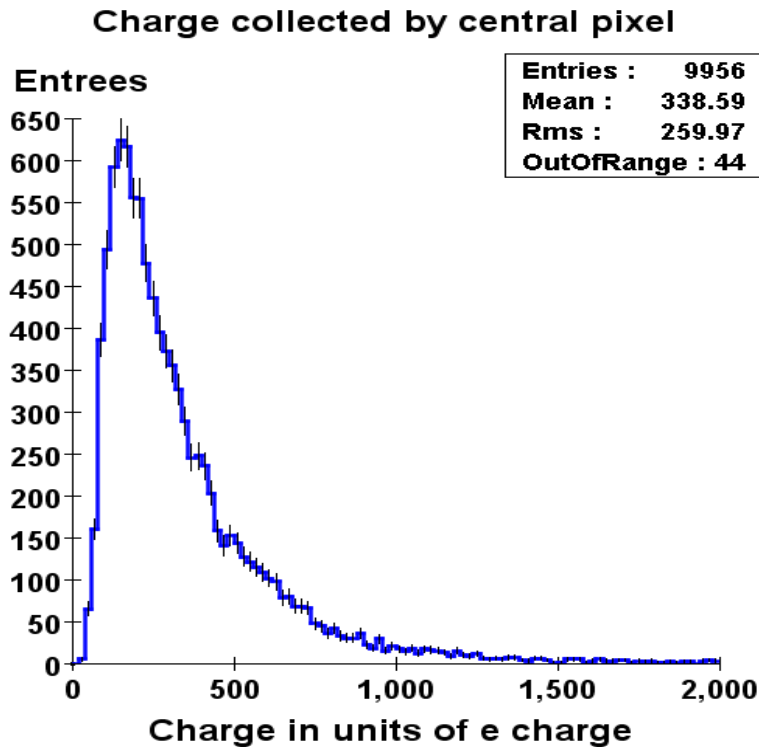| Entries :	10000
Mean :	1.1602
Rms :	0.64586

Here are results of hit **registration efficiency** simulation.
On the left is the distribution of **amount** of charge, collected in the **central pixel** in cluster. On the right - number of **fired pixels** when track passes the sensor with pixel **threshold 75 e**, which is **5 sigma** of noise if its level is **15 e**. Number of events with **0 fired** pixels is about **9%**, so hit registration efficiency is **91%**.

What if we could increase epi thickness?

Charge collected by central pixel

Entries :	9956
Mean :	338.59
Rms :	259.97
OutOfRange :	44

Entrees

Charge in units of e charge

Number of pixels above threshold

Entries :	10000
Mean :	1.8982
Rms :	1.0319

Entrees

Number of fired pixels

Here are results of charge collection simulation for the same design but with **epi layer** thickness of **16 μm** (it was **7 μm** on previous pages – according to expected from manufacturer) .
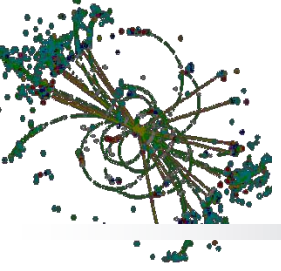On the left is the distribution of **amount of charge**, collected in the **central pixel** in cluster. On the right - **number of fired** pixels when track passes the sensor with pixel threshold **75 e**.
Number of events with **0 fired** pixels is about **2%**, so hit registration efficiency is **98%**.

Pixel variations

○ As soon as Sarnoff design manager gave me **final schematics**, I started **SPICE** simulation of it performance to **double check** their simulations. Suggested by them comparator design **did not pass** my check – it appeared **very sensitive** to the **rise time** of the latch signal. So I insisted that they **use old** (prototype 1) **comparator**, which **did not** have such a problem. But they also **wanted** to **test** their **new** design as they believed that with **additional** latch signal **shaping** it should work and it have **better switching** characteristics. So, we agreed to have **half** of the pixels have their **new** design.

○ They wanted to have **charge collection** electrode only **3x3 μ²** to have **low noise** level. However, with **12 μ²** of PMOS transistors in the pixel would lead to charge collection efficiency **less than 50%** . From my calculations of noise and charge collection efficiency the **optimal** (providing **maximum signal/noise** ratio) charge collection electrode should have about **22 μ²** area. So, we decided to have half of the pixels with **9 μ²** charge collection electrode area (to check how much it helps with noise reduction), and half – with **22 μ²** .

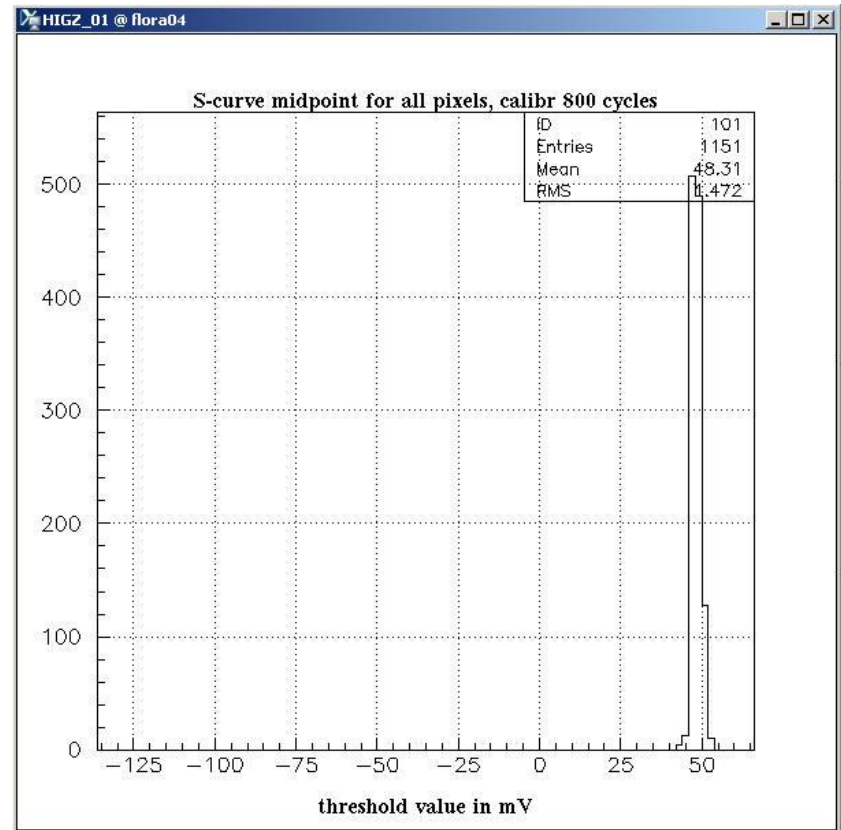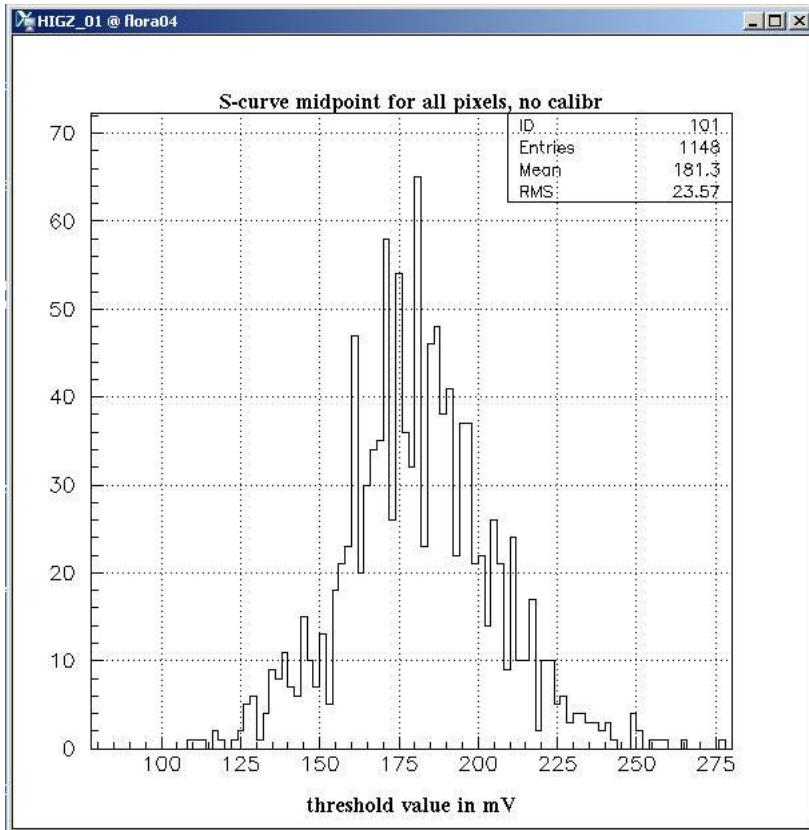○ That leads to **4 different variants** of the pixel, which will be implemented in **each chip**.
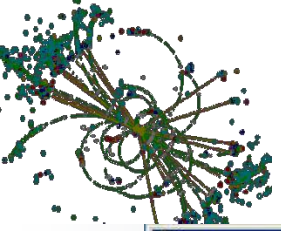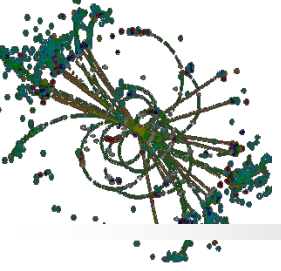
New test stand design

- ○ **New test stand software: completely different waveform generation – driven by dynamic pixel memory (was static in prototype 1).**
- ○ **I have added build-in logical analyzer to FPGA code to enhance debugging ability. New test stand is fully operational right now.**
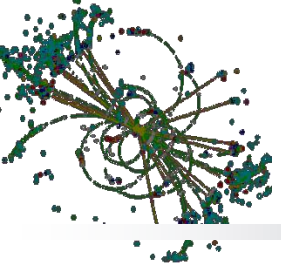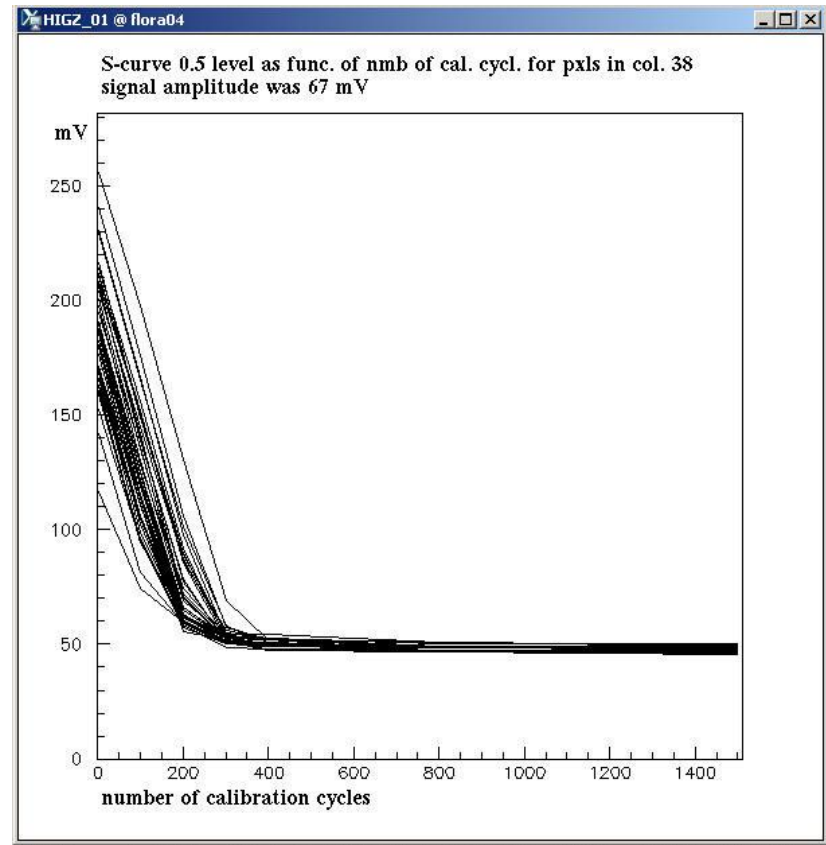
Preliminary test results - calibration

I have used 67 mV pulse to get S-curves – probability of comparator be fired as function of threshold. Without calibration comparator offsets were set to values that all comparators are in fired state at 0 threshold. Calibration changes offsets to the point when comparators flip to non-fired state.
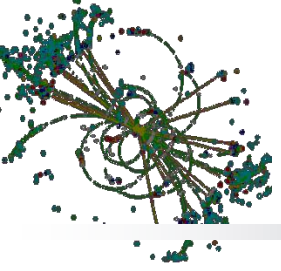
○ **Here you can see how comparator offsets are changing during calibration. Each calibration cycle can change offset by less than 1 mV. So, pixels, which had large offsets initially need more cycles to get to the state when comparators are not fired, which stops calibration process. Each cycle can be as short as bunch crossing interval – 0.3 μs, so calibration can be completed in about 150 μs. The threshold offset is stored on capacitor of about 1 pF, and does not change by more than 1 mV during entire bunch train (1 mS).**
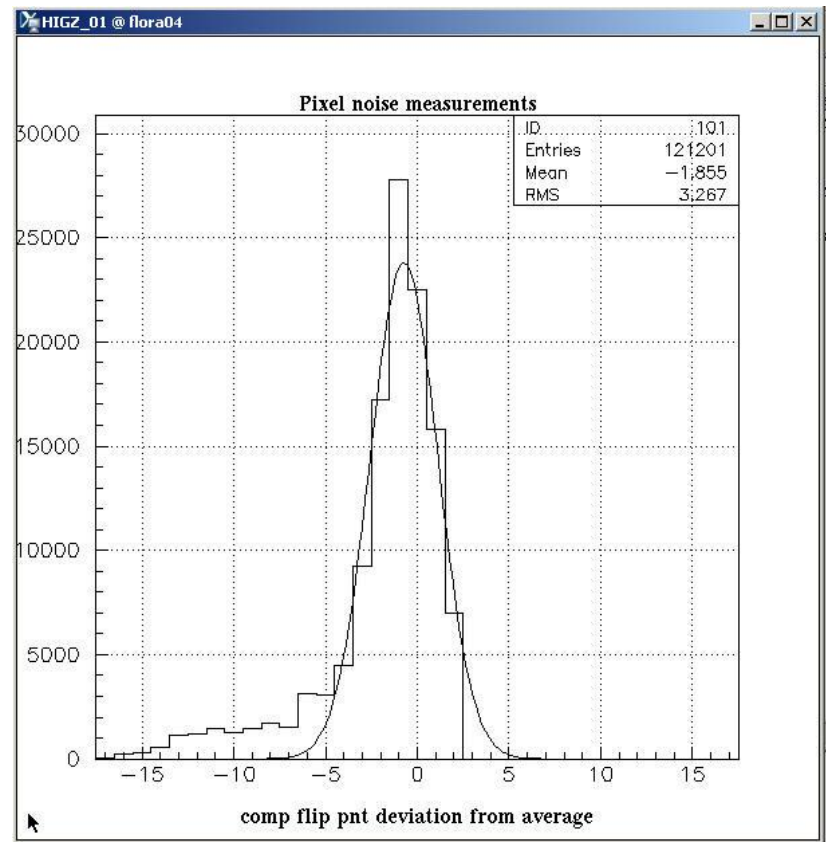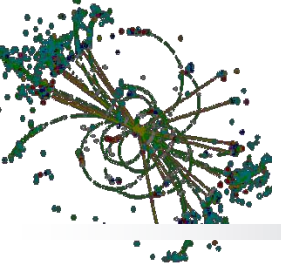
○ **Noise distribution looks very peculiar – what is the source of long tail to the left? Can't it explain calibration results – difference between signal amplitude 67mV and threshold, need to be applied to get 50% registration efficiency ~50 mV (should correspond to distribution peak). Because during calibration offset can change only in one direction, noise tail will push it to the end of the tail. Actually, this may be caused by test stand, not by the chronopixel chip**


HIGZ_01 @ flora04

Pixel noise measurements

ID	101
Entries	121201
Mean	−1.855
RMS	3.267

comp flip pnt deviation from average

○ **Test with Fe55 is not understood yet. Picture on the right shows number of hits per pixel, exceeding some threshold. Left 12 columns have smaller sensor size – 9 μm² , right 12 columns – larger size (~20 μm²) . So, left pixels have smaller capacitance, and should have larger signal – it seems in agreement with this picture. But signal value (about 50 mV for all pixels) indicate that capacitance is much larger than we were expecting (about 5 fF, we expected ~1.5 fF). It need to be investigated farther. Actually, I need higher activity source. With what I had it took many hours to get such picture.**
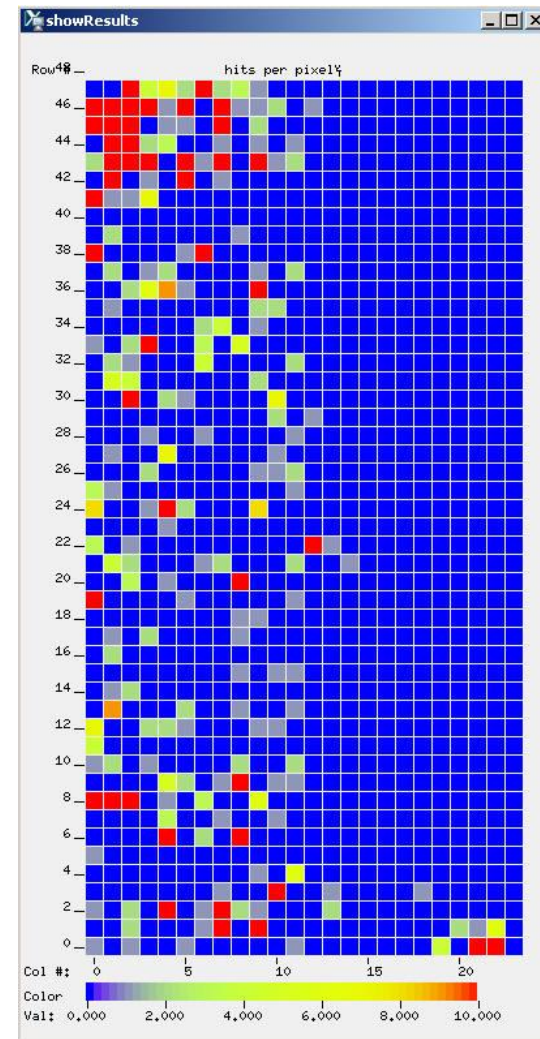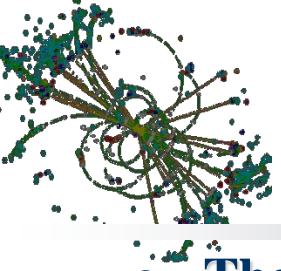
Conclusions

○ **There were 3 major questions to answer with prototype 2 :**

  ↪ **1. Is it possible to make all NMOS electronics inside pixel with acceptable power consumption?**

   ❖ Test have shown that this is possible. All NMOS memory is working fine and consuming power not much higher than CMOS memory.

  ↪ **2. Can we replace digital calibration circuit for compensating comparator offsets with analog circuit? Can analog circuit hold offset value with required precision long enough time (1 ms)?**

   ❖ Test have confirmed that analog calibration works and that voltage on calibration capacitor does not change by more than 1 mV in 1 ms (meets requirements).

  ↪ **3. Is charge collection in the pixel with all NMOS electronics high enough to allow making sensors without deep p-well ?**

   ❖ We do not have answer yet. Notice, that presented here results are VERY PRELIMINARY.
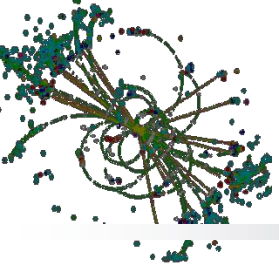
Future plans

○ **If our observation that sensor has larger than expected capacitance (about 5 fF instead of expected 1.5 fF) will be confirmed, we may want to increase epi layer resistivity and thickness. Unfortunately, no foundry employing 90 or 65 nm technology can do this. So we may need to go back to 180 nm, keeping all other prototype 2 features. This will make working high efficiency sensor, but pixel size will be 50x50 μm^2. Though it will not meet requirement on pixel size, it will show the way to follow.**

○ **Another option – go to smaller feature size (65 or 45 nm) to have required pixel size and prove that everything works as expected, hoping to find suitable manufacturer for higher silicon resistivity and thicker epi layer later, as more money will be available**