Minutes of WP-meeting 156

Attendance:
DESY: Szymon Bugiel, Ralf Diener, Isa Heinze, Leif Jönsson, Klaus Zenker
Webex: Gilles De Lentdecker, Philippe Gros, Jochen Kaminski, Martin Killenberg, Dan Peterson, Akira Sugiyama, Ron Settles, Jan Timmermans

PCMAG/LP setup, test beam:
Ralf: LP

- There has been not much progress in the work on the LP nor on the test beam area, since the responsible technician was sick in the last couple of weeks. Tests to measure the vibrations caused by the cryo-coolers have started. A sensor was placed by the DESY Quality Management department on the LP and measurements will take place from last Tuesday until tomorrow. Results of this test will be presented in one of the upcoming meetings.

Testbeam schedule

- Ralf reported that DESY is working hard on preparing the test beam for next week. They are still confident, that they can place at least one module in the LP and start data taking on the 20^{th}. He reminded that also the ECAL would like to place a part of their detector in the PCMAC to make a short test beam in September or October.

News from the groups:
Ralf: All the pad planes have been equipped with connectors and have been tested and glued to the backframes. A first complete module has been finished last Monday, but during the final HV test a short developed in one sector and the GEM has to be replaced by one originally assigned to a different module. The last two spare GEMs are being glued to the frame currently. However, there are not many GEMs left, since several of them had to be sent back to the CERN workshop for additional cleaning and are not expected back before the test beam. Therefore, it is not clear, if all 3 modules can be used as planned.

Philippe reported on some ideas on a wire grid: Since a satisfactory performance of a GEM gating device has not been demonstrated yet, a viable solution for the DBD is necessary. Therefore, Philippe suggested a radial arrangement of gating wires, which would be much simpler to integrate in the modules and which would minimize the dead area, since the support frame could be limited to the upper and lower arc, which is used for HV contacts anyway. Disadvantageous could be the non-parallelism of the wires, which creates radial fields that do not vanish at larger drift distances, and possible angular dependence. These effects were discussed in the following: To estimate the effect of non-parallel wires Philippe calculated the radial electrical field deviation E_r by using a model with infinitely long wires, that are at the same potential as parallel wires. The field distortion, however, is smaller by at least a factor of 10^{-3} than the drift field and, therefore, the effects can be neglected. Additionally, realistic boundary conditions would reduce the effect even further. Next the effects on the electron displacement were discussed. The LCTPC will be operated in a high $\omega\tau$ environment, where electrons will follow more the magnetic field lines than the electric ones. In this context, it helps to reduce the perpendicular deviation from the wire and, therefore, reduces the opacity of the grid down to the optical limit given by $2\times R_{wire}/\text{spacing} \sim 1\%$. Also, hardly any influence on the spatial resolution in the direction perpendicular to the wire is expected giving further benefit to the radial arrangement of the wires. The deviations along the wires could be somewhat larger and have to be tested experimentally. Finally the effect on tracks with a high p_T was discussed. Such a track could be

completely absorbed by a wire. Since it was shown, that the high $\omega\tau$ reduces the effect perpendicular to the wire, the charge of the track should be diffused less that $2\times R_{wire}$, which is possible only for very short drift distances (O(cm)).
Besides, the modules are staggered and a track which is partially covered on one module would be uncovered on the next one degrading the momentum resolution only minimally. The effect on the dE/dx- measurement could be significantly more difficult to evaluate. Finally, two different closing configurations of the gate were discussed.: (1) a single voltage operation, where the voltage is raised so much, that the electric field between the wire gate and the gas amplification stage is inverted and the ions drift back to the GEM/MM, where they are neutralized. This configuration is simpler to implement, but needs higher voltages and puts more mechanical strain on the wires, since they repulse each other. The (2)nd approach would be similar to ALEPH, where a smaller voltage difference was applied to the neighboring wires and ions were thus guided towards one set of wires to be neutralized there. This would require lower voltages, but an extra HV-line. The voltages needed in both settings depend on the spacing between the wires, which should be maximized to reduce the mechanical stress.

Philippe discussed in a second presentation also some ideas on the 2-phase CO_2 cooling of the sALTRO-16 module. Due to the central arrangement of the 25 MCMs there is some space left on the sides for cooling. The current design of the MCMs foresees a 3 mm spacing between the padplane and the MCM as well as between the MCM and the FPGA carrier. A first approach foresees cooling pipes at the left and right side of the modules with for example one pipe guided first on the lower level directly on the padplane and then being bent by 180° it can be guided on the next level between the MCMs and the FPGAs. In this way the number of connections could be minimized and placed on one side of the module leaving enough space for HV-connections on the other side. In both levels sheets of a material with good heat conductivity such as TPG could be placed to transport the heat from the chips to the cooling pipes. This setup was simulated with a software program called CRADLE and it was shown, that the heat gradient due to the different distance to the cooling pipes is too high and that the central chips are overheated if no power pulsing is used. Two solutions were suggested by Philippe: An additional cooling pipe could be mounted on the lower TPG plane to increase the cooling power. This pipe could also be integrated in the heat conducting plane. There would be enough space to implement this additional pipes by moving the MCMs outward by a few mm. Simulations show, that a temperature below 50°C could be guaranteed then, but the temperature of the padplane will still vary by 10 K. The general feeling of the audience was, that is might not be sufficient and a more homogeneous temperature would be preferable. In this case a larger gap between the padplane and the MCM is necessary to use a thicker TPG plane and increase the heat transport. This could be reached by carving those areas of the padplane where the TPG will be placed, or elevating the padplane, where the limiting connectors will be placed. Both options are not very attractive, since they are very costly and influence the stability of the padplane. In September KEK will get some samples of the TPG, from which they will build test module with dummy chips to verify the simulations and learn how to contact the material and the heat pipes.

AOB:
The next workpackage meeting will take place on August 30th.