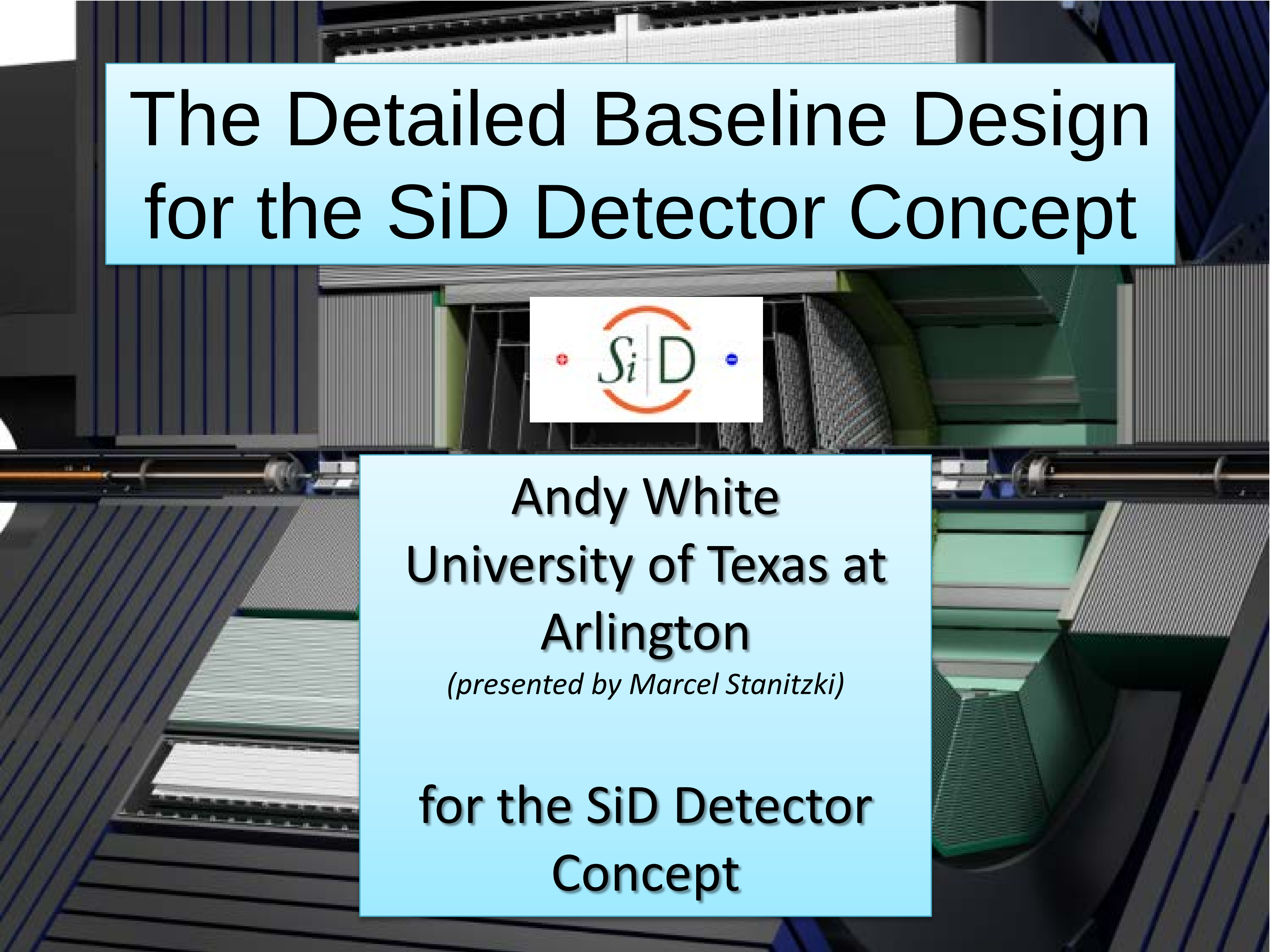


The Detailed Baseline Design for the SiD Detector Concept

Andy White
University of Texas at Arlington
(presented by Marcel Stanitzki)

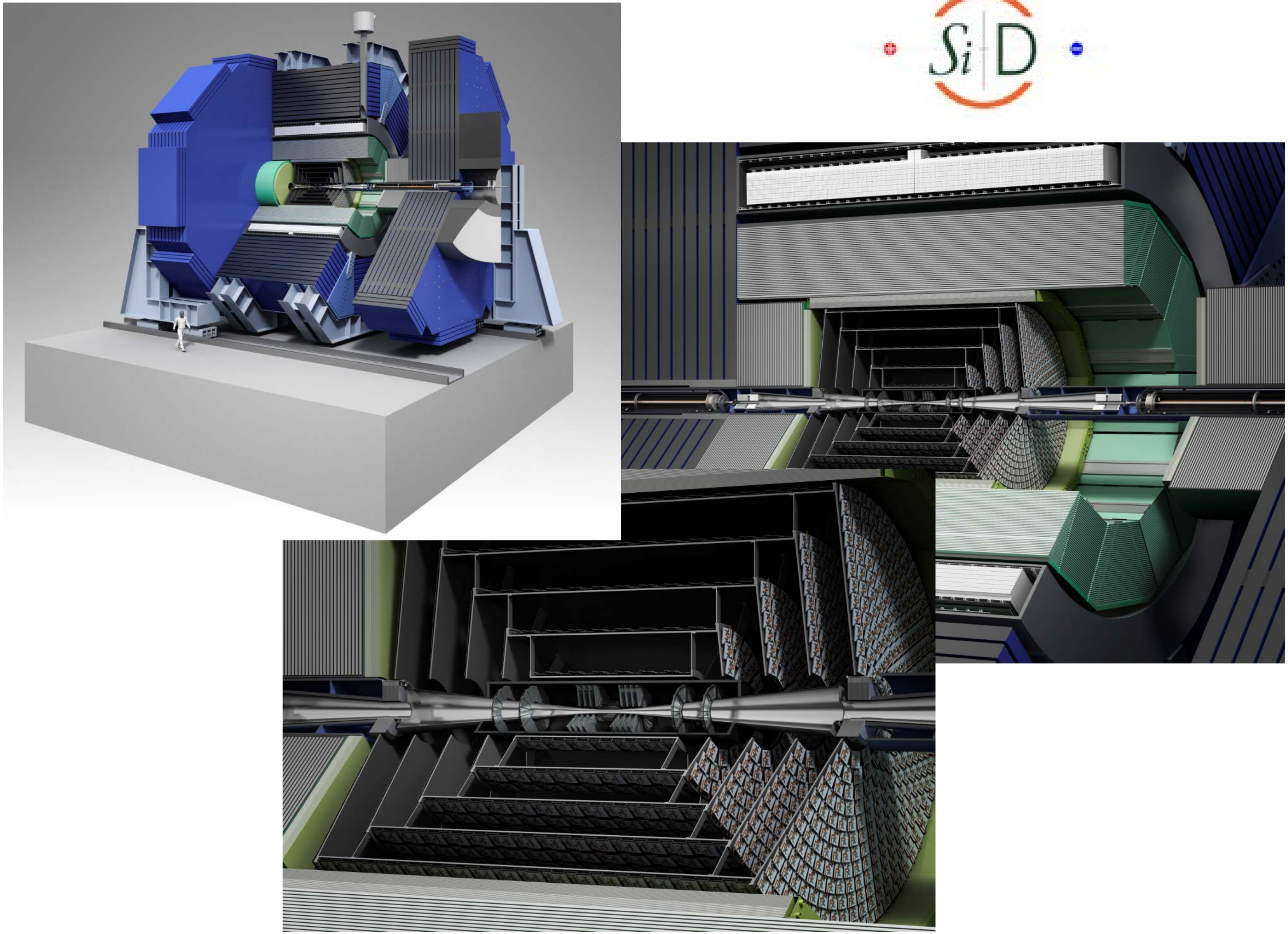
for the SiD Detector Concept

Outline

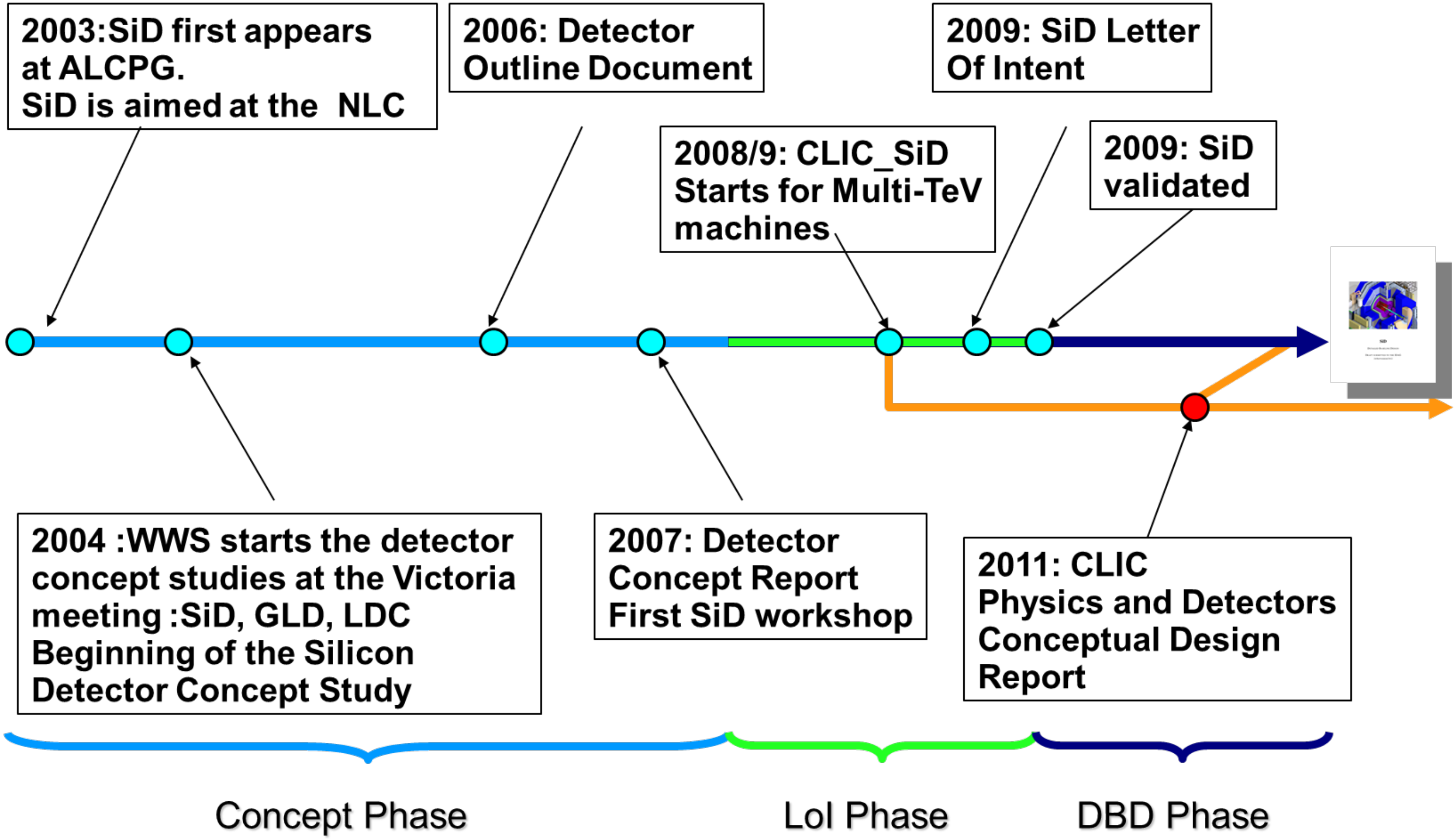
- Introduction
  - Detector design
  - Design Study Organization
  - DBD Editors
- Areas of SiD included in DBD
  - summary for detector components
- Simulation/reconstruction, PFA, Benchmarking
  - see next talk by Tim Barklow
- SiD Costing
- Summary
- This is a short talk about a large design study – summarize main features of SiD, current status, and a word about the future.

SiD Detector overview

- SID Rationale
  - *A compact, cost-constrained detector designed to make precision measurements and be sensitive to a wide range of new phenomena*
- Design choices
  - Compact design with 5 T field.
  - Robust all-silicon vertexing and tracking system with excellent momentum resolution
  - Time-stamping for single bunch crossings.
  - Highly granular Calorimetry optimized for Particle Flow
  - Iron flux return/muon identifier is part of the SiD self-shielding
  - Detector is designed for rapid push-pull operation



SiD Detailed Baseline Design



2003:SiD first appears at ALCPG.
SiD is aimed at the NLC

2006: Detector Outline Document

2009: SiD Letter Of Intent

2008/9: CLIC_SiD Starts for Multi-TeV machines

2009: SiD validated

2004 :WWS starts the detector concept studies at the Victoria meeting :SiD, GLD, LDC
Beginning of the Silicon Detector Concept Study

2007: Detector Concept Report
First SiD workshop

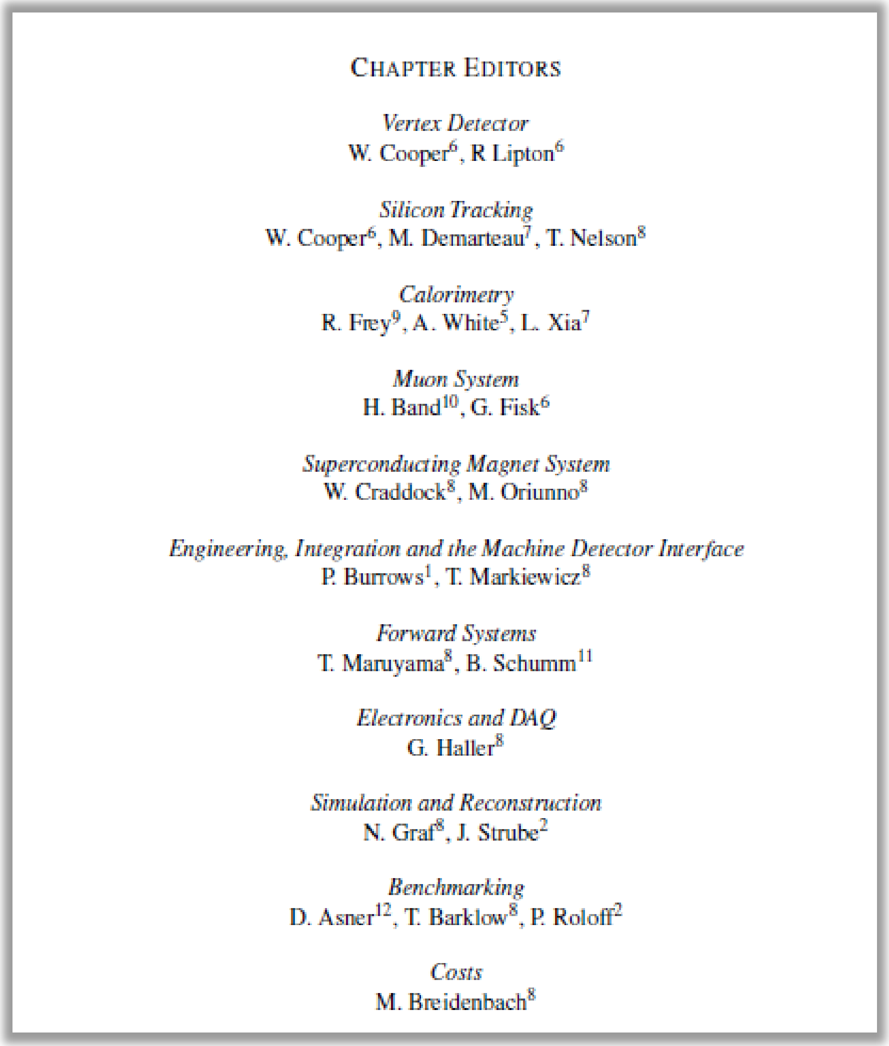
2011: CLIC Physics and Detectors Conceptual Design Report

Marcel Stanitzki, LCWS 2012

Creating the SiD DBD

Main DBD Editors:

Phil Burrows (Oxford)
Lucie Linssen (CERN)
Mark Oreglia (UChicago)
Marcel Stanitzki (DESY)
Andy White (UTA)



CHAPTER EDITORS

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Costs
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SiD Detailed Baseline Design

- The DBD is a detailed description of a detector design concept, with examples of performance for selected ILC physics processes.

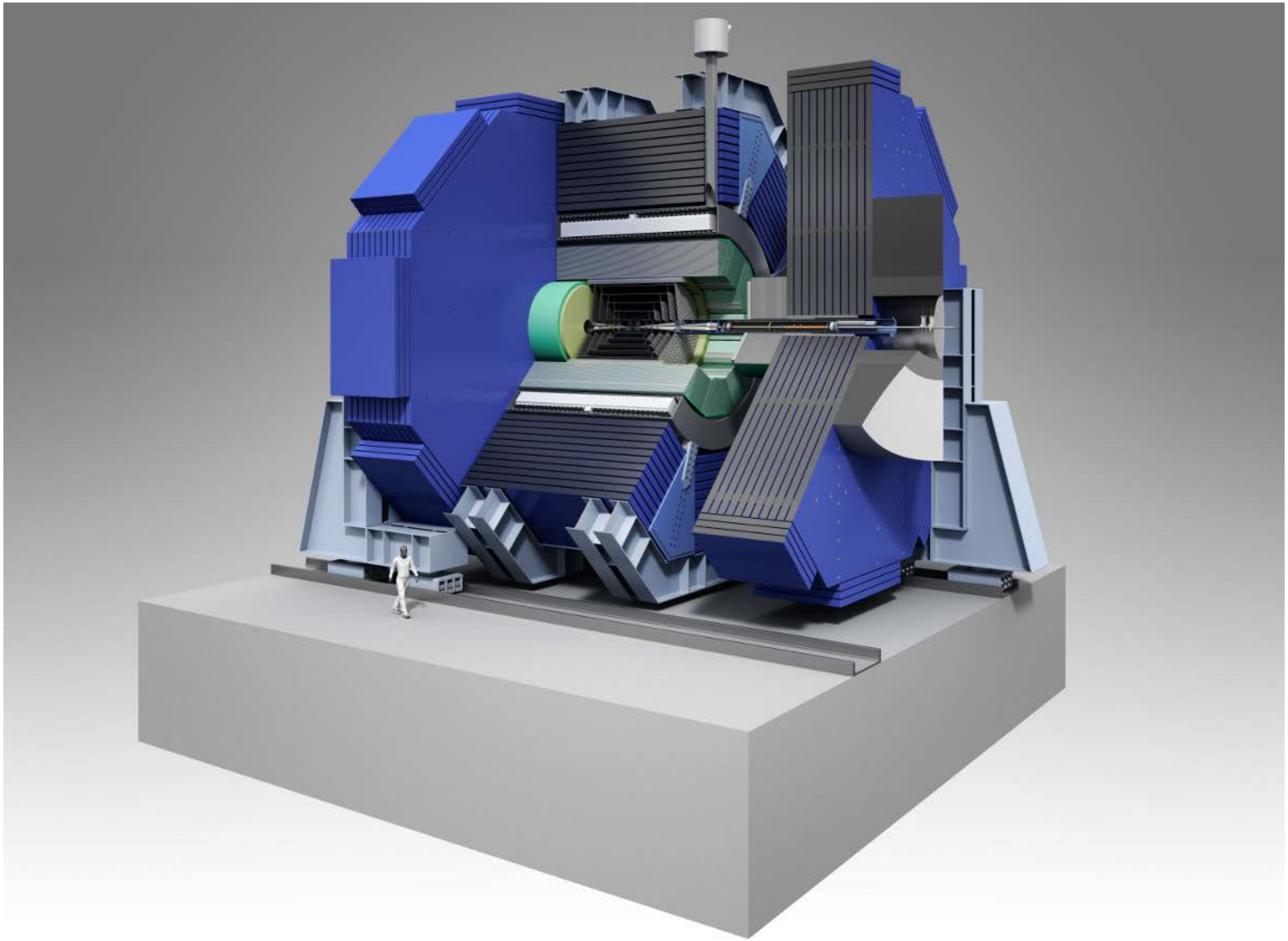
- The DBD is not at the level of a TDR
  - only limited engineering effort was available.

- It includes a large R&D effort, but this is not yet complete.

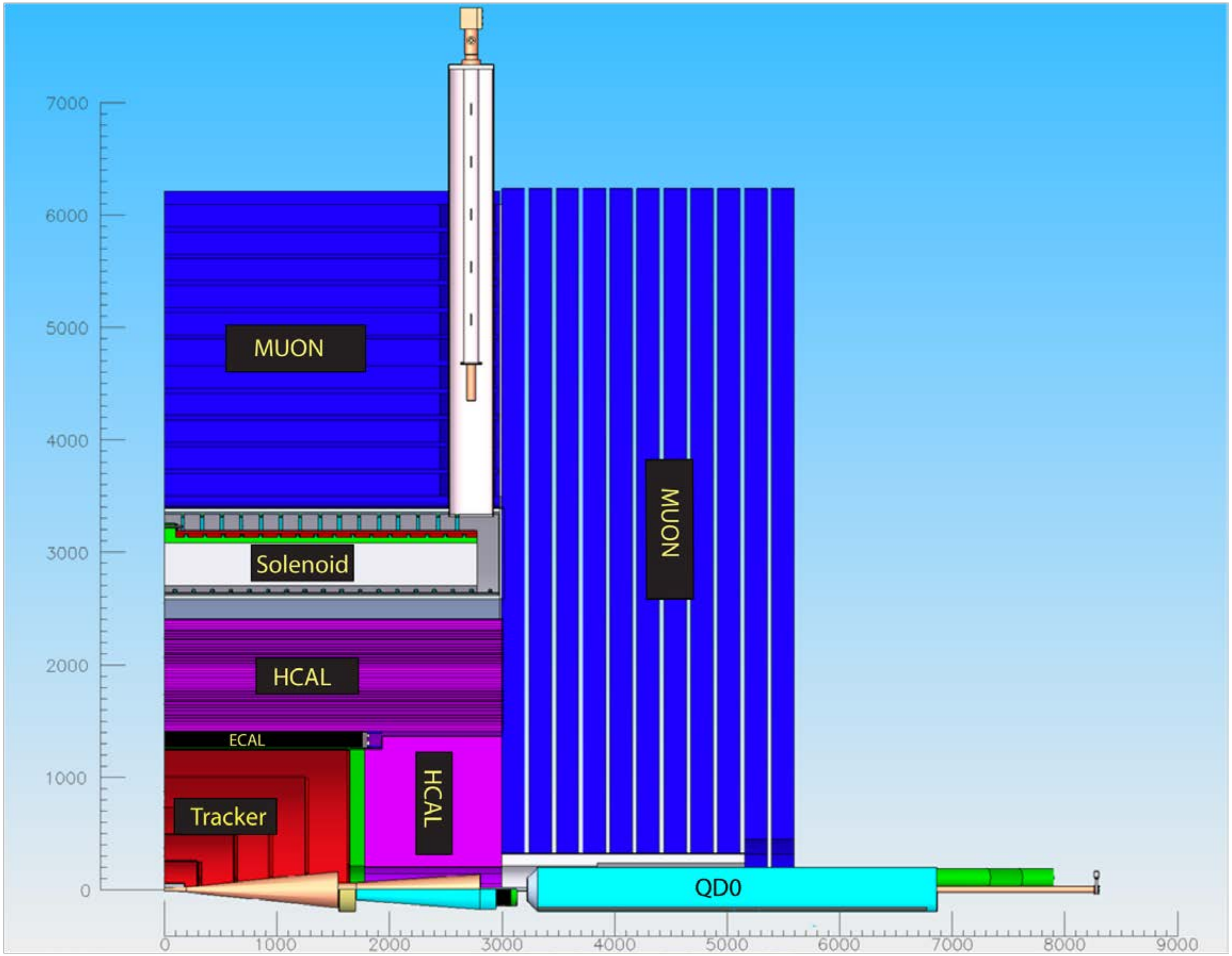
- Baseline choices have been made for all subsystems except the vertex detector; options are also included.

- We provide a full cost evaluation for the detector.

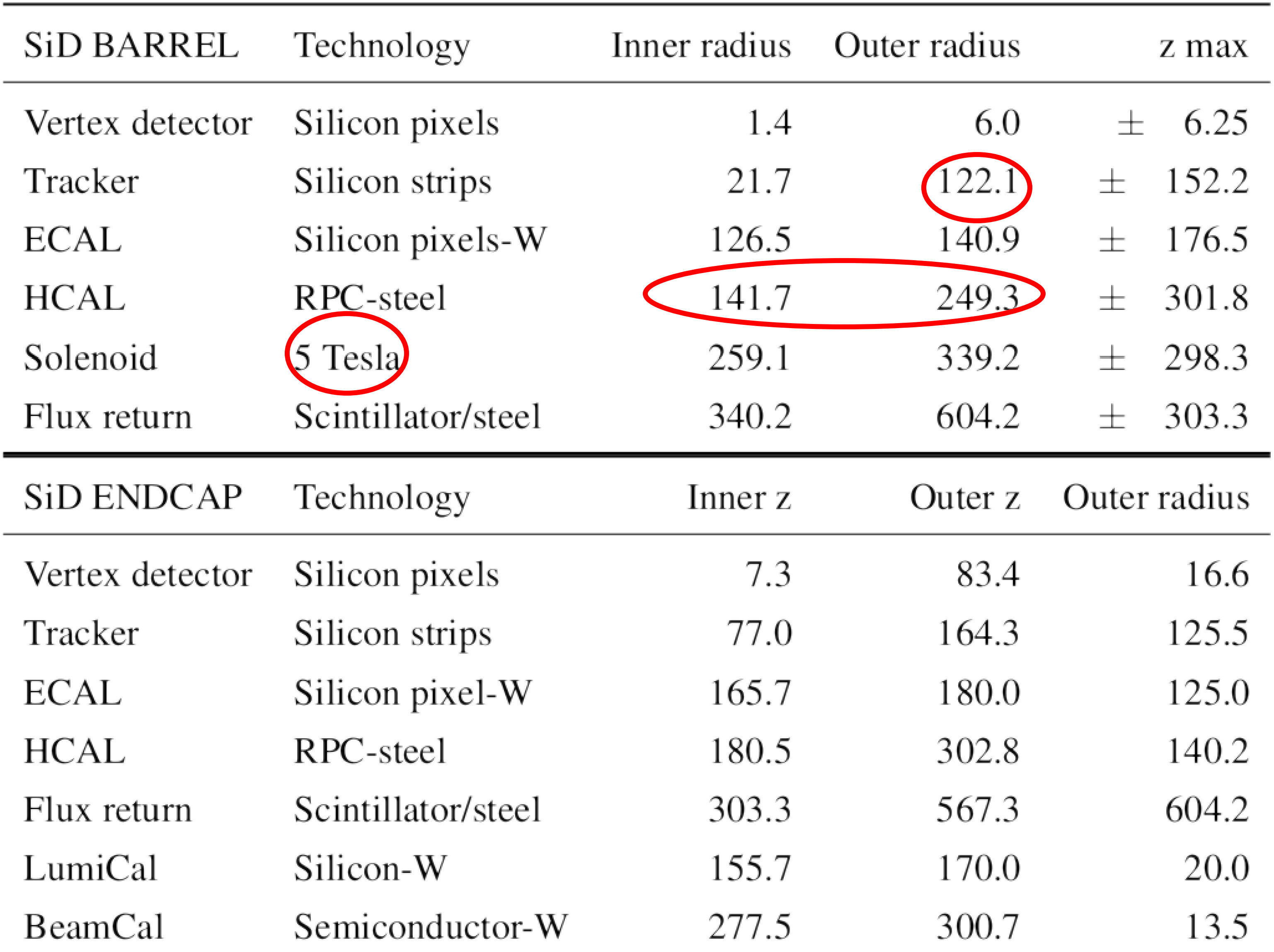
The SiD DBD Detector



The SiD DBD Detector



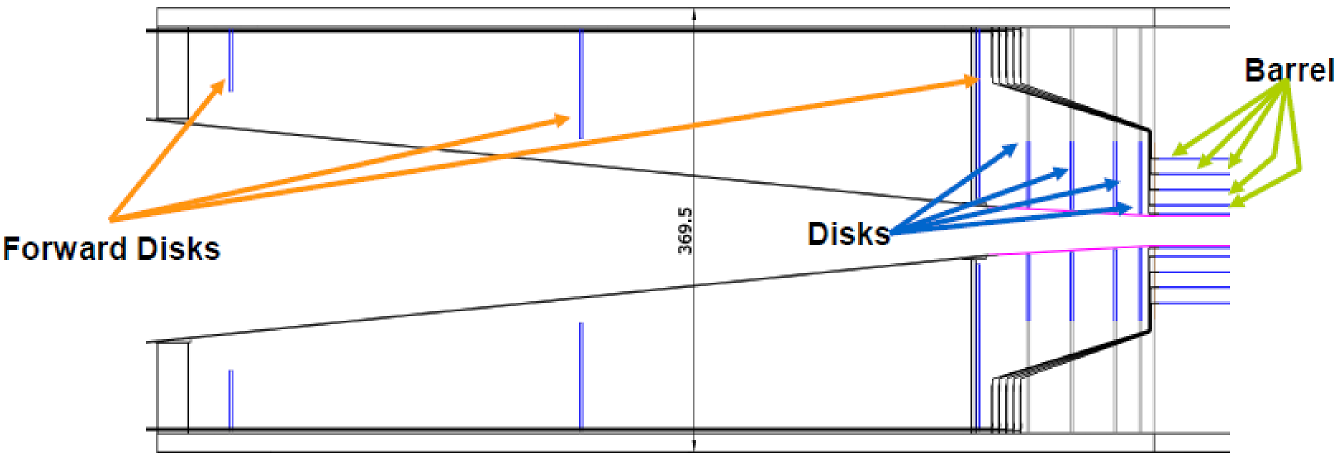
The SiD DBD Detector - parameters

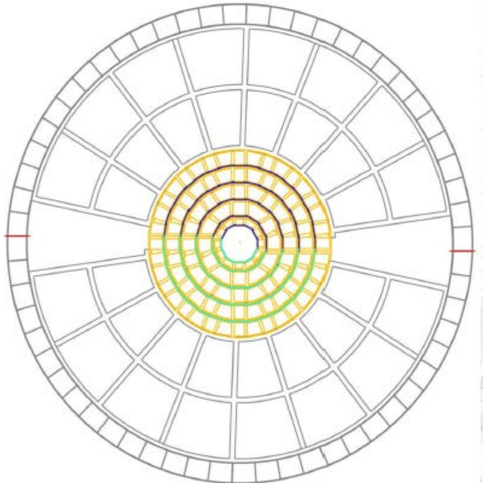


SiD BARREL	Technology	Inner radius	Outer radius	z max
Vertex detector	Silicon pixels	1.4	6.0	± 6.25
Tracker	Silicon strips	21.7	122.1	± 152.2
ECAL	Silicon pixels-W	126.5	140.9	± 176.5
HCAL	RPC-steel	141.7	249.3	± 301.8
Solenoid	5 Tesla	259.1	339.2	± 298.3
Flux return	Scintillator/steel	340.2	604.2	± 303.3

SiD ENDCAP	Technology	Inner z	Outer z	Outer radius
Vertex detector	Silicon pixels	7.3	83.4	16.6
Tracker	Silicon strips	77.0	164.3	125.5
ECAL	Silicon pixel-W	165.7	180.0	125.0
HCAL	RPC-steel	180.5	302.8	140.2
Flux return	Scintillator/steel	303.3	567.3	604.2
LumiCal	Silicon-W	155.7	170.0	20.0
BeamCal	Semiconductor-W	277.5	300.7	13.5

Vertex Detector





Split-cylinder support structures

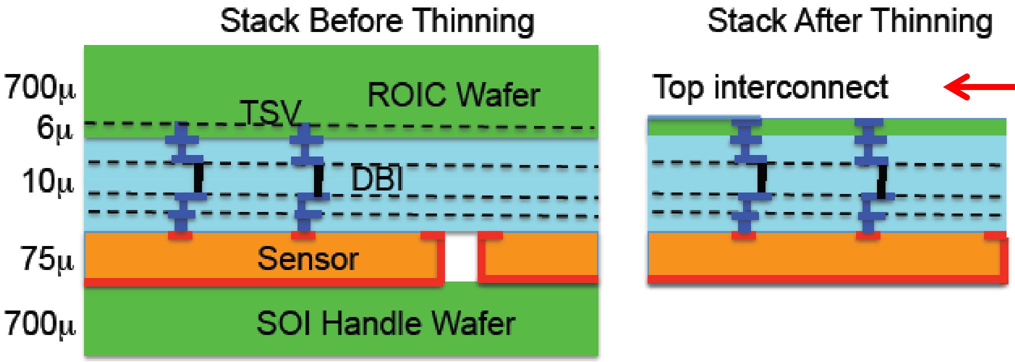
- Requirements
  - $< 5\ \mu m$ hit resolution
  - $\sim 0.1\ \%\ X_0$ per layer
  - $< 130\ \mu W/mm^2$
  - Single bunch timing resolution

- ILC bunch timing and low radiation environment allows very light, low power vertex system
- Pulsed power/DC-DC conversion
- Forced dry air cooling

Vertex Detector

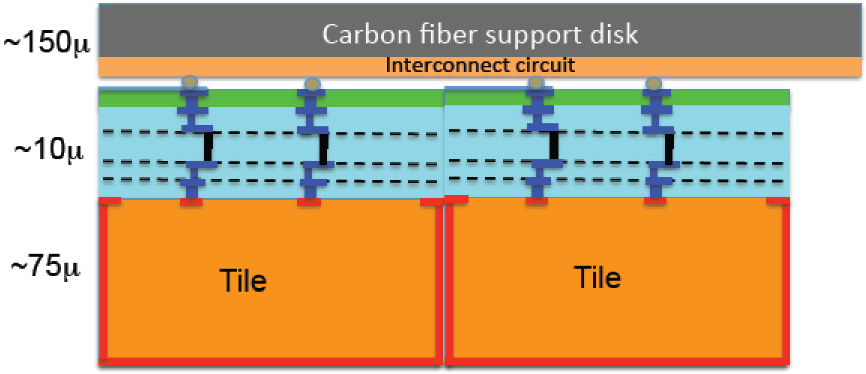
No preferred technology – many choices/still an evolving picture

Example 3-D/active edge design:



Barrel

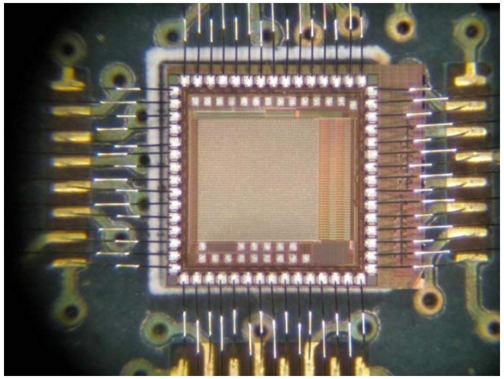
Readout and power connections on top layer



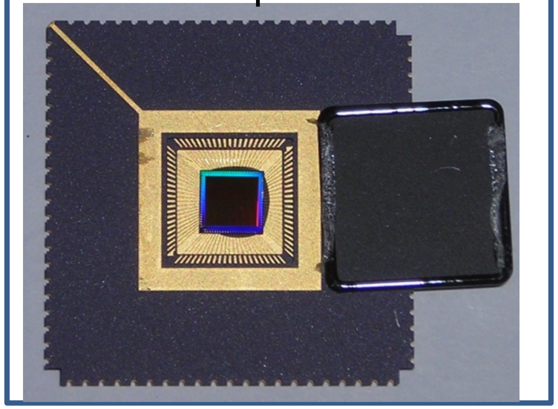
Disk tiling

Vertex Detector – R&D

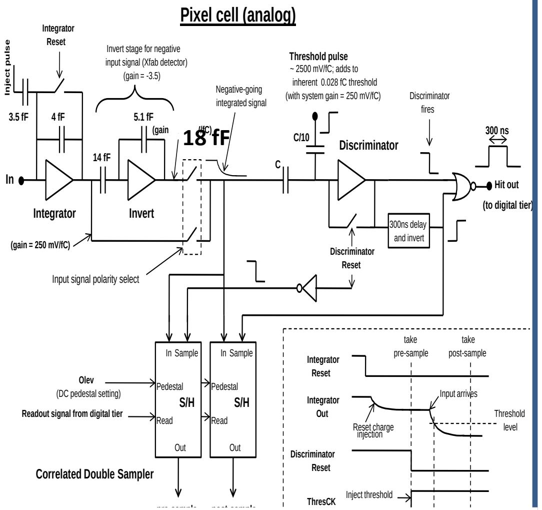
VIP 2a – 3 tier MIT-LL

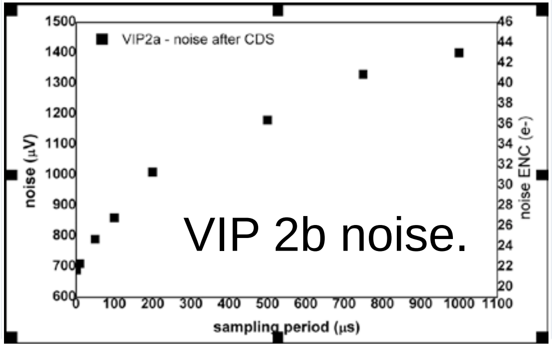


Chronopixel V1



VIP 3D chip





VIP 2b noise.

VIP

- VIP2a (3-tier MIT-LL chip) is produced and tested
- Both analog and digital sections work well, solving problems found in VIP1
- VIP2b (2-Tier Tezzaron/Global foundries) is in process.
- Initial tests of 2D test devices shows good analog performance.
noise = 8e + 0.5 e/ fF
- Sensors for 3D integration of VIP2b produced and tested.

Chronopixel

- Measured noise of 24 e, specification is 25 e.
- Sensitivity measured to be 35.7µV/e, exceeding design spec of 10µV/e.
- Comparator accuracy 3 times worse then spec, need to improve this in prototype 2.
- Sensors leakage currents ($1.8 \cdot 10^{-8}$A/cm^2) is not a problem.
- Readout time satisfactory
- Prototype 2 late 2011, 65nm TSMC

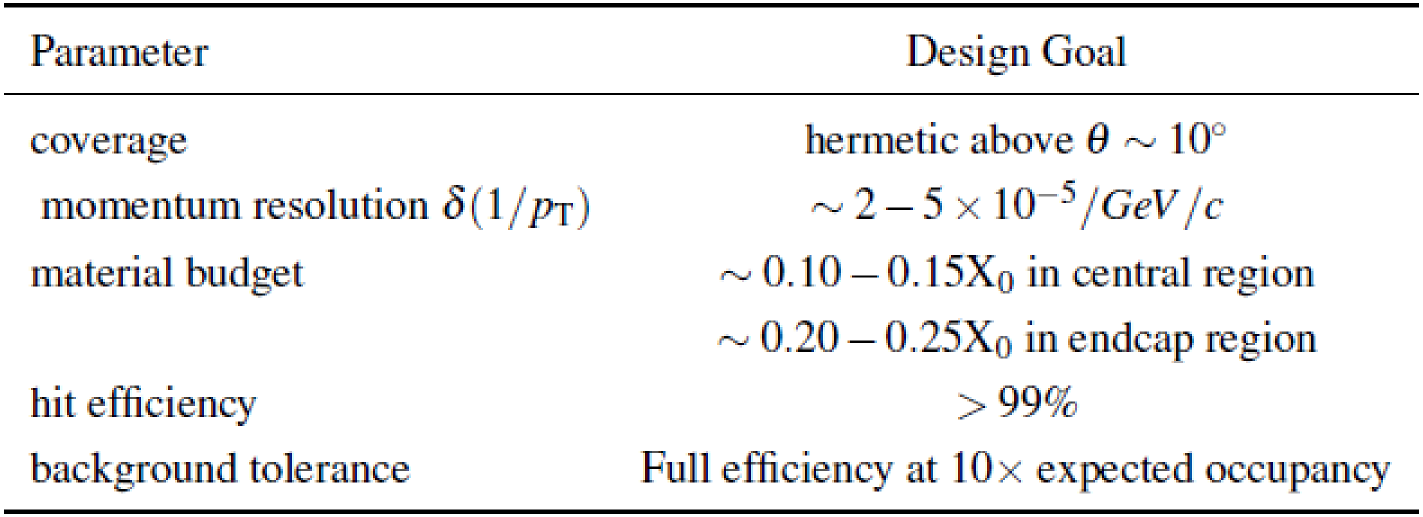
Next: Full sized ladder for barrel, wedge segment for disks, support structures, cooling. power pulsing, cabling.

Silicon Tracking

ILC Physics requires:

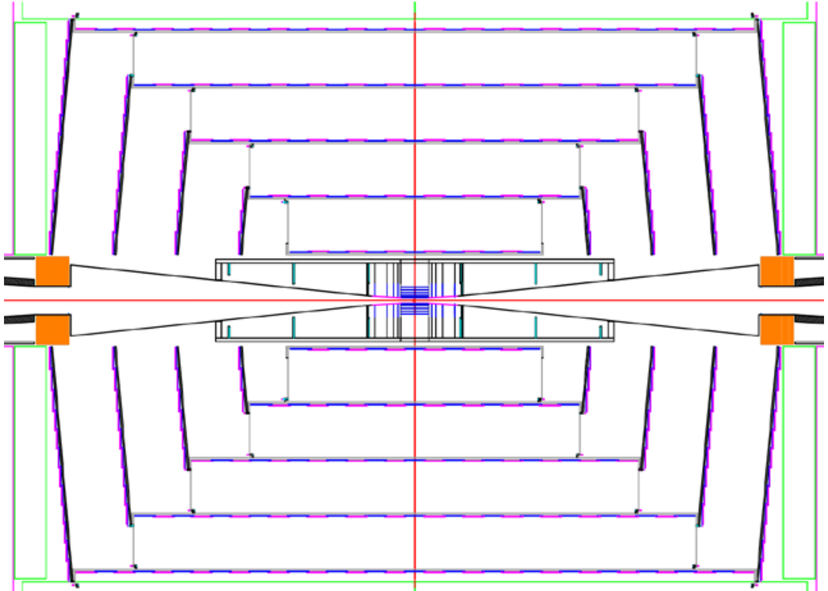
- excellent momentum resolution over wide P_T range
- high point precision, mechanical stability for high P_T
- low material budget for low P_T
- high efficiency for all momenta/angles

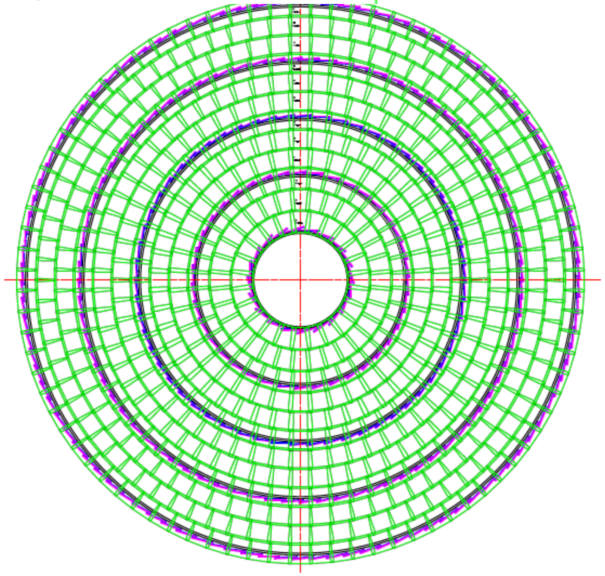
-> Performance goals



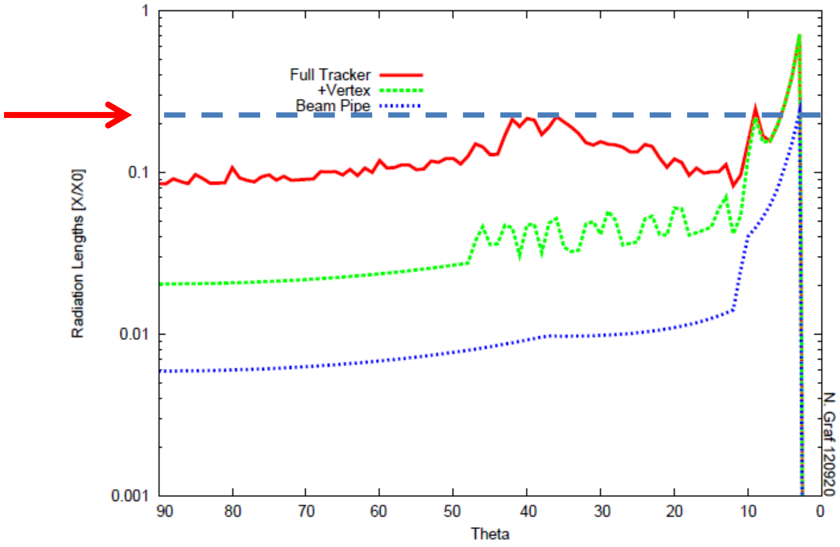
Parameter	Design Goal
coverage	hermetic above $\theta \sim 10^\circ$
momentum resolution $\delta(1/p_T)$	$\sim 2-5\times 10^{-5}/GeV/c$
material budget	$\sim 0.10-0.15X_0$ in central region
	$\sim 0.20-0.25X_0$ in endcap region
hit efficiency	$> 99\%$
background tolerance	Full efficiency at $10\times$ expected occupancy

Silicon Tracking





Below 20% X_0
for whole
VTX/TRK
system

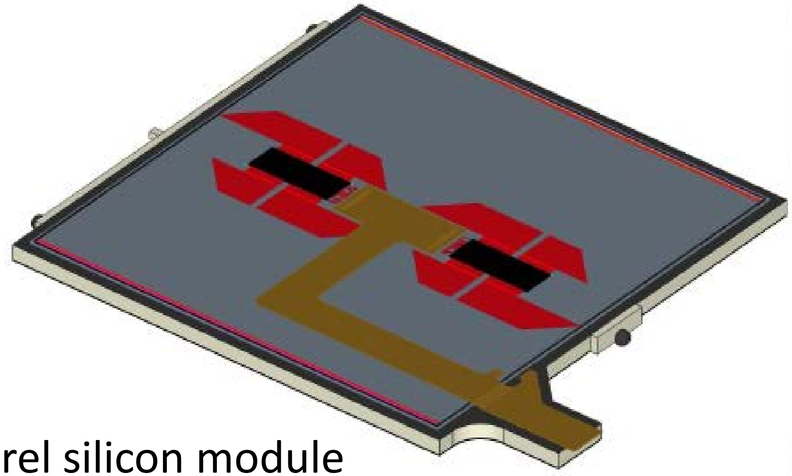


Silicon Tracking

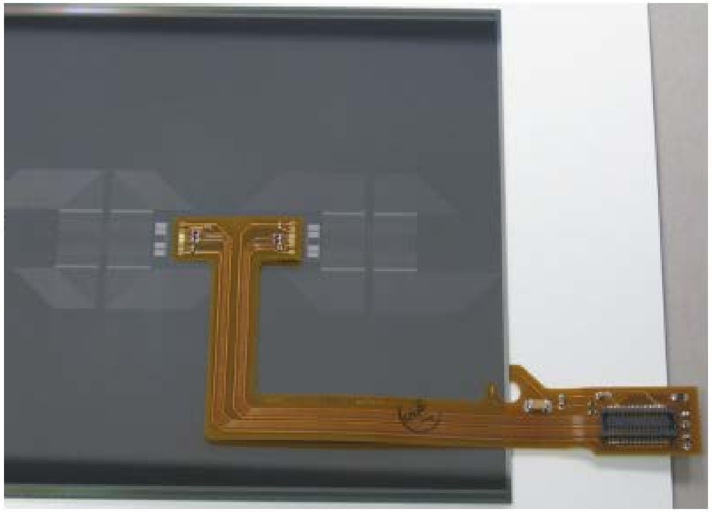
Design features:

- Single-sided silicon micro-strips, double metal layer
- KPiX readout, with time stamping
- Gas cooling
- DC-DC converters supply high instantaneous current

Realization:



Barrel silicon module
300 μm Si, 25(50) μm
sense(readout) pitch

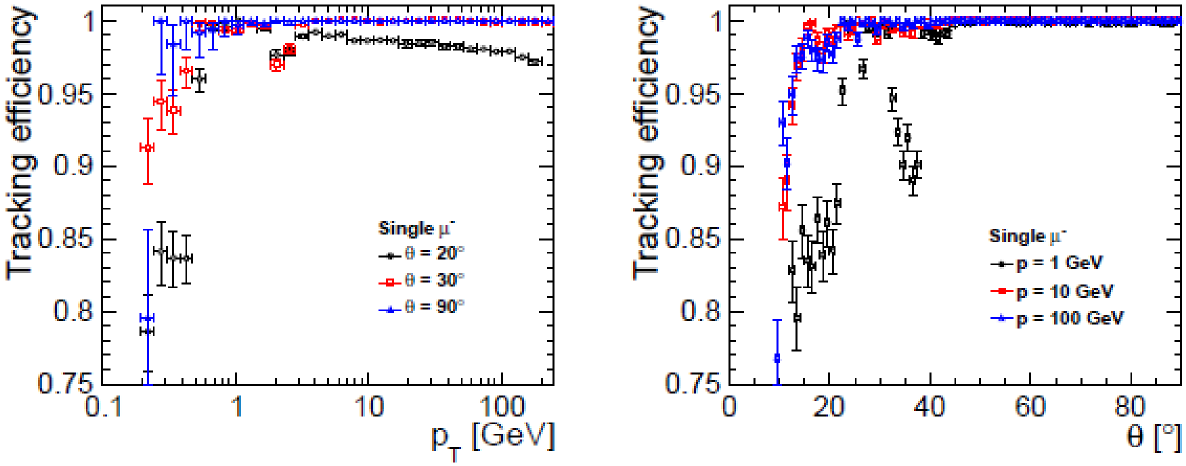


Barrel sensor with prototype pigtail cable.

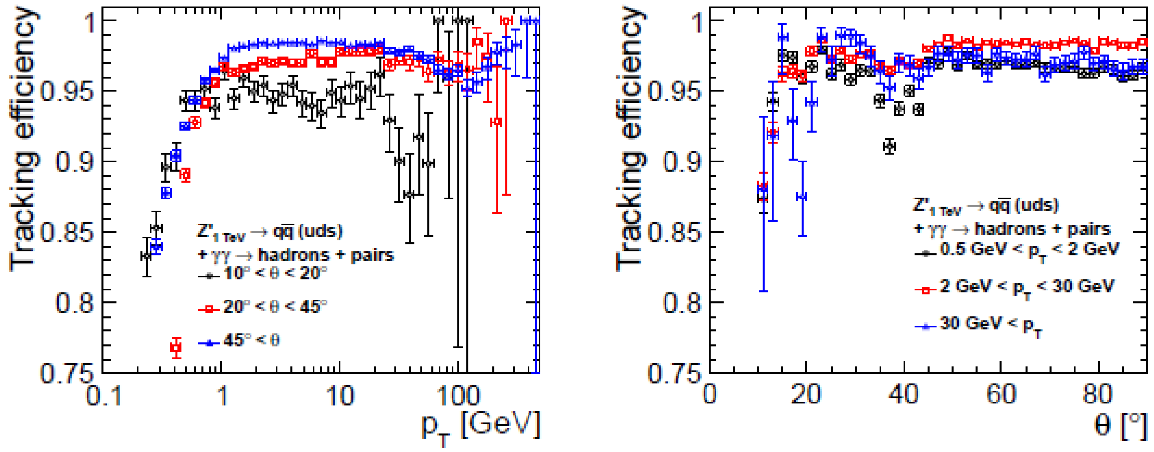
Silicon Tracking

Performance - efficiency

Single muons



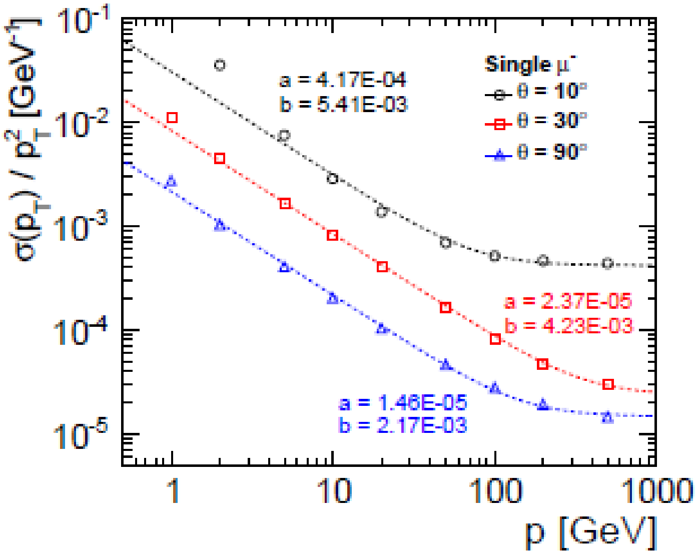
Di-jet Z'
(M = 1 Tev/c^2)



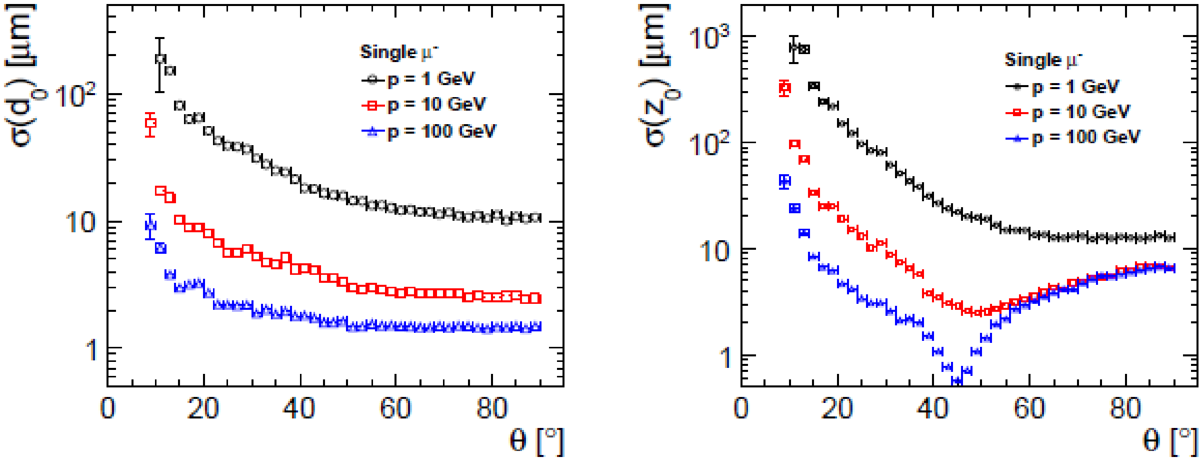
Silicon Tracking

Performance

Momentum resolution



Impact parameter



Tracker Alignment

SiD Alignment is based on:

1. Small number of robust, rigid elements
   - Minimize deviations
2. Precise positioning of smaller components during fabrication and assembly
   - Achieving ~ 20 μm (or better) precision
3. Real-time monitoring of alignment changes, including during push-pull moves
   - Using FSI, laser-tracks, and strain measurements using fibers
   - Building on ATLAS, CMS and AMS experiences
4. Track-based alignment for final precision
   - For each data-taking period
   - Overall accuracy ~ 3 μm (Tracker) / ~ 1 μm (Vertex)

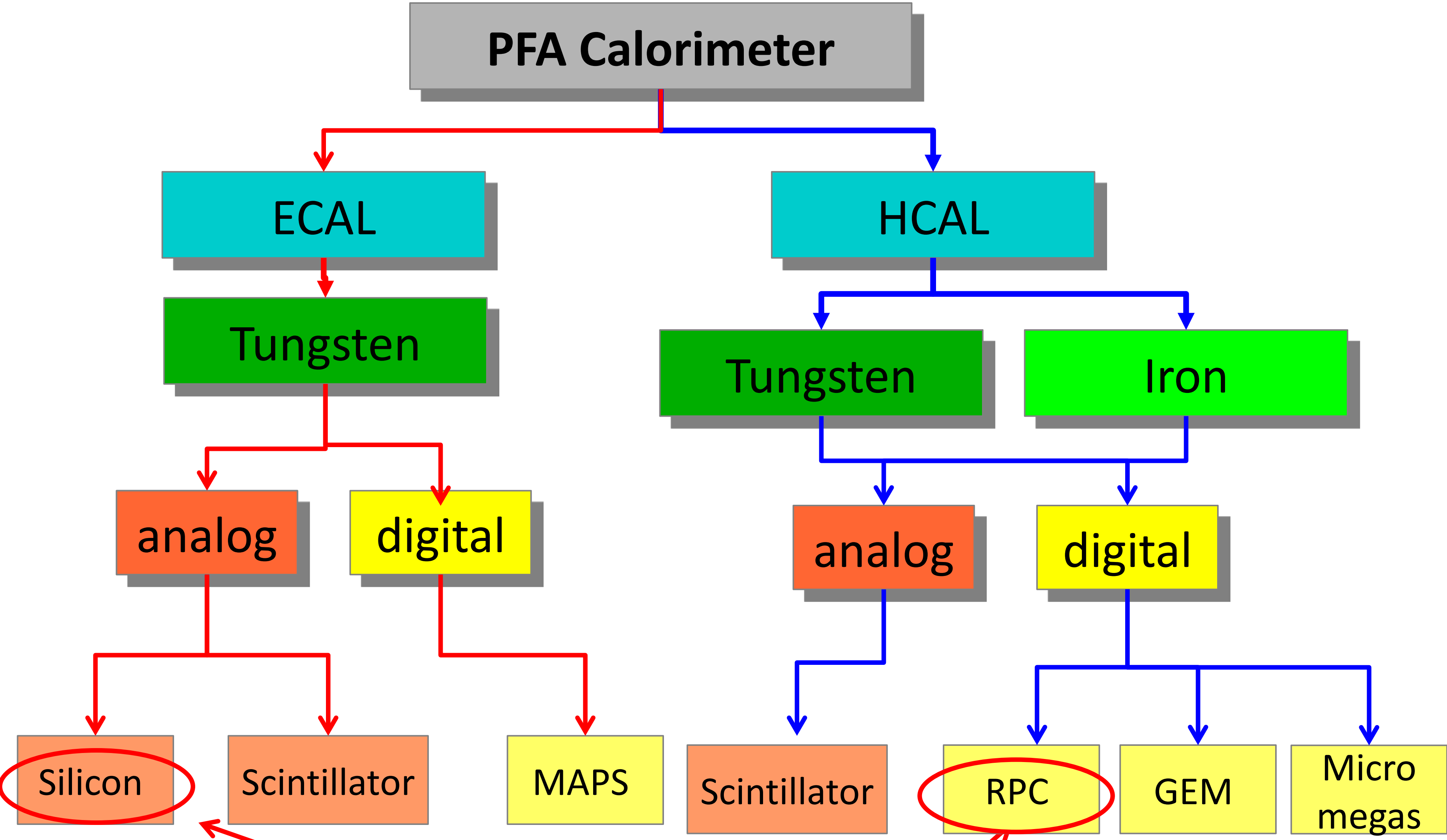
Calorimetry

SiD Calorimetry is designed for the PFA approach:

- ECAL and HCAL must be “imaging”: high granularity
- Small Moliere radius for ECAL – separate e^-/charged h
- Minimize gap between tracker and ECAL
- Sufficient overall depth

- SiD ECAL
  - Tungsten absorber
  - 20+10 layers
  - $20 \times 0.64 + 10 \times 1.30\ X_0$
- Baseline Readout using
  - 5x5 mm^2 silicon pads

- SiD HCAL
  - Steel Absorber
  - 40 layers
  - $4.5\ \lambda_i$
- Baseline readout
  - 1x1 cm^2 RPCs



PFA Calorimeter

ECAL

Tungsten

analog

Silicon

Scintillator

digital

MAPS

HCAL

Tungsten

Iron

analog

Scintillator

digital

RPC

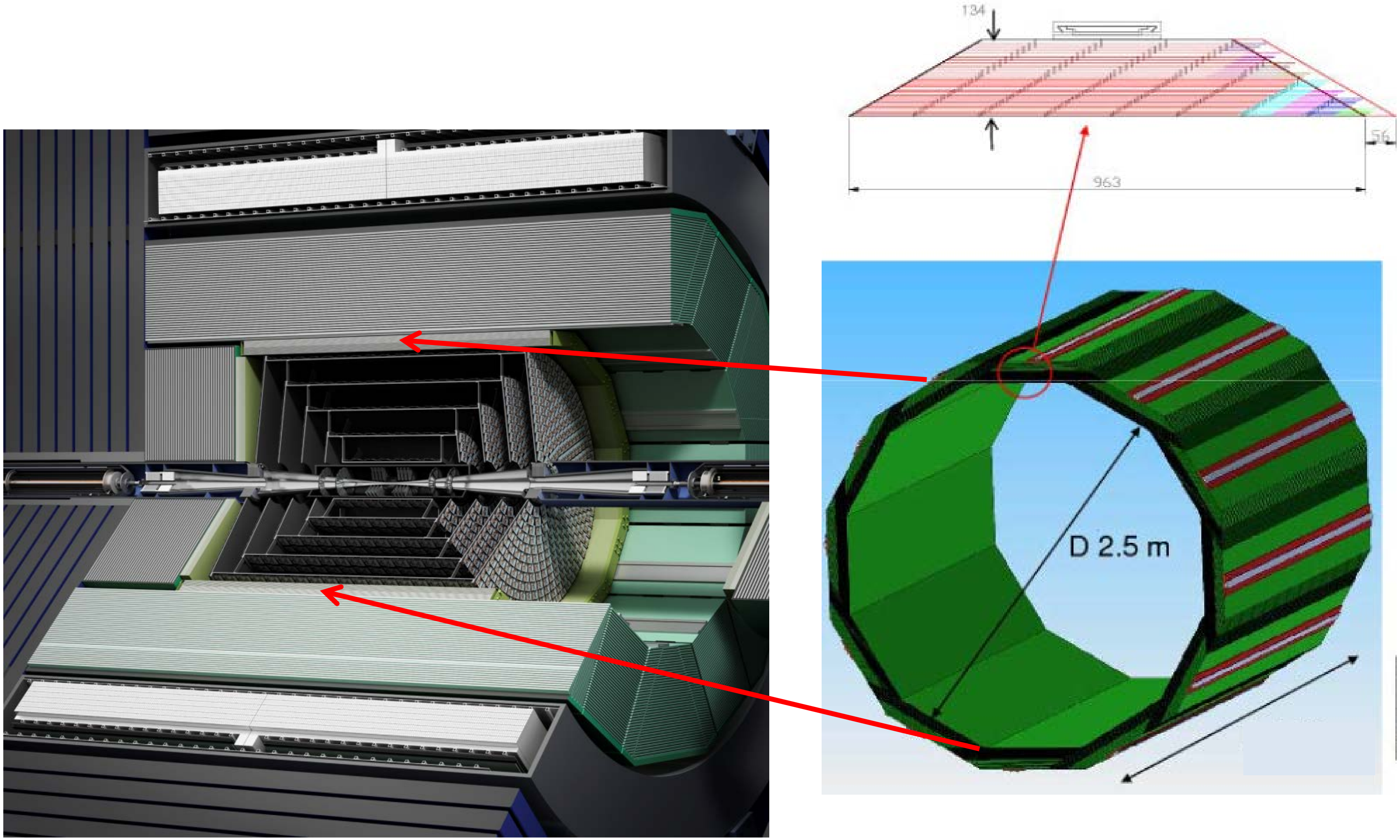
GEM

Micro megas

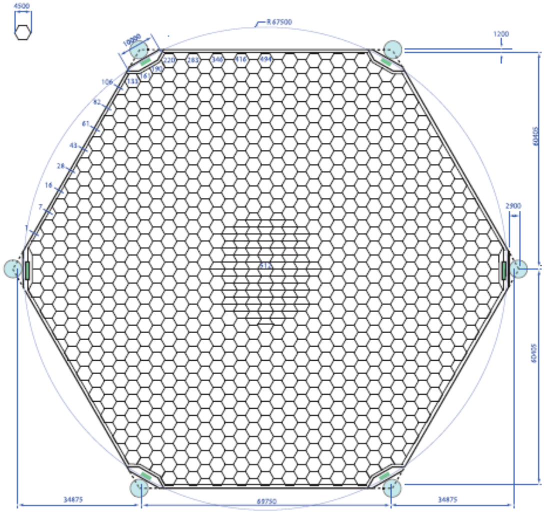
SiD Baseline choices

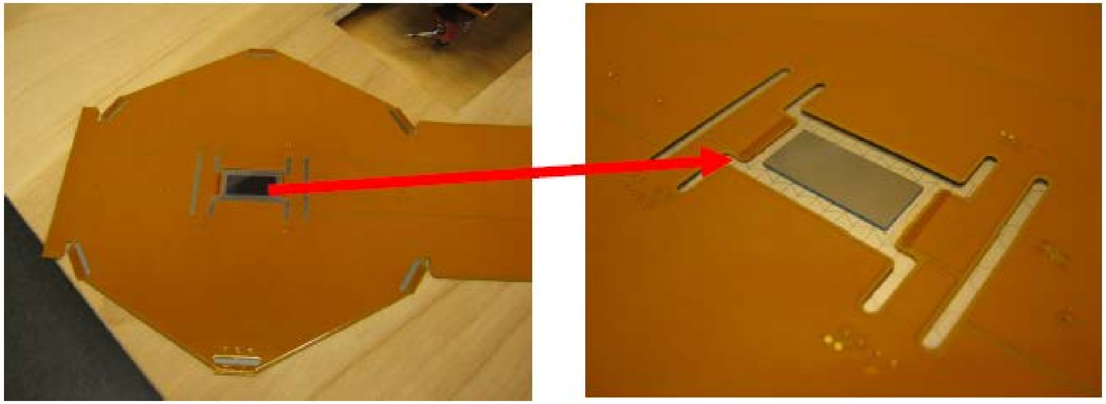
All other options (except a scintillator ECAL) are being considered

Electromagnetic Calorimetry



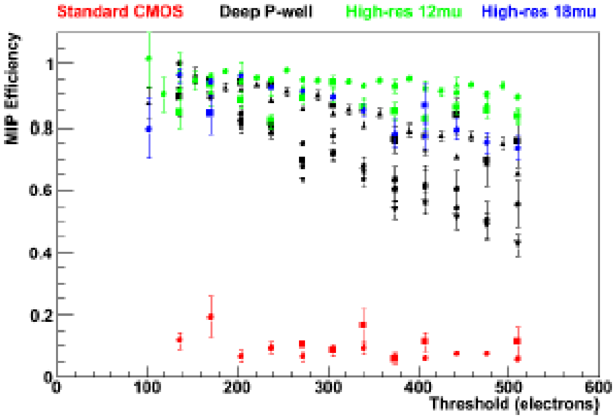
Electromagnetic Calorimetry



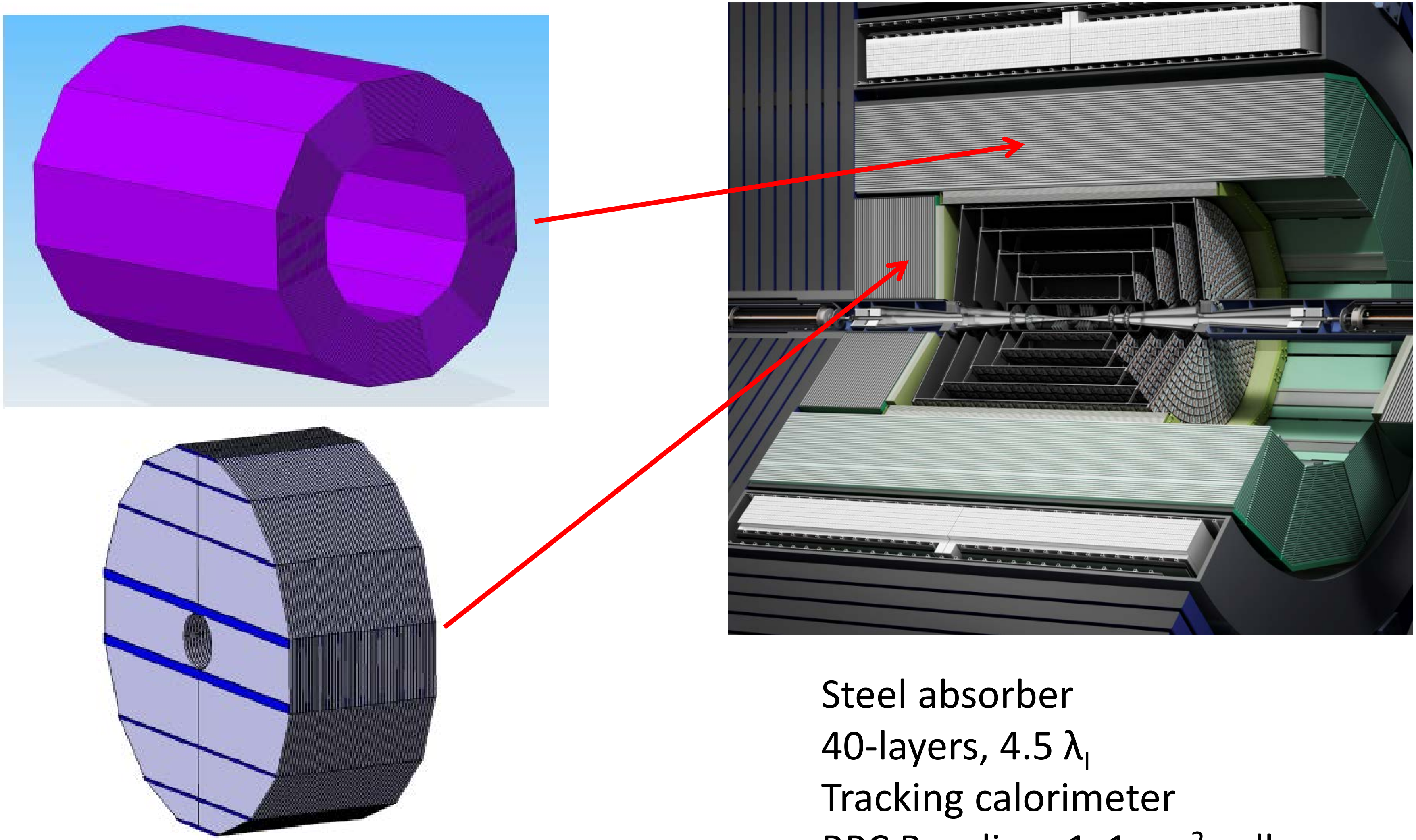


	Baseline
pixel size	13 mm^2
readout gap	1.25 mm (incl. 0.32 mm thick Si sensors)
effective Molière radius	14 mm
pixels per silicon sensor	1024
channels per KPiX chip	1024
dynamic range requirement	$\sim$ 0.1 to 2500 MIPs
heat load requirement	20 mW per sensor

Option: Monolithic Active Pixels (MAPS) 50µm x 50µm pixels



Hadronic Calorimetry



Steel absorber

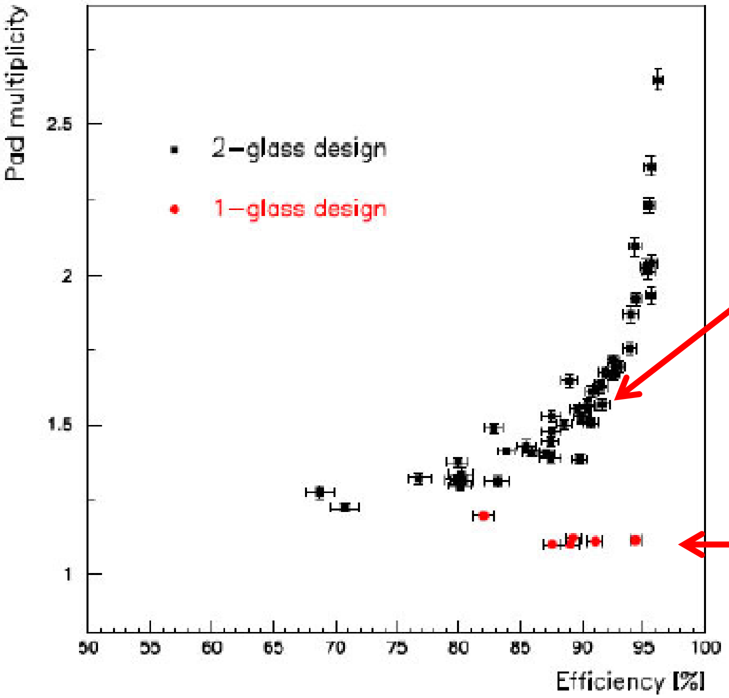
40-layers, 4.5 λ_I

Tracking calorimeter

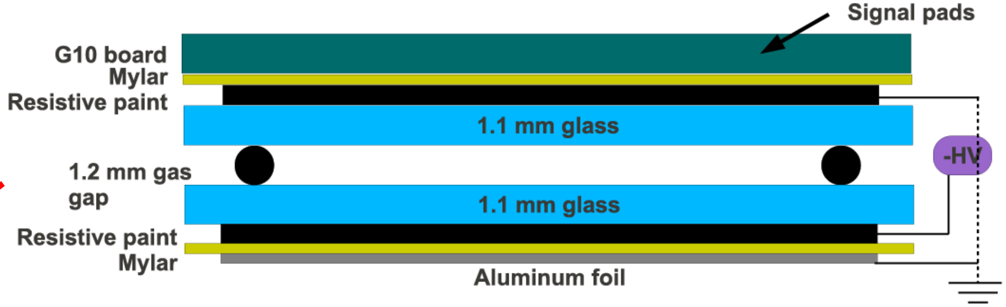
RPC Baseline. 1x1 cm^2 cells

Hadronic Calorimetry

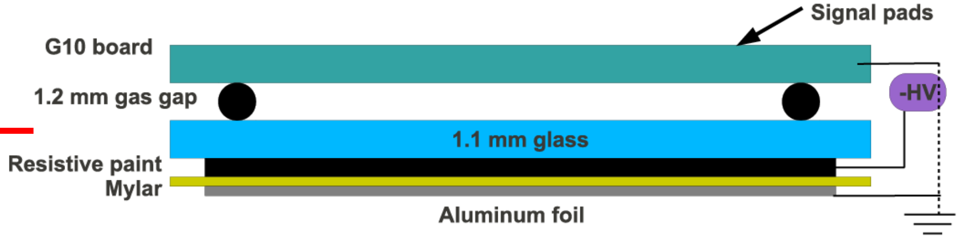
Baseline: RPC DHCAL



Default “two-glass” RPC



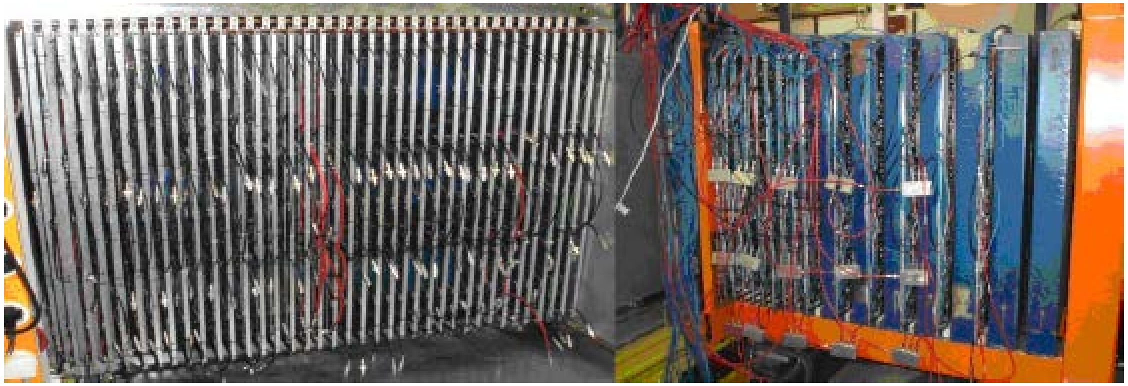
Special “one-glass” RPC



- 2-glass design can operate at good efficiency *and* low multiplicity
- 1-glass design has flat multiplicity vs. efficiency - still being understood/under development)

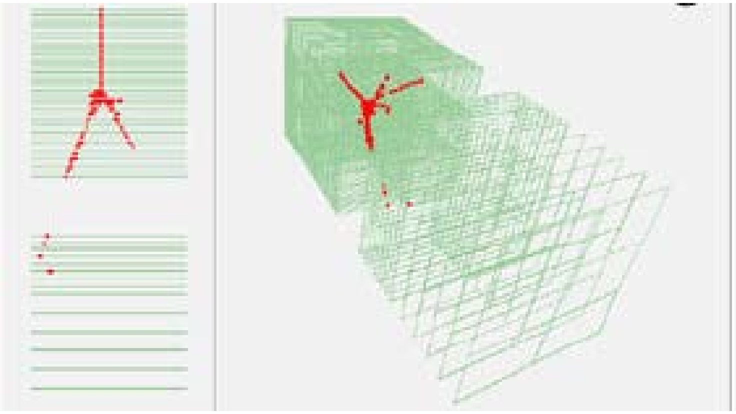
Hadronic Calorimetry

Baseline: RPC DHCAL

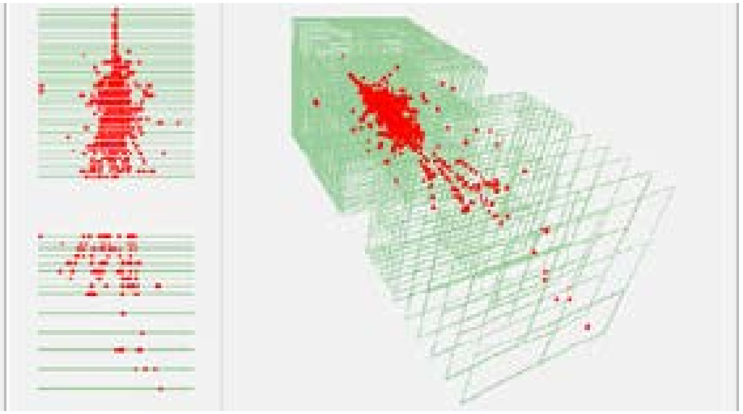


Test beam with 1 m^3 stack

Largest Calorimeter by channel count



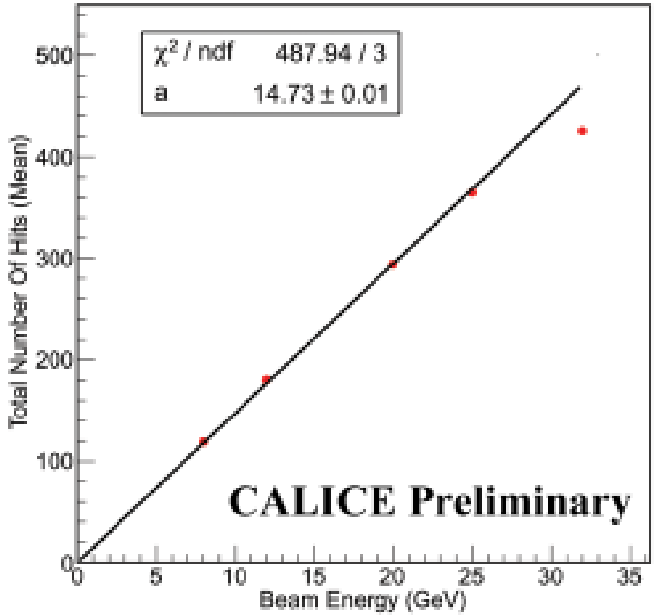
8 GeV pion shower

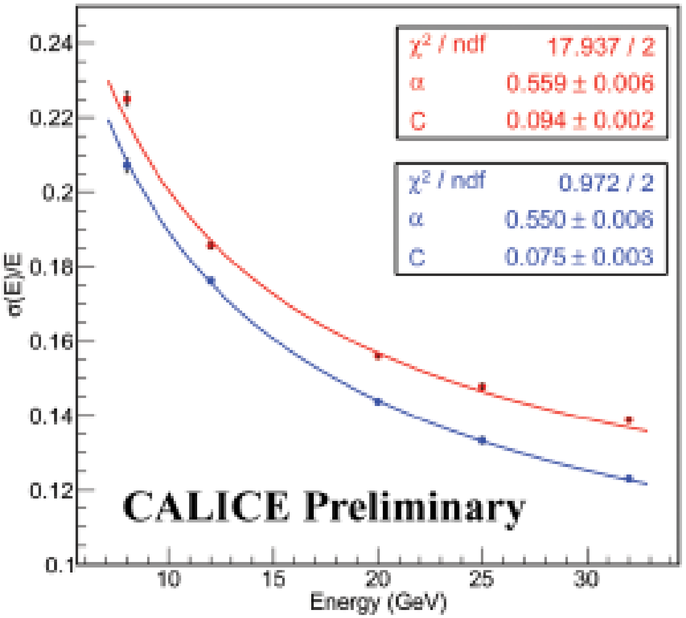


120 GeV proton shower.

Hadronic Calorimetry

Baseline: RPC DHCAL



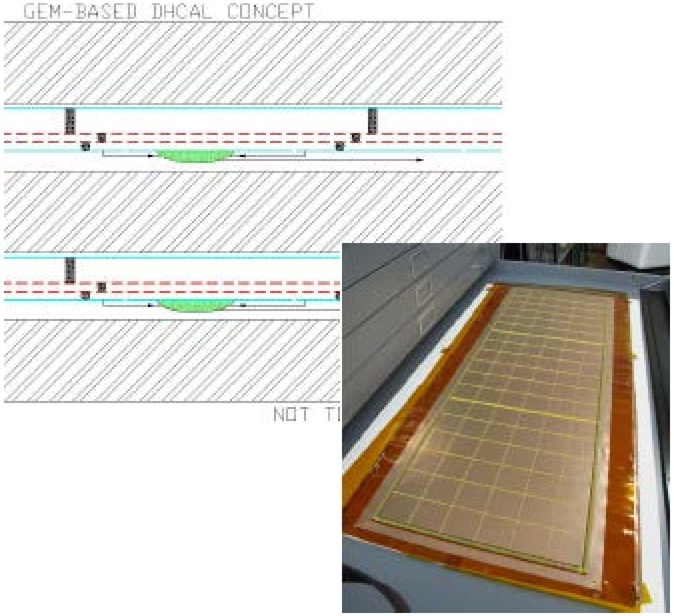


- The RPC technology is a great candidate for the readout of a highly segmented calorimeter.
- The dark rate in the DHCAL is very low
- The response is linear up to about 30 GeV/c.

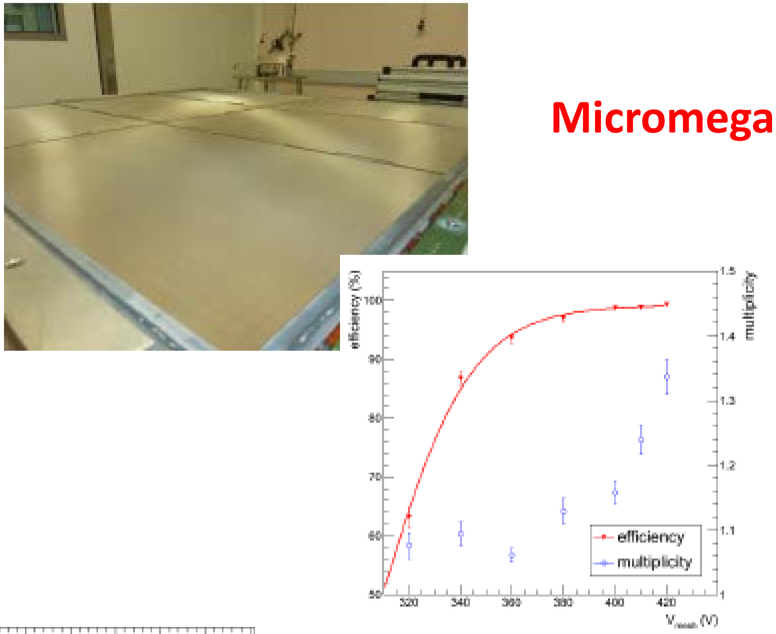
Hadronic Calorimetry

Options: GEM, Micromegas, Scintillator

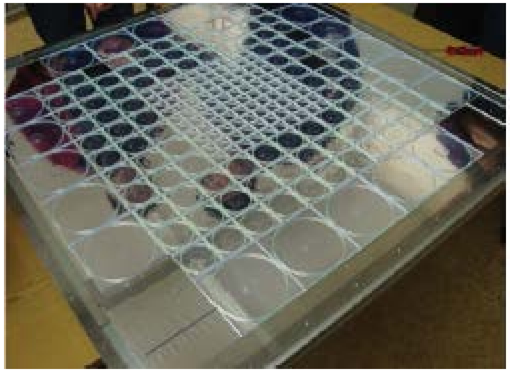
GEM

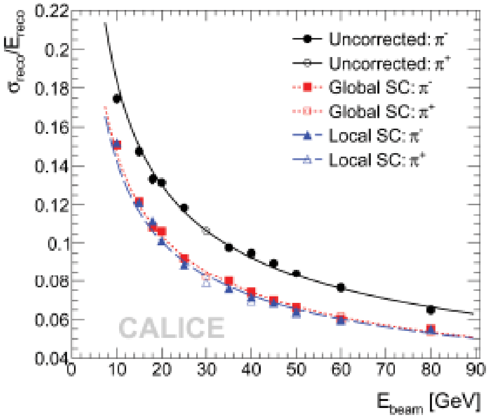


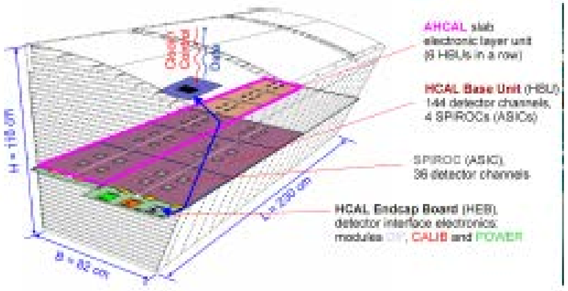
Micromegas



Scintillator

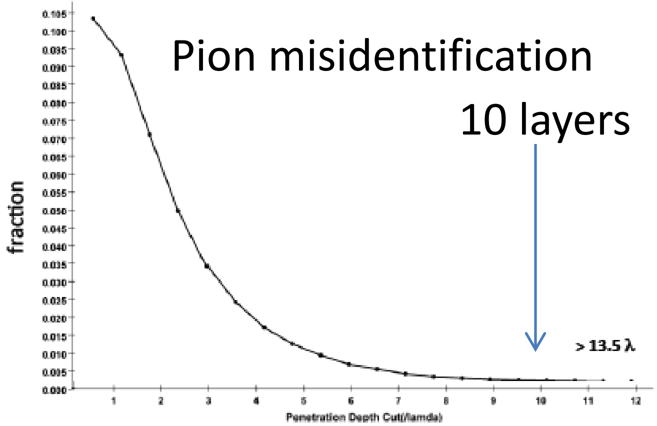


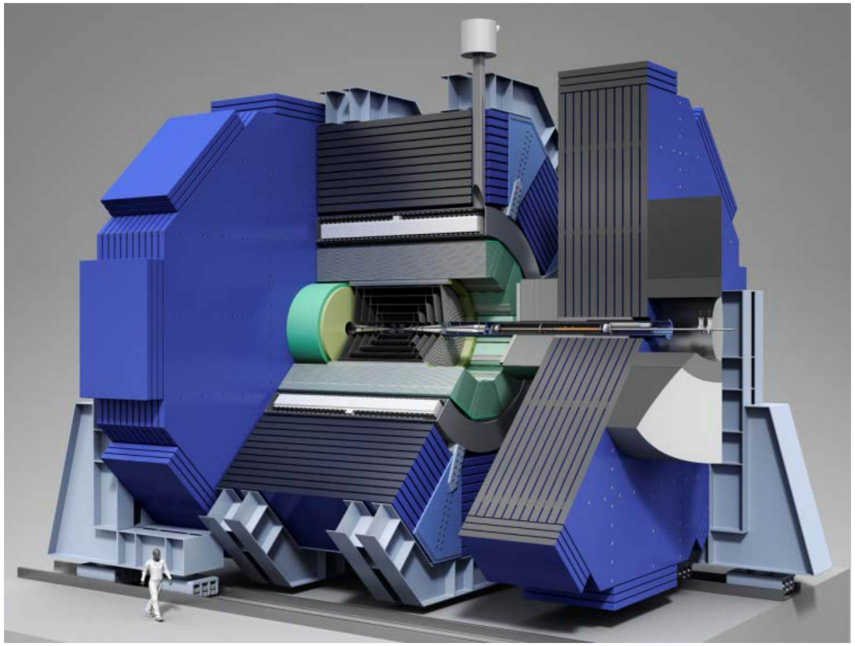


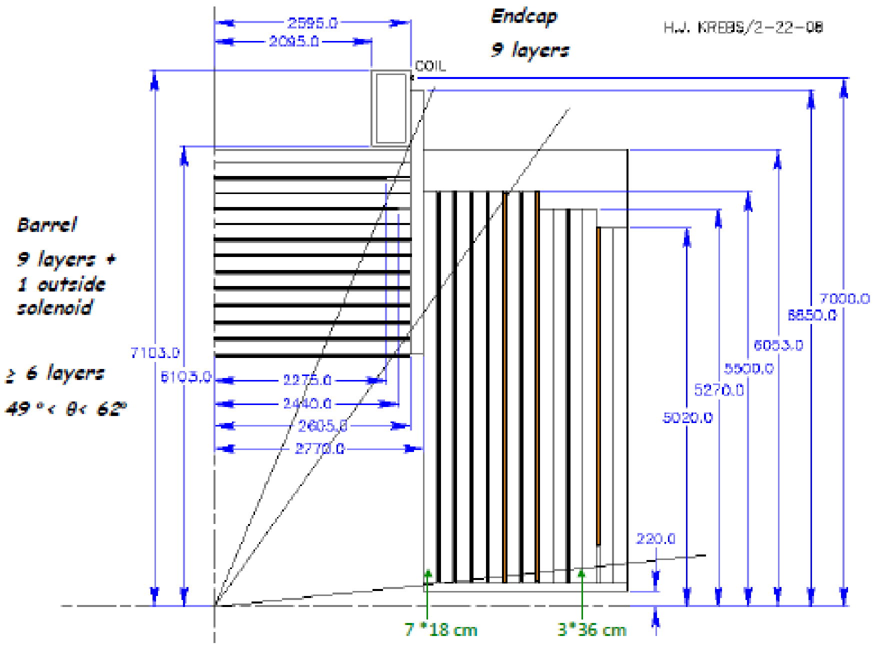


Muon System

- Muon identification/hadron rejection
- Flux return
- Tail catcher for calorimeter system
- Low rates/large area





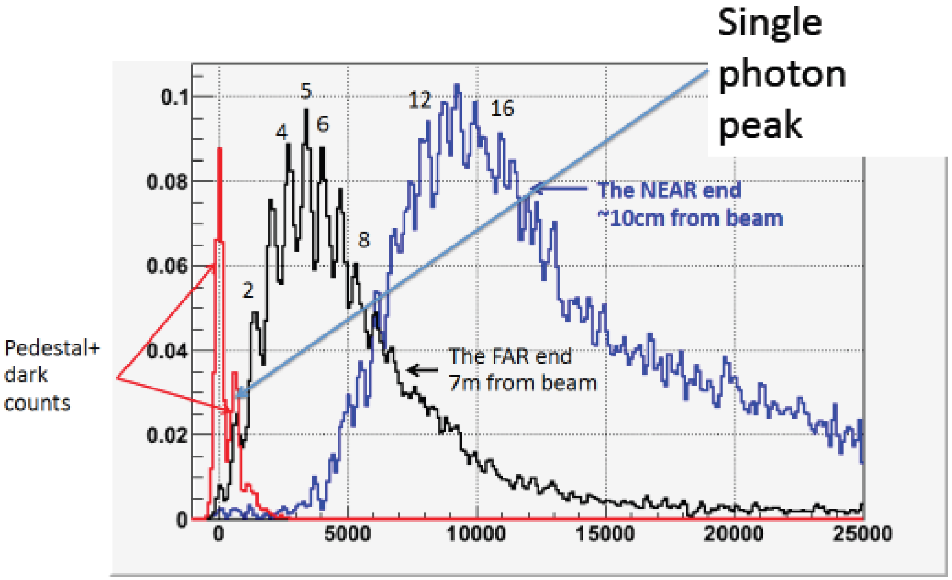


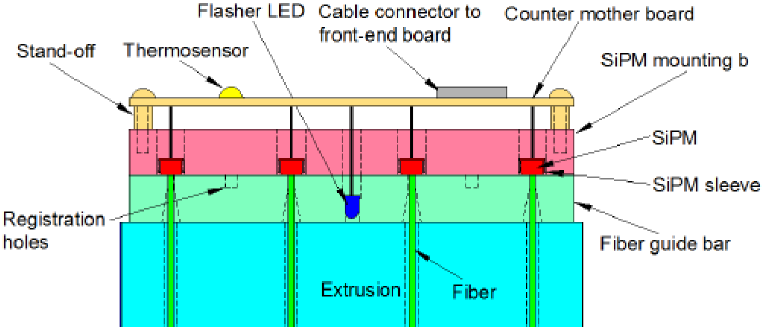
Muon System

Major change of baseline vs. LOI:

Scintillating strips/wavelength shifting fibers

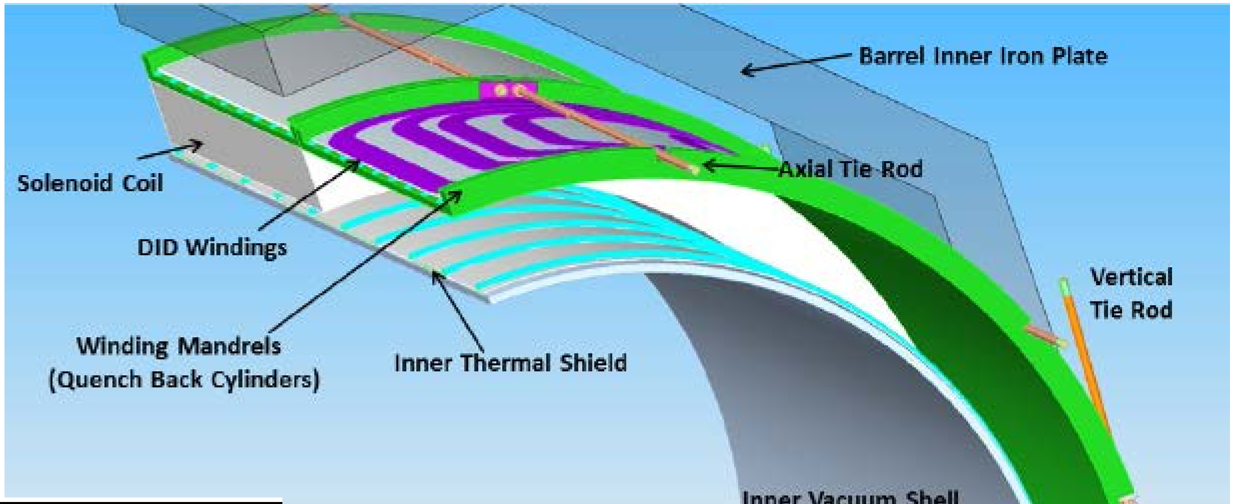
(RPC remains as an option)

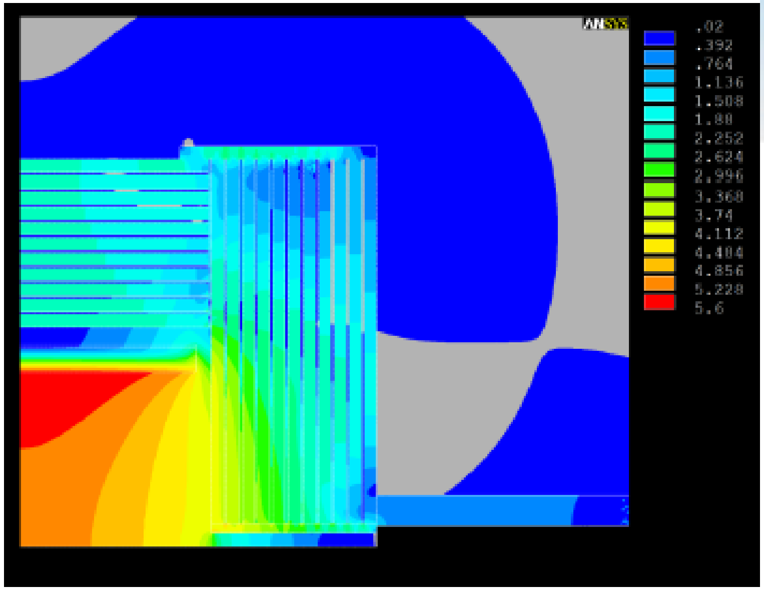




Development of system to position SiPM at the end of a fiber

Magnet System

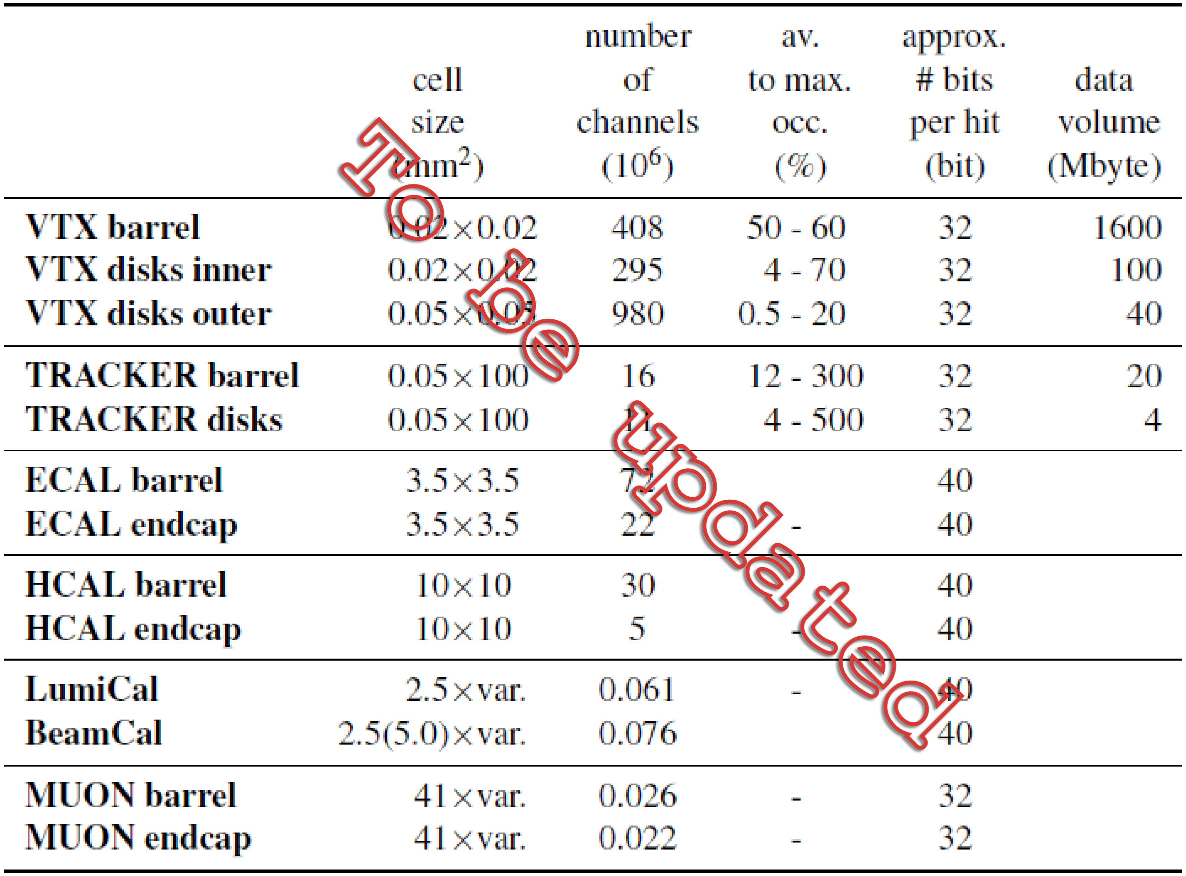




- 5 T design based on 4 T CMS solenoid
- Muon system flux return
  - ANSYS 2-D and 3-D models used in design work
  - Benefitted from cryo engineering at SLAC and BNL and advances in computation

Electronics and DAQ - Rates

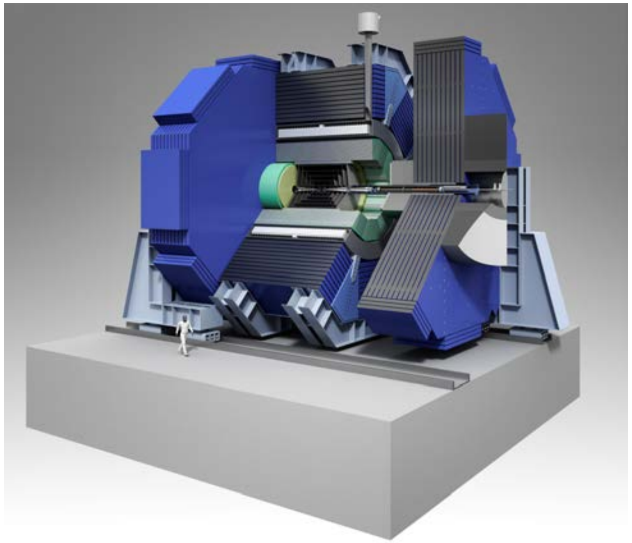
- SiD Electronics and DAQ built around KPiX approach
  →Maximize common components



To be updated

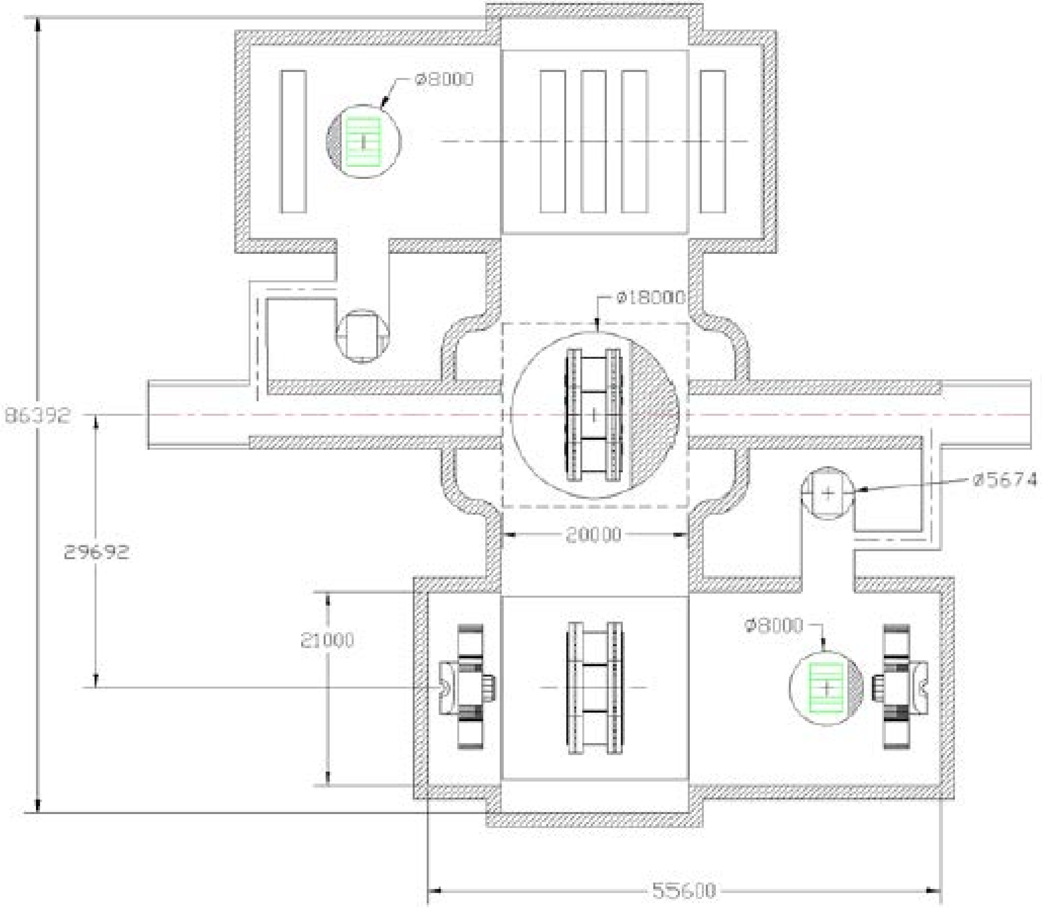
	cell size (mm^2)	number of channels (10^6)	av. to max. occ. (%)	approx. # bits per hit (bit)	data volume (Mbyte)
VTX barrel	0.02×0.02	408	50 - 60	32	1600
VTX disks inner	0.02×0.02	295	4 - 70	32	100
VTX disks outer	0.05×0.05	980	0.5 - 20	32	40
TRACKER barrel	0.05×100	16	12 - 300	32	20
TRACKER disks	0.05×100	11	4 - 500	32	4
ECAL barrel	3.5×3.5	72		40	
ECAL endcap	3.5×3.5	22	-	40	
HCAL barrel	10×10	30		40	
HCAL endcap	10×10	5	-	40	
LumiCal	2.5×var.	0.061	-	40	
BeamCal	2.5(5.0)×var.	0.076		40	
MUON barrel	41×var.	0.026	-	32	
MUON endcap	41×var.	0.022	-	32	

Detector Integration and MDI

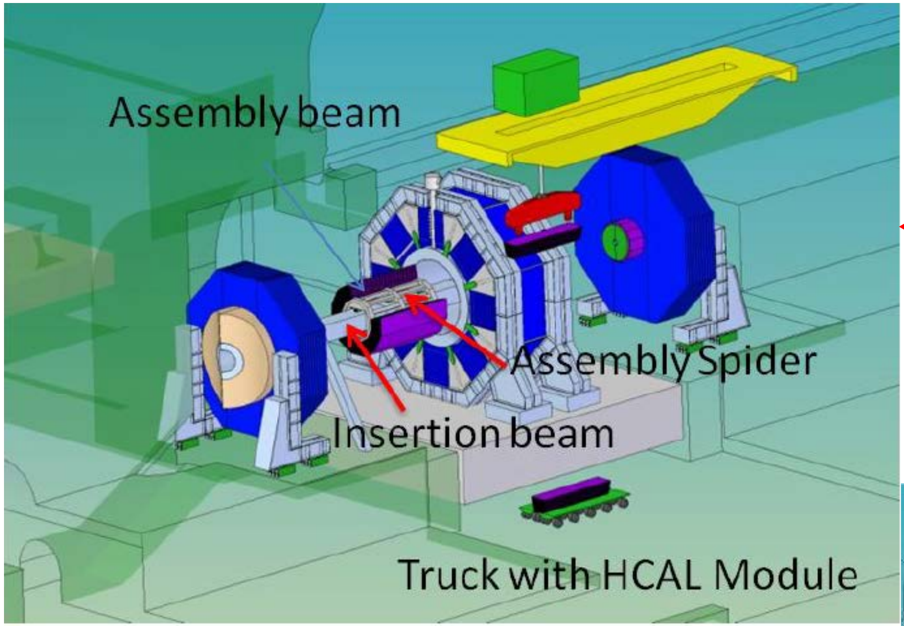


3 m thick concrete push-pull platform:
- 30 m travel for detector swap
- ~1 mm max static deflection at detector support points

IR Hall configuration (vertical access)

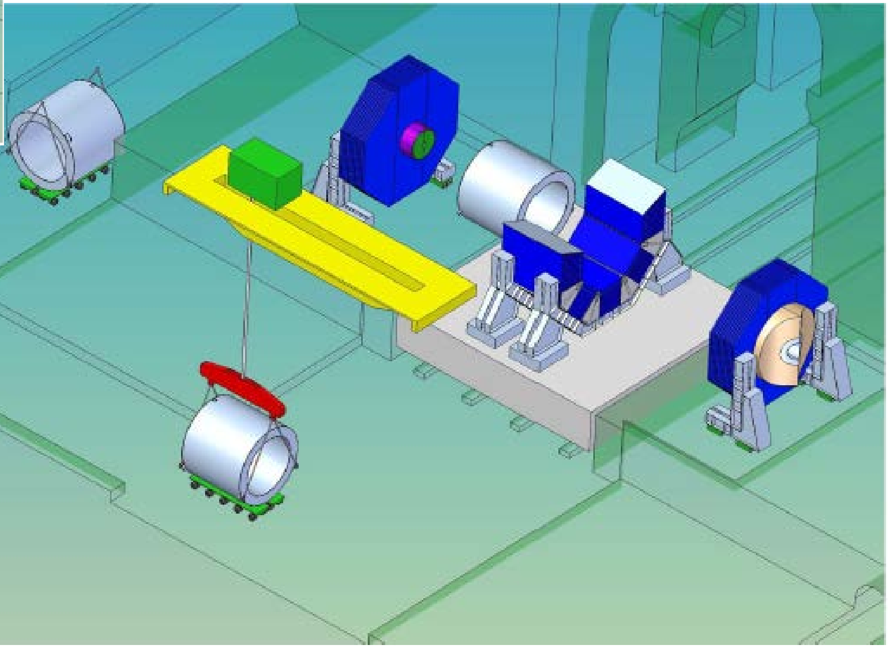


Detector Assembly - examples

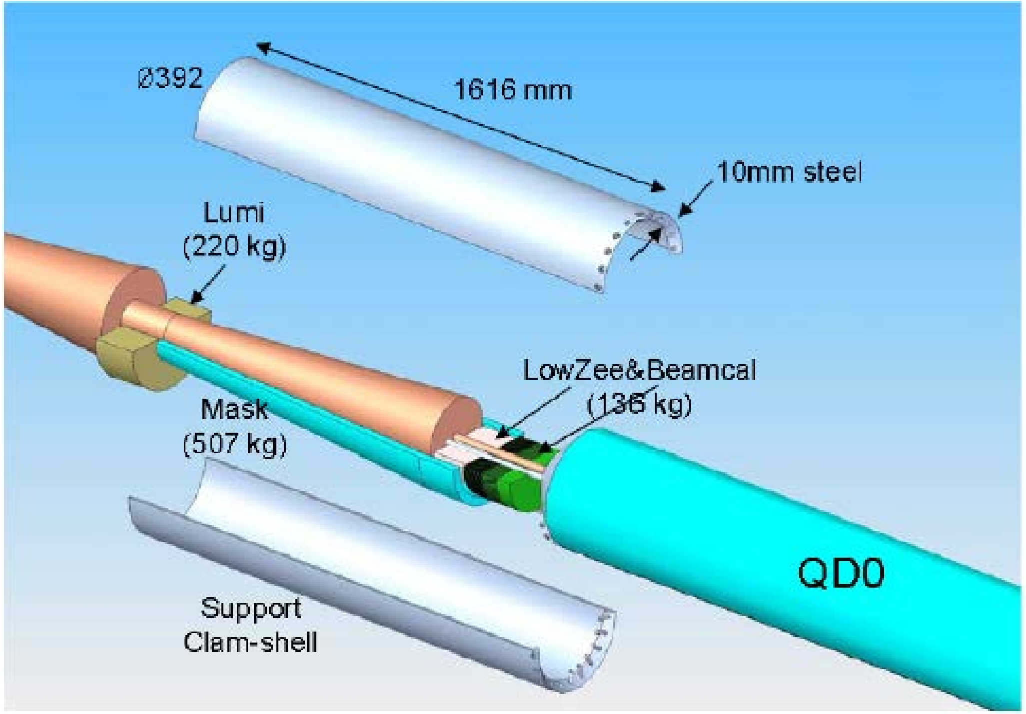


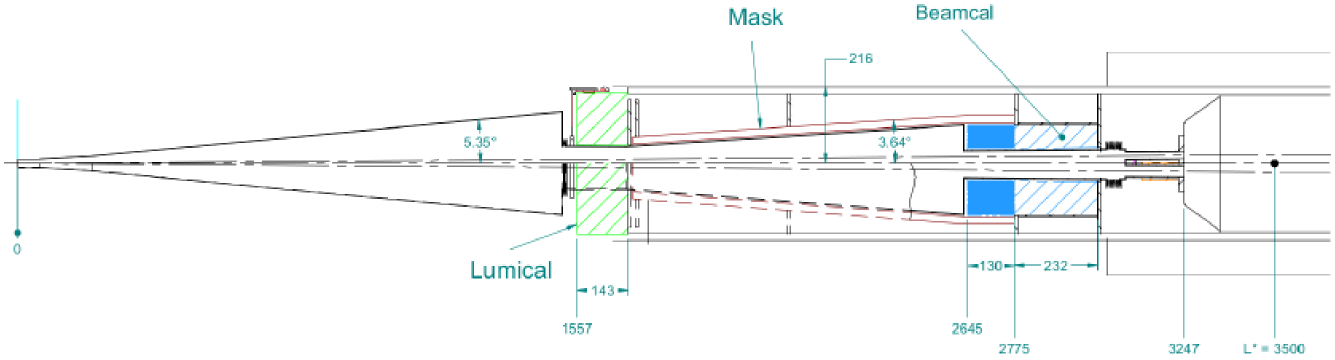
Assembling the Hadron Calorimeter

Horizontal access – moving the solenoid

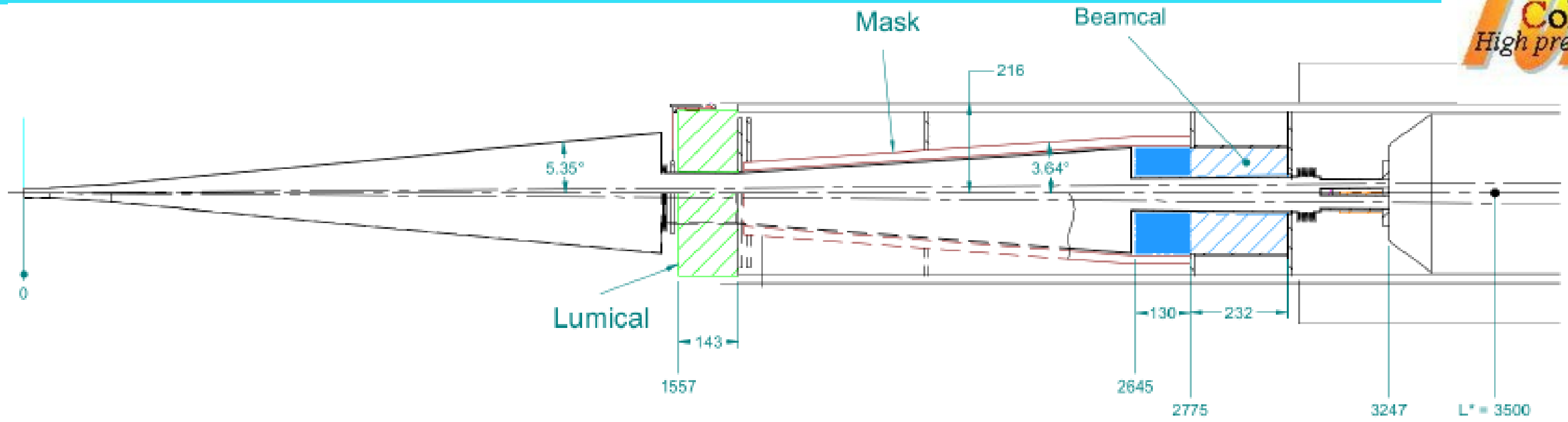


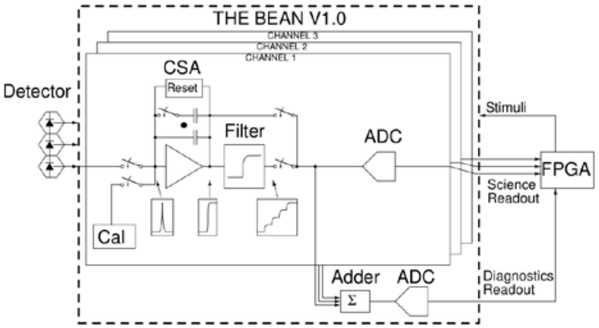
Beampipe/Forward Region





Beampipe/Forward Region

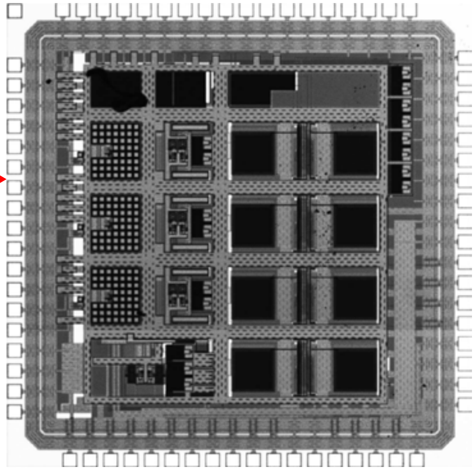




LumiCal - integrated luminosity and luminosity spectrum

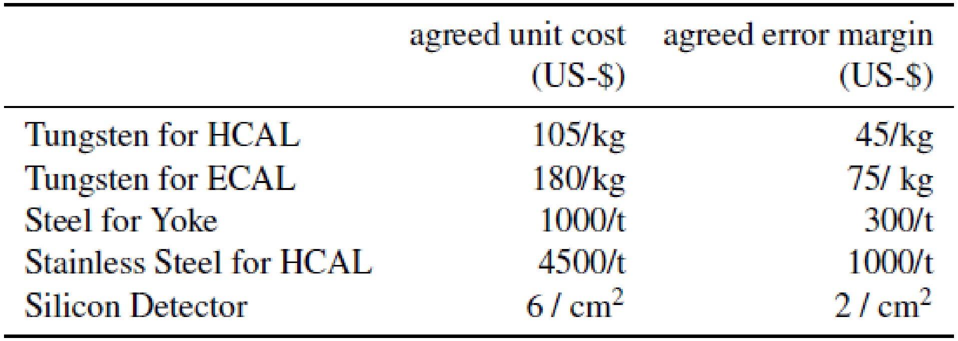
BeamCal – small angle coverage (with LumiCal), instantaneous luminosity

Dedicated ASIC (Bean chip) for high luminosity region



SiD Costs

- Costing is based on SiD Parametric Model
- Basic items have agreed cost (SiD, ILD and CLIC):



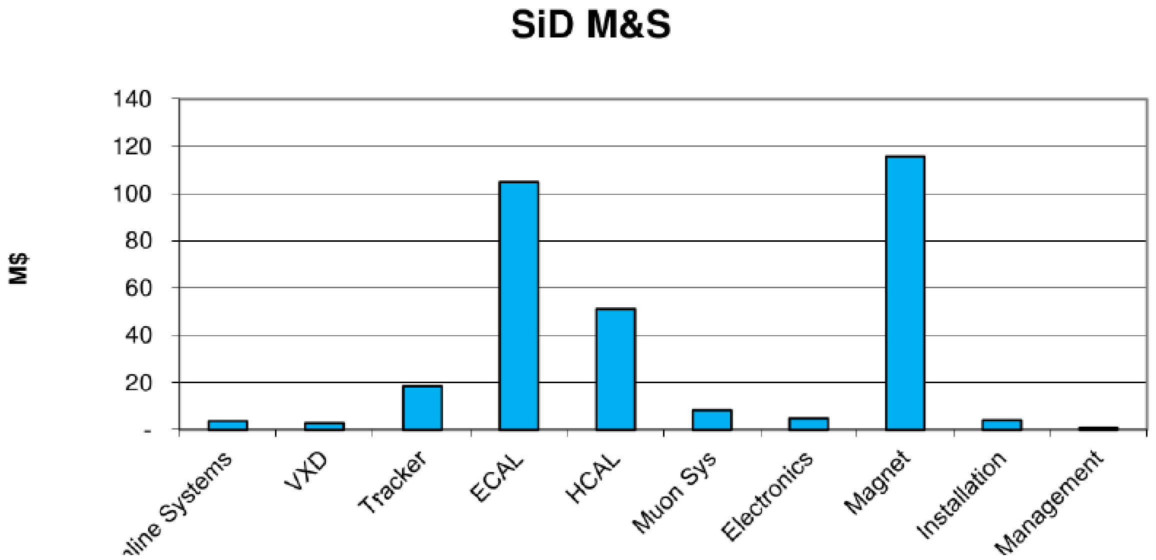
	agreed unit cost (US-\$)	agreed error margin (US-\$)
Tungsten for HCAL	105/kg	45/kg
Tungsten for ECAL	180/kg	75/ kg
Steel for Yoke	1000/t	300/t
Stainless Steel for HCAL	4500/t	1000/t
Silicon Detector	6 / cm^2	2 / cm^2

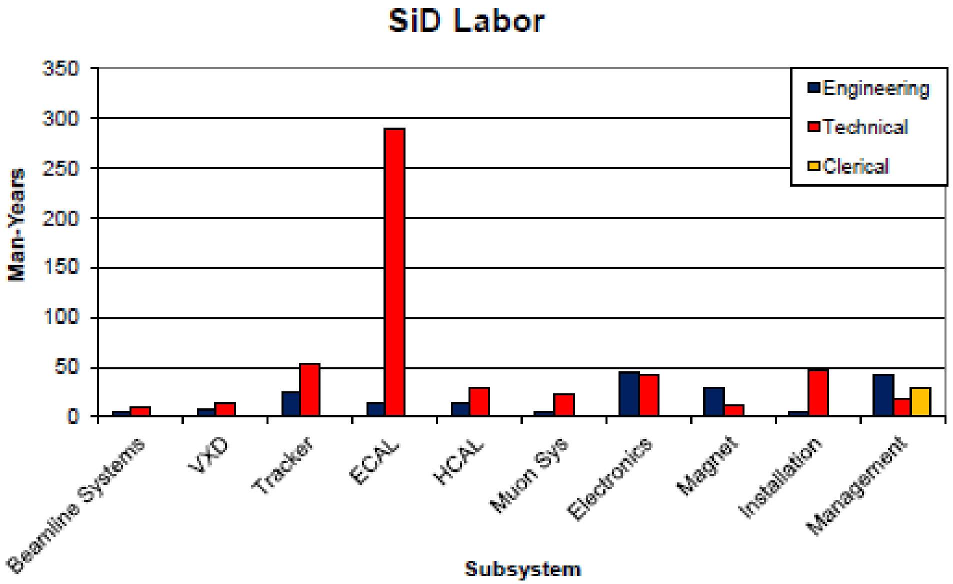
- Costs in 2008 U.S. $

M&S 315 $M
Contingency 127 $M
Labor 748 $M

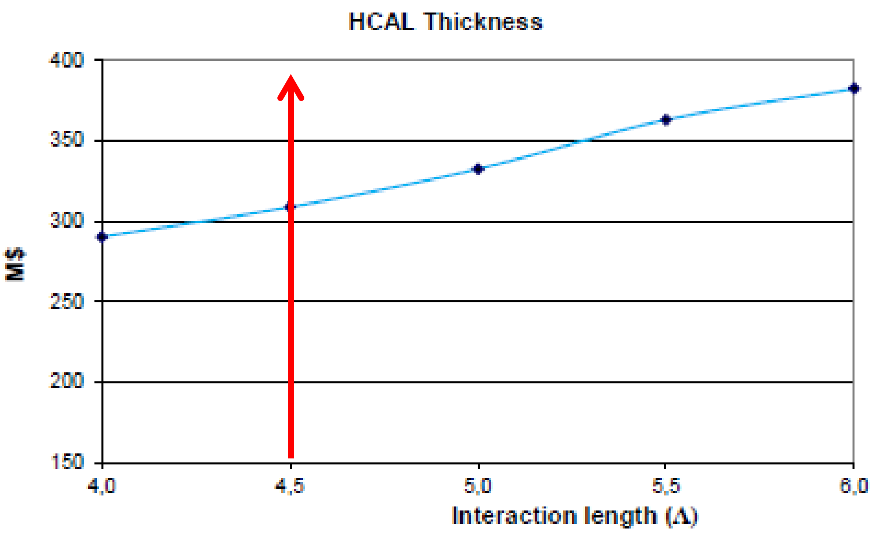
- Model allows exploration of sensitivity to cost increase and detector parameter changes

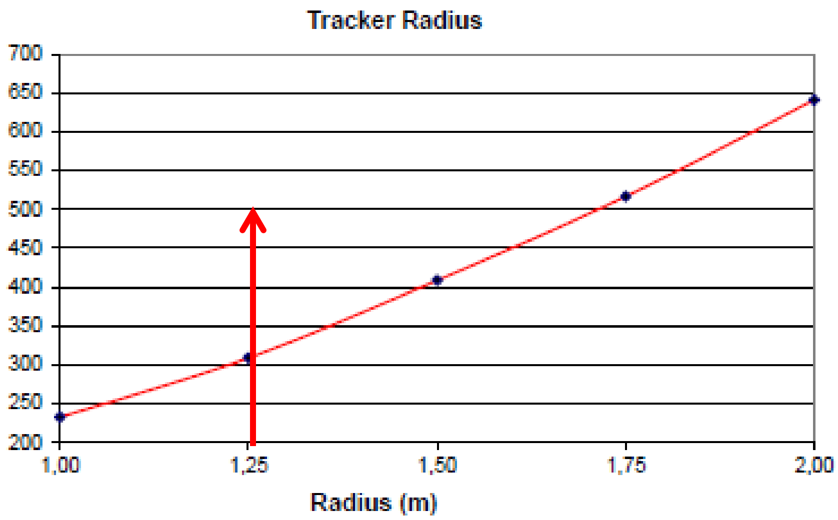
SiD Costs


SiD M&S
M$
140
120
100
80
60
40
20
-
line Systems
VXD
Tracker
ECAL
HCAL
Muon Sys
Electronics
Magnet
Installation
Management


SiD Labor
Man-Years
350
300
250
200
150
100
50
0
Engineering
Technical
Clerical
Beamline Systems
VXD
Tracker
ECAL
HCAL
Muon Sys
Electronics
Magnet
Installation
Management
Subsystem

SiD Costs





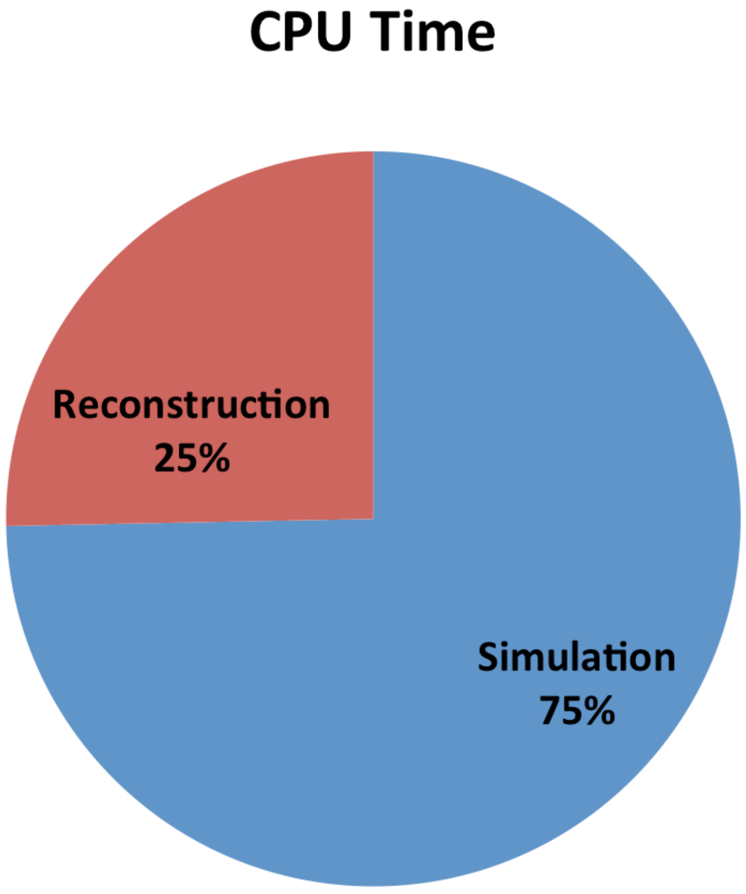
Note: For the LOI an optimal cost region was found near the baseline parameters:

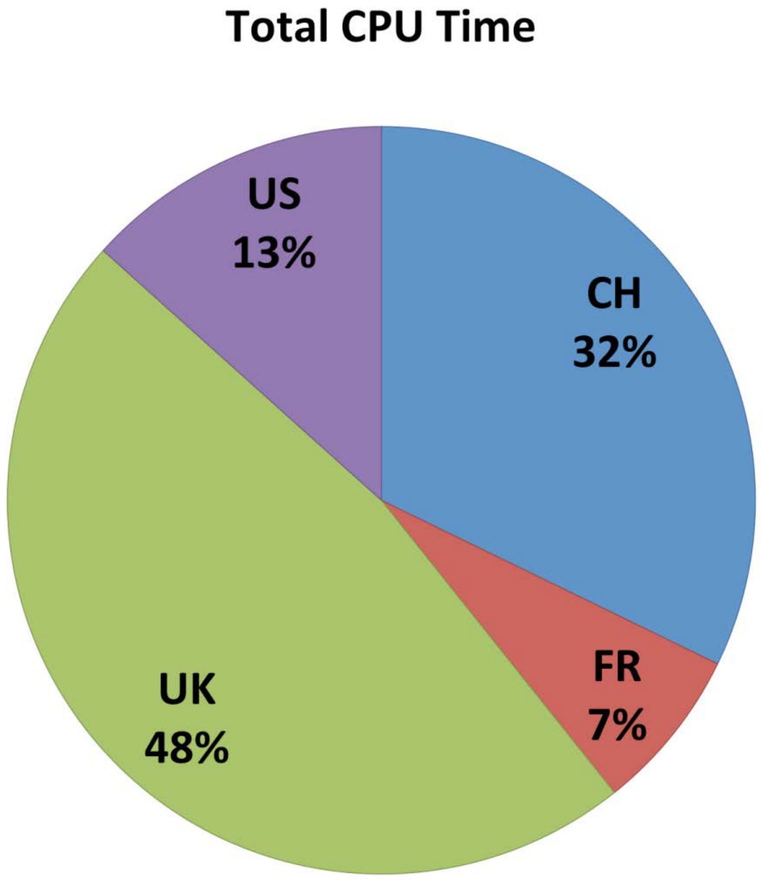
$R_{tracker}$ = 1.25 m, B = 5 T, HCAL λ_I = 4.5

Cost of Tungsten HCAL has been evaluated (requested by IDAG)

No potential savings

SiD Production Status





- 3000 CPU days and 79000 Jobs
- 89 % Efficiency (Jobs successful)

SiD DBD Summary and Beyond

- We have presented a detailed design for a detector capable of high precision physics studies and discoveries at the ILC.

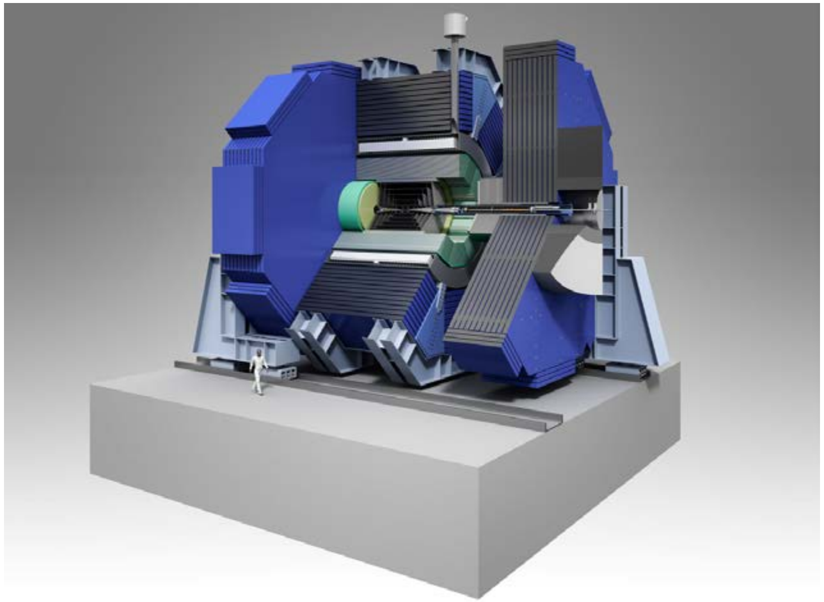
- Our technology choices are based on the currently available R&D results from SiD, CALICE, FCAL and other sources.

- We will continue to study/develop the SiD concept and pursue additional physics studies.

- As the ILC moves towards realization, we will expand SiD globally and work energetically with the new Linear Collider Organization to promote the ILC project

SiD研究グループは、日本でDBDを紹介する機会を与えてもらえましたことを大変光栄に思います。

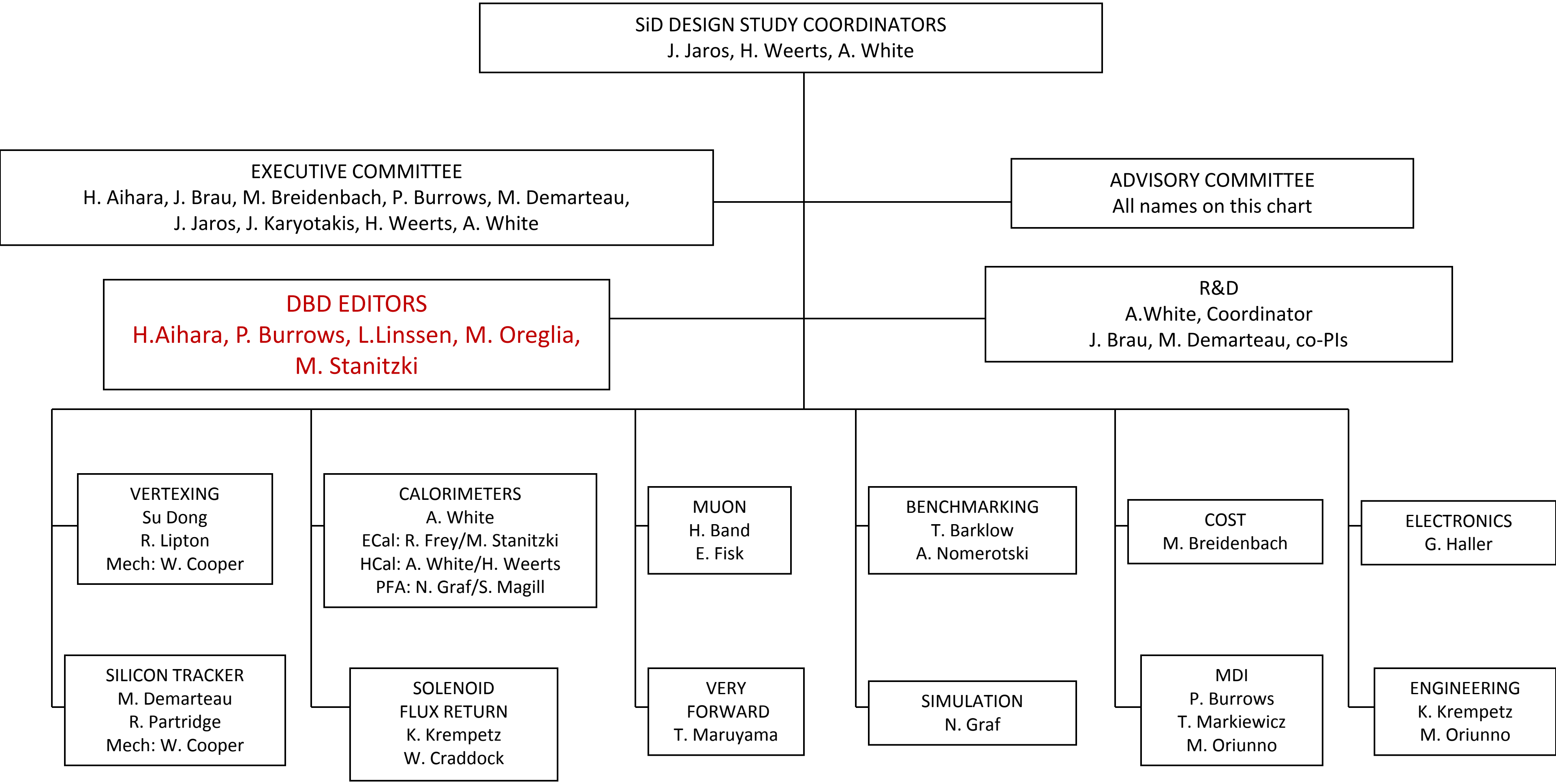
SiD Workshop
SLAC, January 16-18, 2013



This will be a critical meeting as we move forward from the DBD towards the next phase of the realization of the ILC and the SiD detector concept

Extra slides

SiD Design Study Organization



SiD DESIGN STUDY COORDINATORS
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J. Jaros, J. Karyotakis, H. Weerts, A. White

ADVISORY COMMITTEE
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M. Stanitzki

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A.White, Coordinator
J. Brau, M. Demarteau, co-PIs

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R. Lipton
Mech: W. Cooper

SILICON TRACKER
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Mech: W. Cooper

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ECal: R. Frey/M. Stanitzki
HCal: A. White/H. Weerts
PFA: N. Graf/S. Magill

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FLUX RETURN
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W. Craddock

MUON
H. Band
E. Fisk

VERY
FORWARD
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BENCHMARKING
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A. Nomerotski

SIMULATION
N. Graf

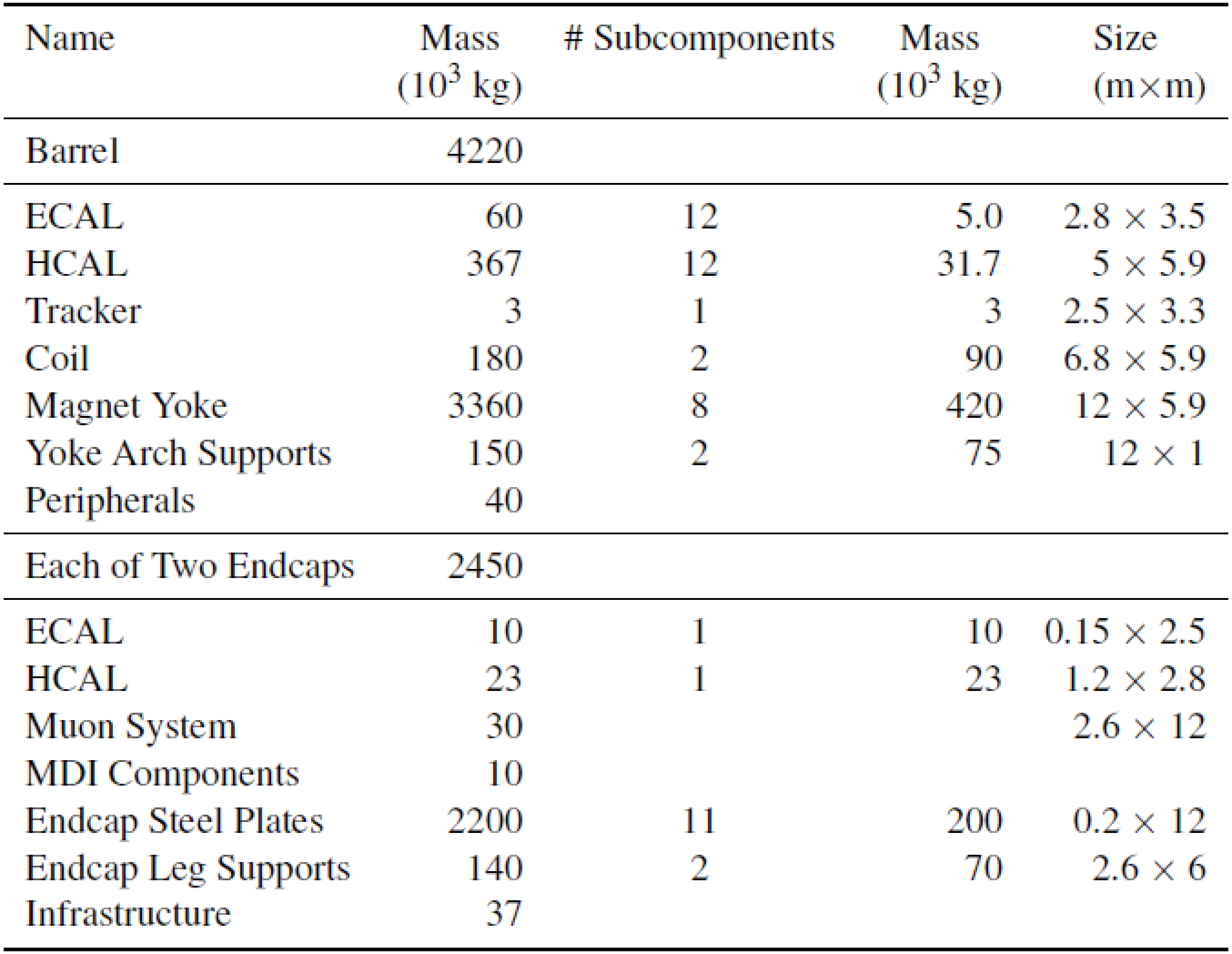
COST
M. Breidenbach

MDI
P. Burrows
T. Markiewicz
M. Oriunno

ELECTRONICS
G. Haller

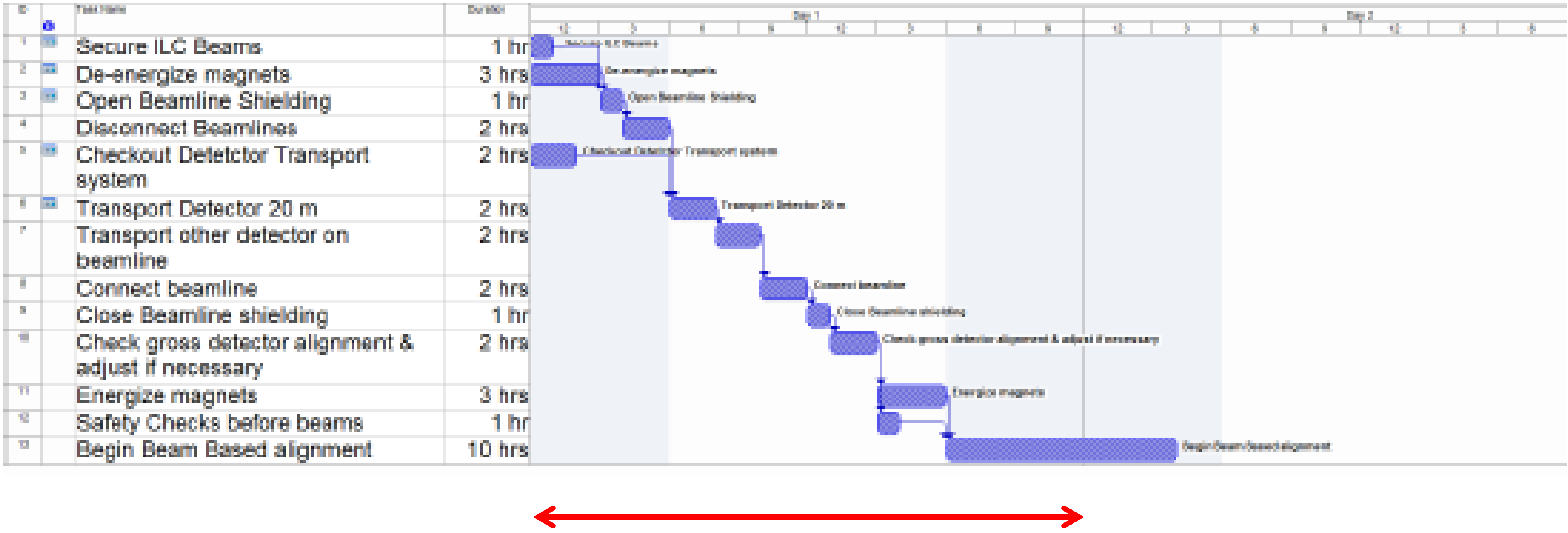
ENGINEERING
K. Krempetz
M. Oriunno

SiD Elements, Masses and Sizes



Name	Mass (10^3 kg)	# Subcomponents	Mass (10^3 kg)	Size (m×m)
Barrel	4220			
ECAL	60	12	5.0	2.8 × 3.5
HCAL	367	12	31.7	5 × 5.9
Tracker	3	1	3	2.5 × 3.3
Coil	180	2	90	6.8 × 5.9
Magnet Yoke	3360	8	420	12 × 5.9
Yoke Arch Supports	150	2	75	12 × 1
Peripherals	40			
Each of Two Endcaps	2450			
ECAL	10	1	10	0.15 × 2.5
HCAL	23	1	23	1.2 × 2.8
Muon System	30			2.6 × 12
MDI Components	10			
Endcap Steel Plates	2200	11	200	0.2 × 12
Endcap Leg Supports	140	2	70	2.6 × 6
Infrastructure	37			

SiD Push-Pull detector exchange

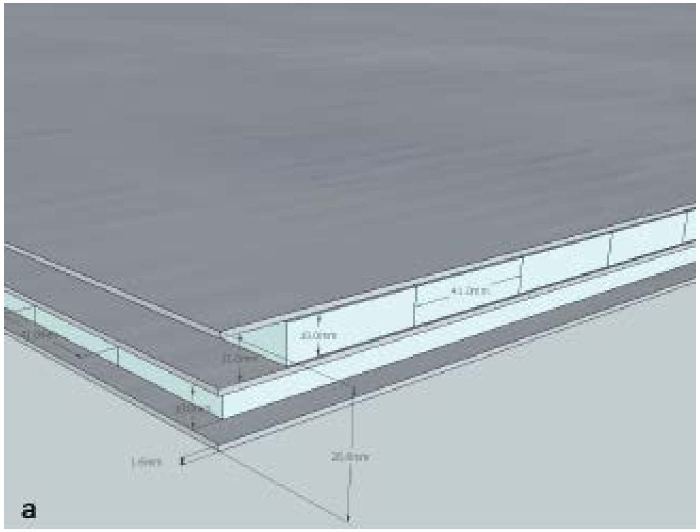


ID	Task Name	Duration
1	Secure ILC Beams	1 hr
2	De-energize magnets	3 hrs
3	Open Beamline Shielding	1 hr
4	Disconnect Beamlines	2 hrs
5	Checkout Detetctor Transport system	2 hrs
6	Transport Detector 20 m	2 hrs
7	Transport other detector on beamline	2 hrs
8	Connect beamline	2 hrs
9	Close Beamline shielding	1 hr
10	Check gross detector alignment & adjust if necessary	2 hrs
11	Energize magnets	3 hrs
12	Safety Checks before beams	1 hr
13	Begin Beam Based alignment	10 hrs

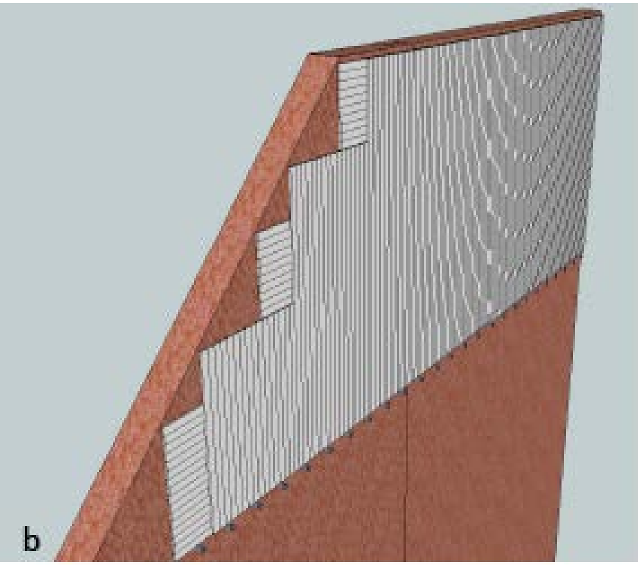
1 day

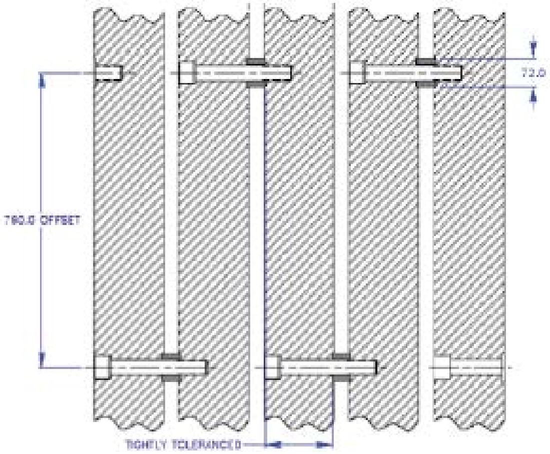
Muon System

Barrel - two orthogonal planes of strips

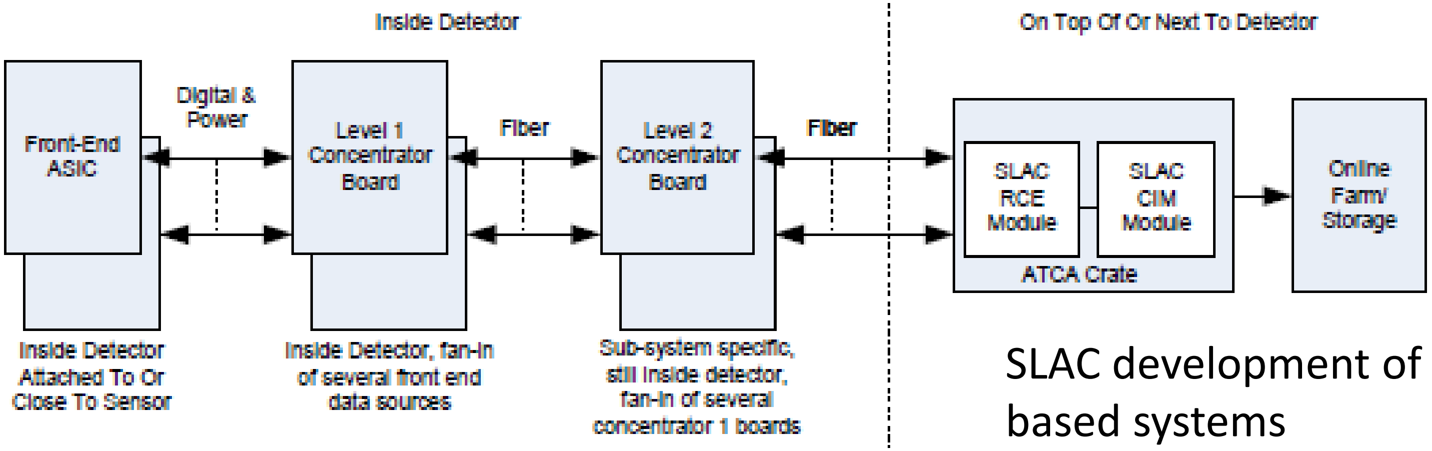


Endcaps – modules slide between spacers/steel layers



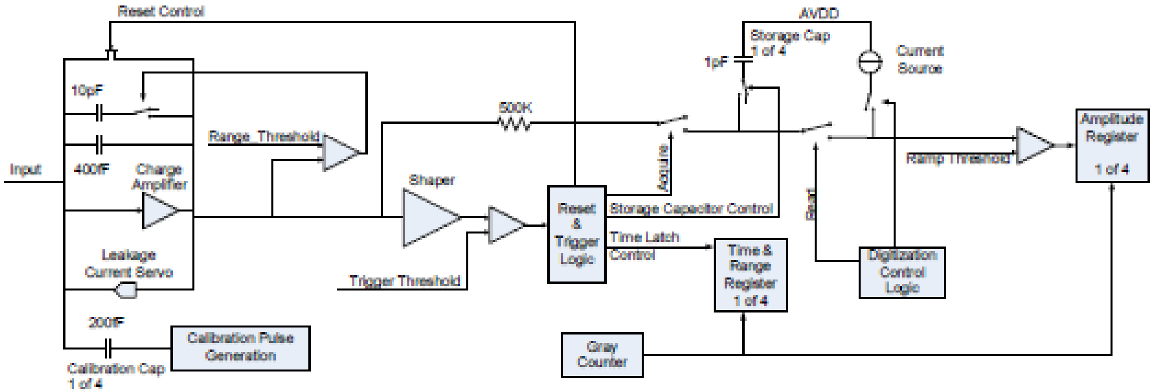


Electronics and DAQ



SLAC development of ATCA-based systems

KPiX schematic



Versions of KPiX will be used for all subsystems except VTX and the high occupancy forward regions.