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RESULTS OF A BEAM TEST OF A LARGE MICROMEGAS TPC PROTOTYPE WITH 6 MODULES

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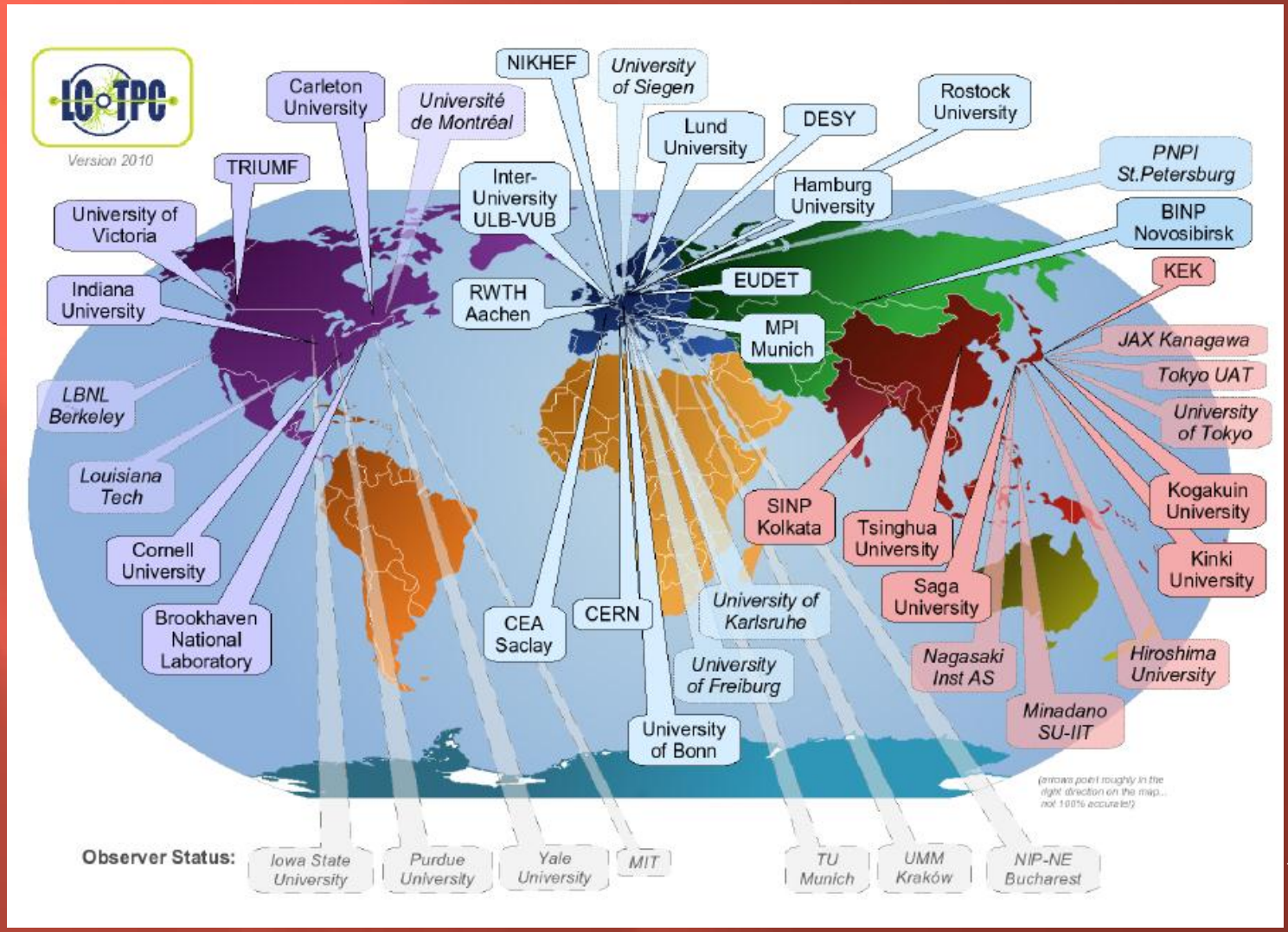
A. Robichaud, J. Timmermans, W. Wang

All the R&D is gathered in LCTPC



38(*) member + 7 observer institutes from 12 countries

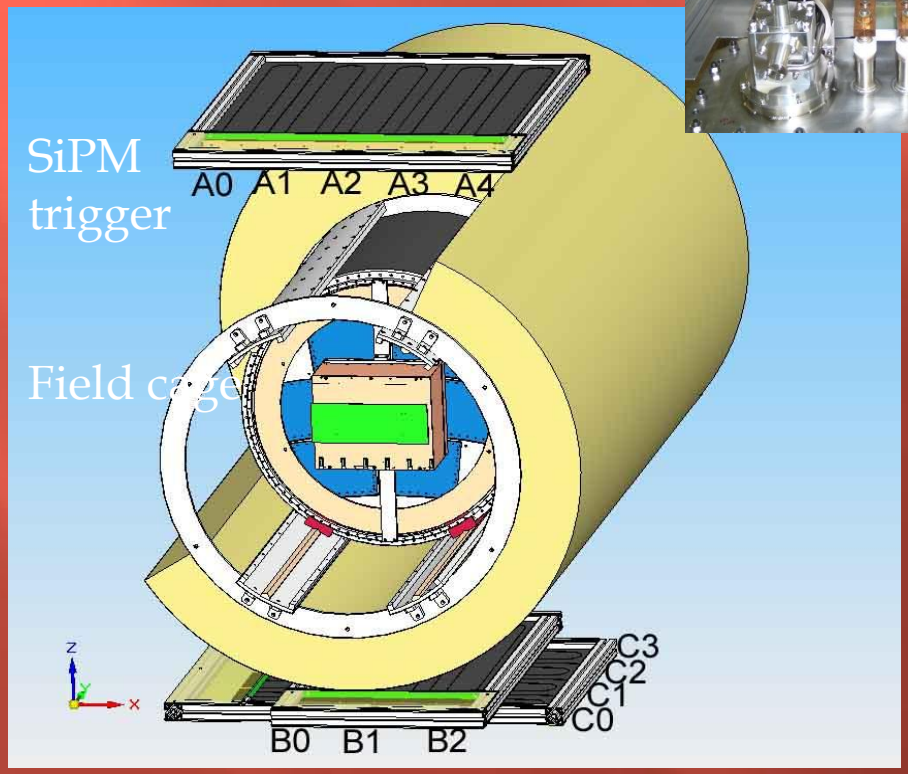
(*) 25 signed the MOA

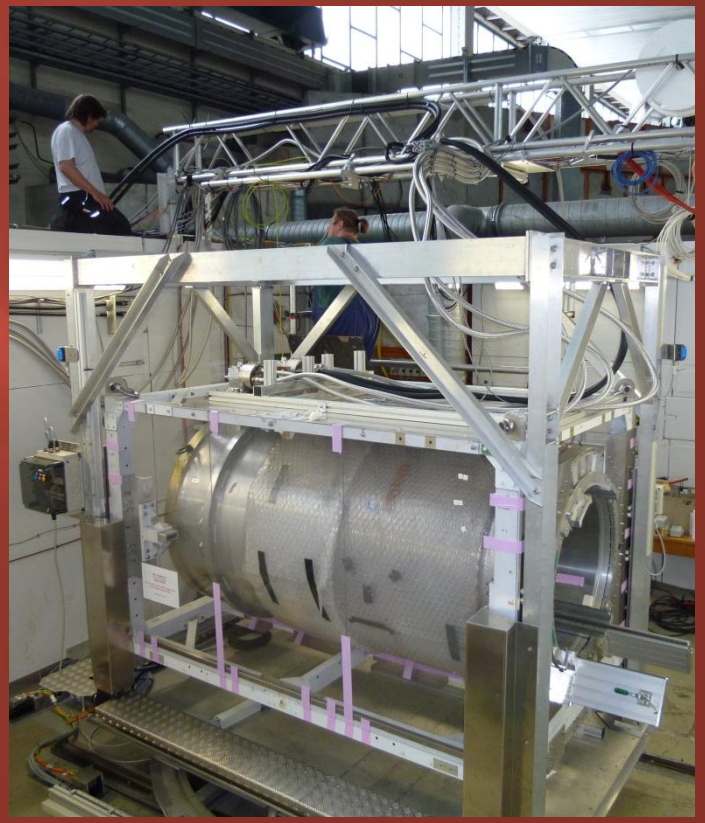
www.lctpc.org

The EUDET test setup at DESY

The EUDET (FP6) setup at DESY is operational since 2008

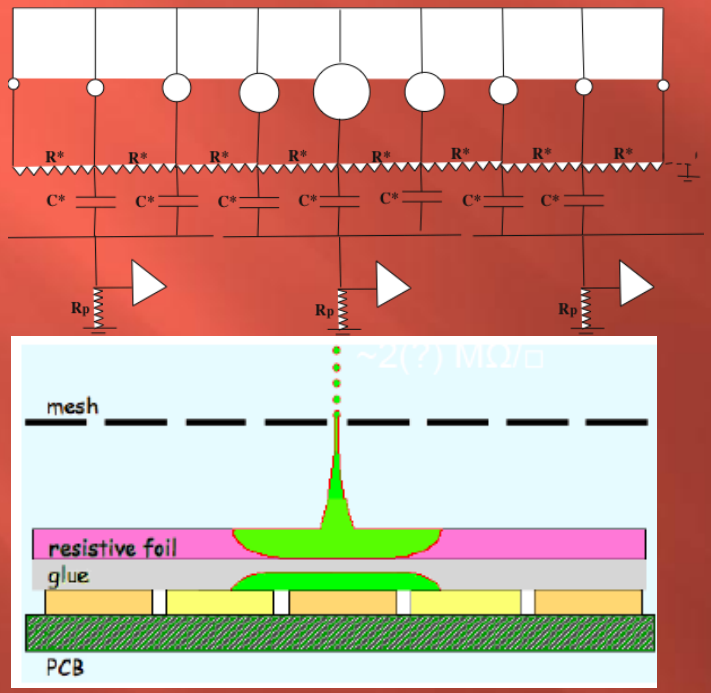
Upgraded within AIDA (FP7): autonomous magnet with 2 cryo-coolers since July





Charge spreading by resistive foil

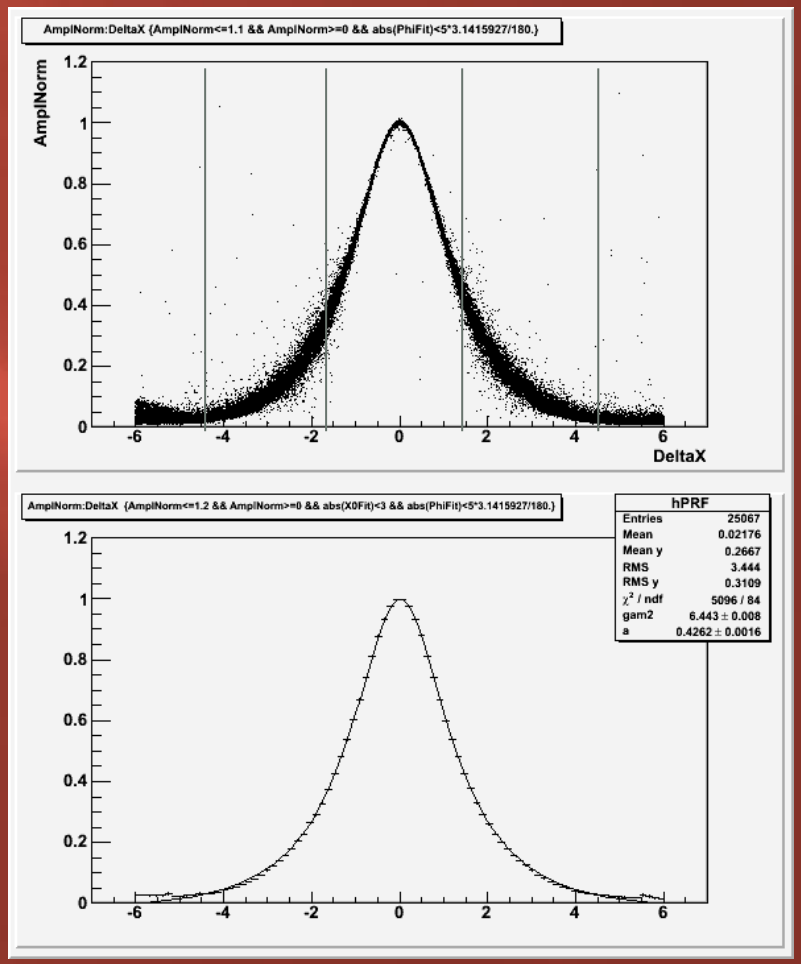
Resistive coating on top of an insulator: Continuous RC network which spreads the charge from σ(avalanche)~15μ to mm: matching pad width improves position sensitivity



M. Dixit, A. Rankin, NIM A 566 (2006) 28

PAD RESPONSE: Relative fraction of 'charge' seen by the pad, vs x(pad)-x(track)

Z=20cm, 200 ns shaping



x(pad) – x(track) (mm)

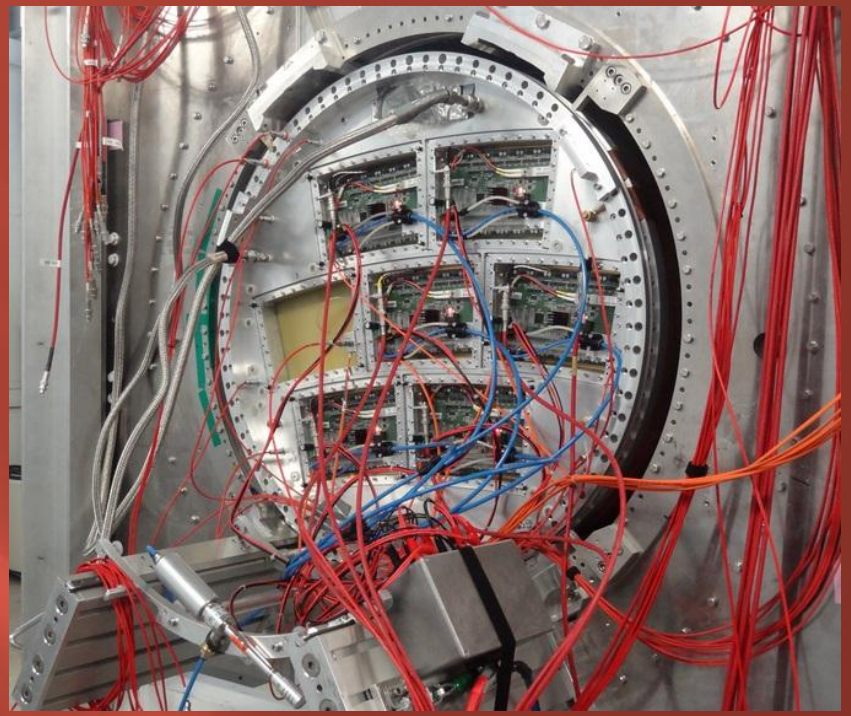
D. Calvet et al., IEEE Real Time 2012

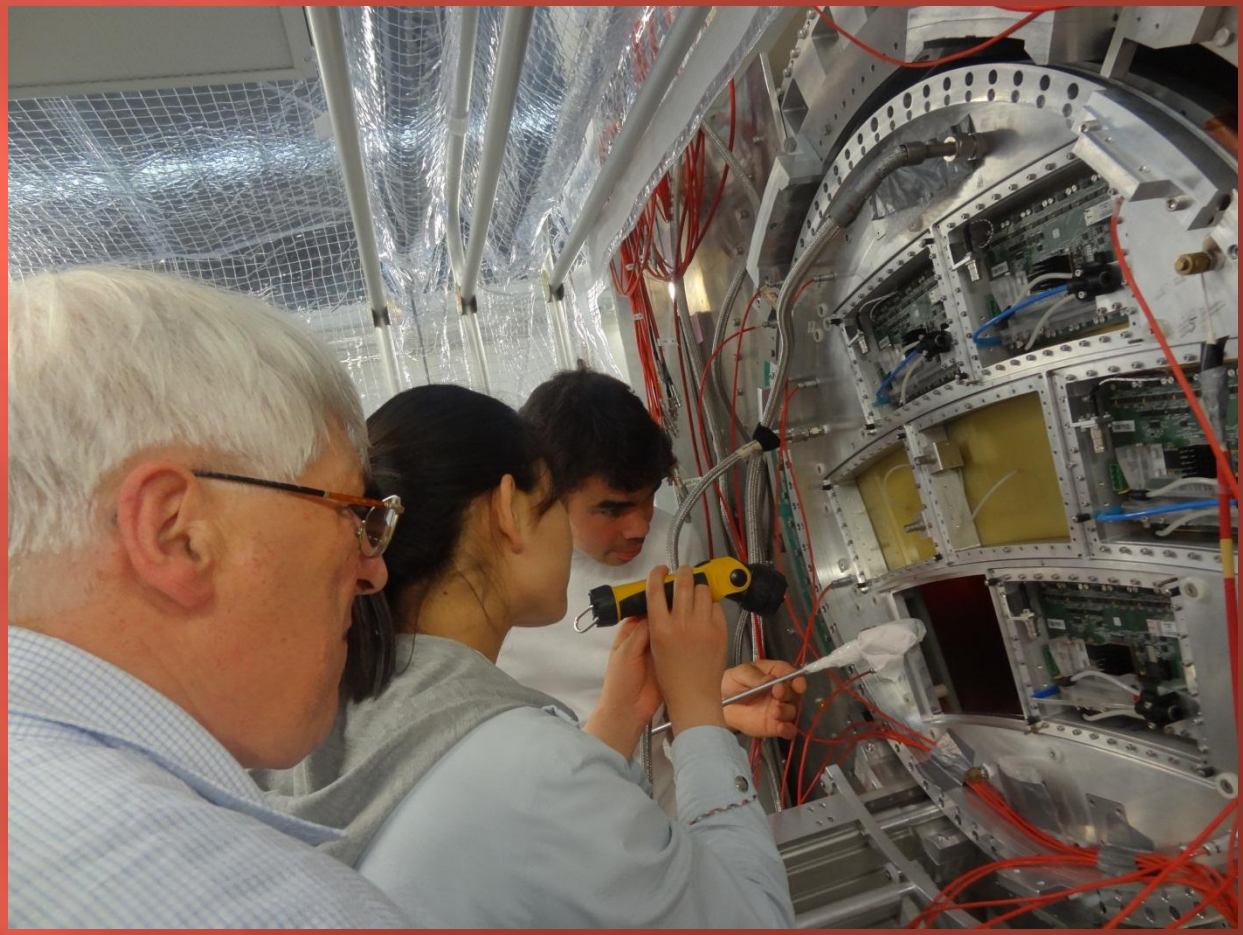
Integrated electronics

- New detector : new routing to adapt to new connectors, lower anode resistivity (3 MΩ/sq), new res. foil grounding on the edge of the PCB.
- New 300 points flat connectors (zero extraction force)
- New front end: keep naked AFTER chips and remove double diodes (count on resistive foil to protect against sparks)
- New Front End Mezzanine (FEMI)
- New back-end for up to 12 modules
- New DAQ, 7-module and more compact format
- New trigger discriminator and logic (FPGA).

The multi-module configuration allows new studies :

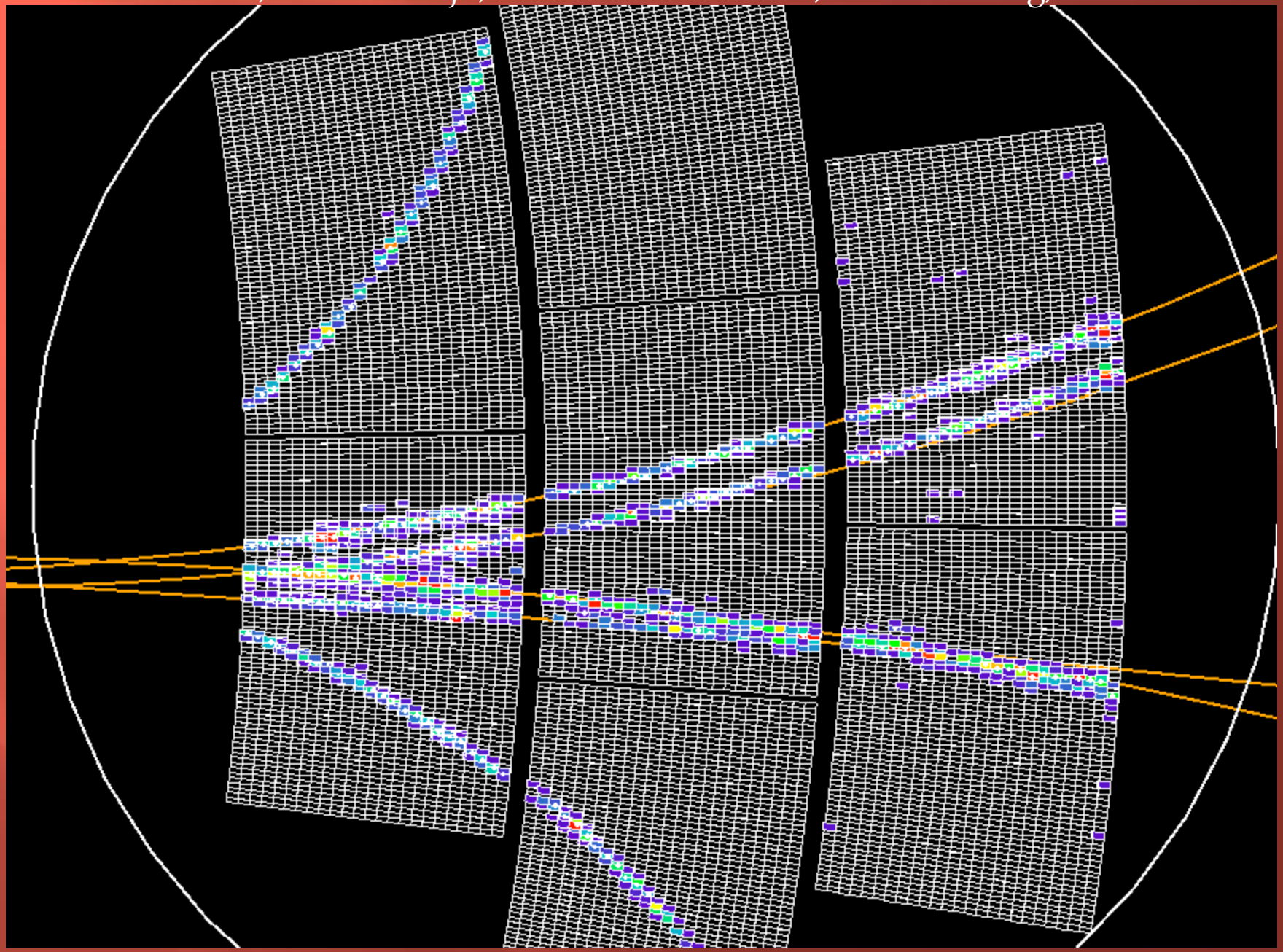
- Performance in cracks
- Module misalignment
- distortions



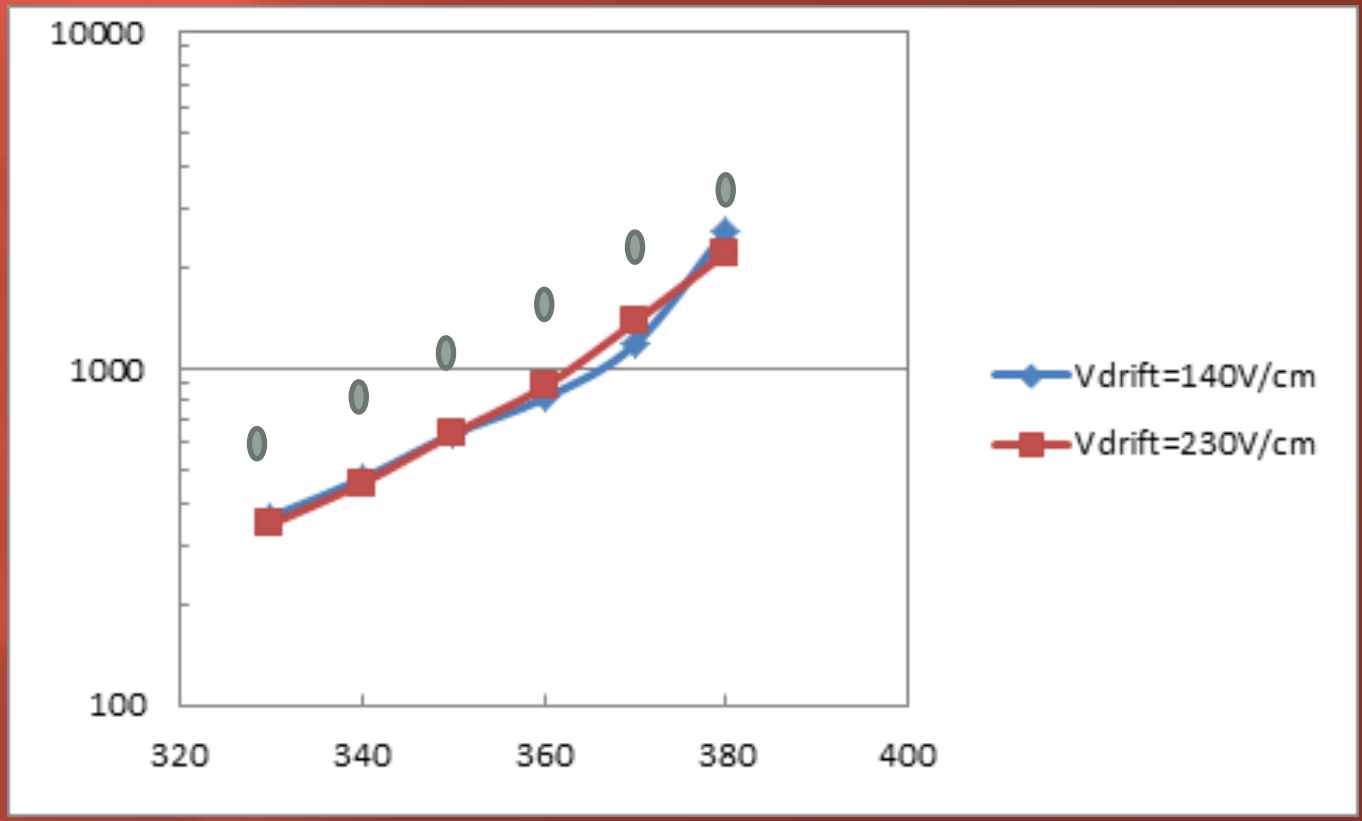


Smooth data taking in July, with over 1 000 000 evts. Air cooling and temperature control. However 6 modules only, 2 of them prototype or pre-serie, imperfect contacts

Thanks to Bo Li, Keisuke Fujii, Gilles de Lentdecker, M. Killenberg,…

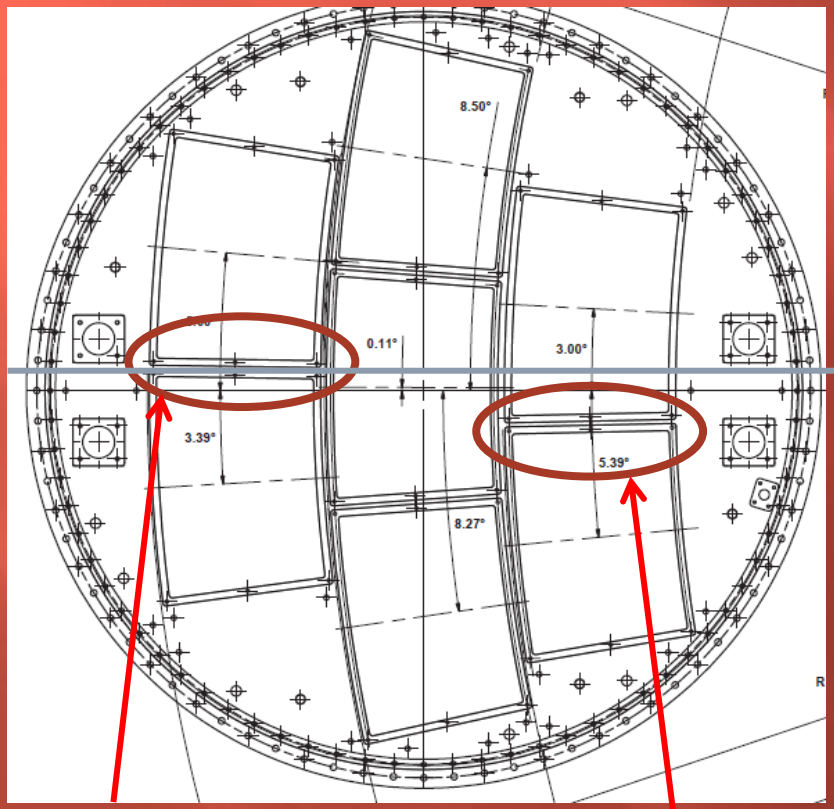


Effective gain vs mesh voltage is measured by using the fitted MPV of the (Landau) distribution of the measured charge. It compares well with direct gain measurements with a 55Fe source on a detector without resistive foil (x2 lower)



Crack scan

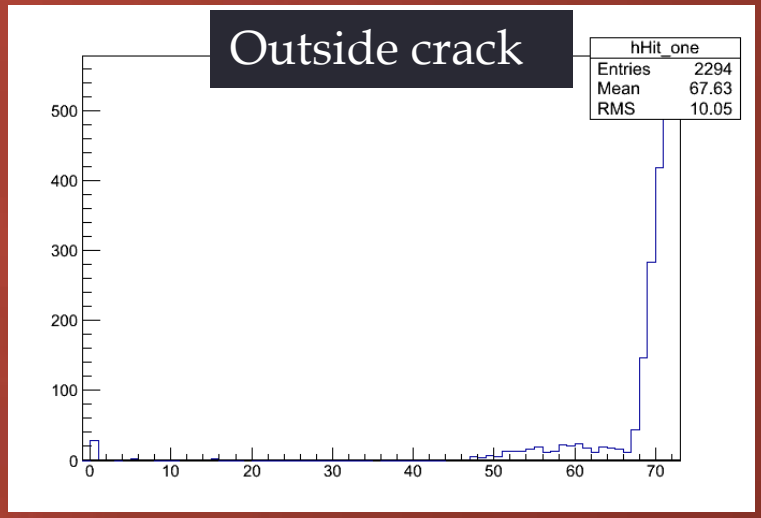
Study the hit reconstruction efficiency at or near the crack: take data with beam, moving by steps of 2mm

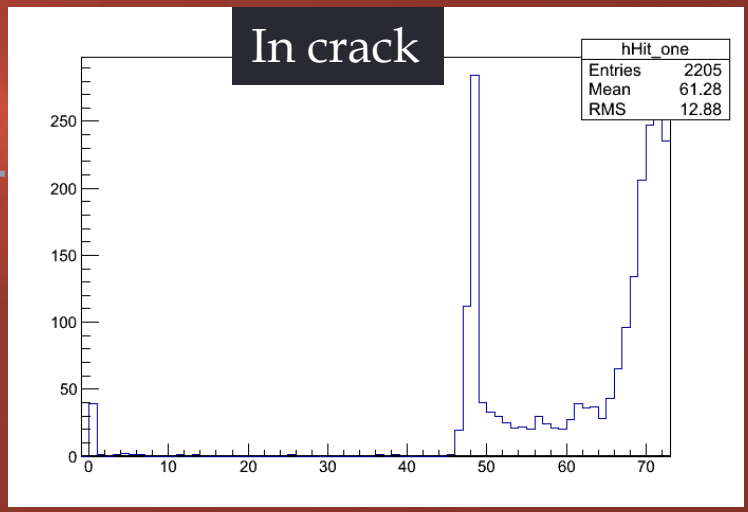


Beam direction

Upper crack

Lower crack

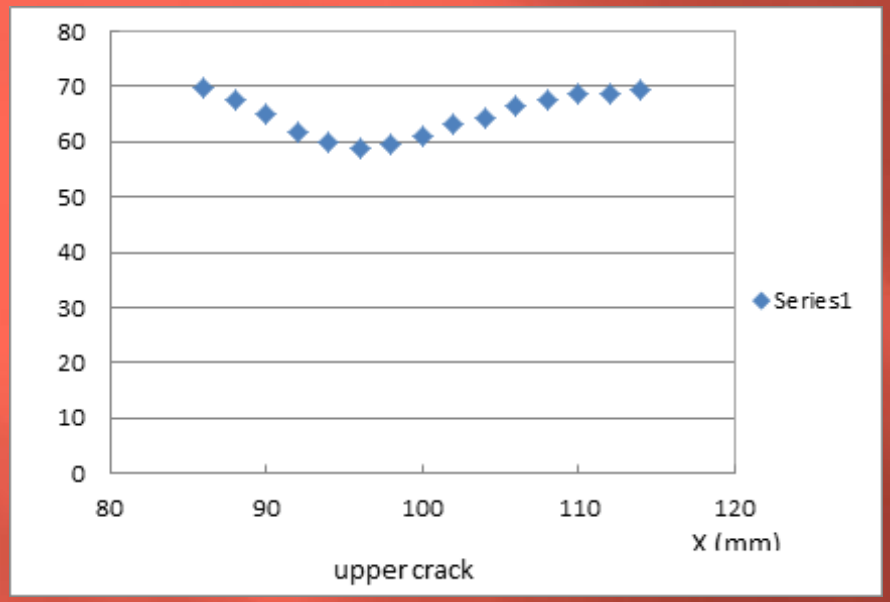


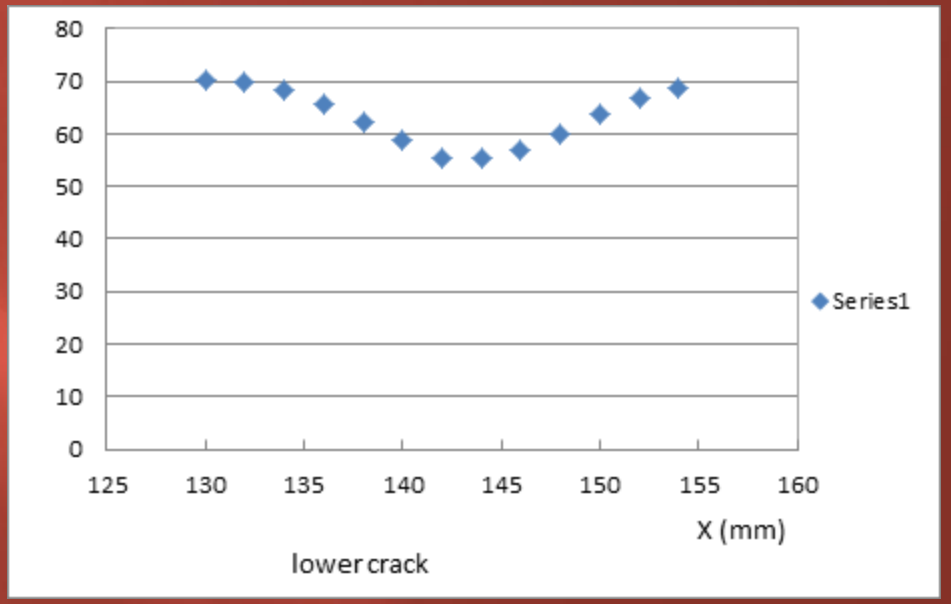


Padrow number (3x24=72)

Hits with ADC>150, 1-track evts

Crack scan

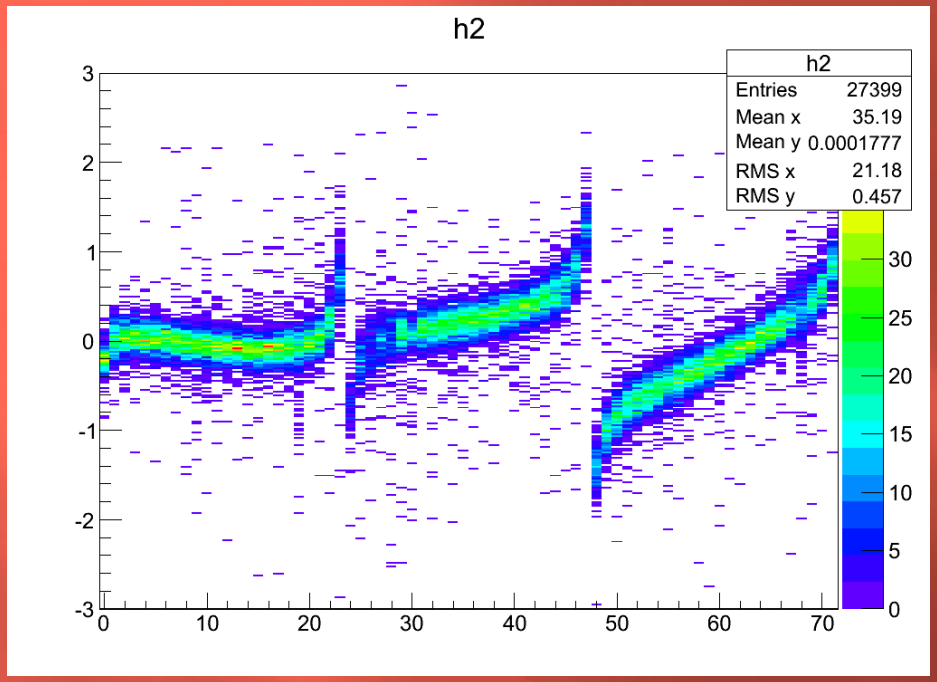


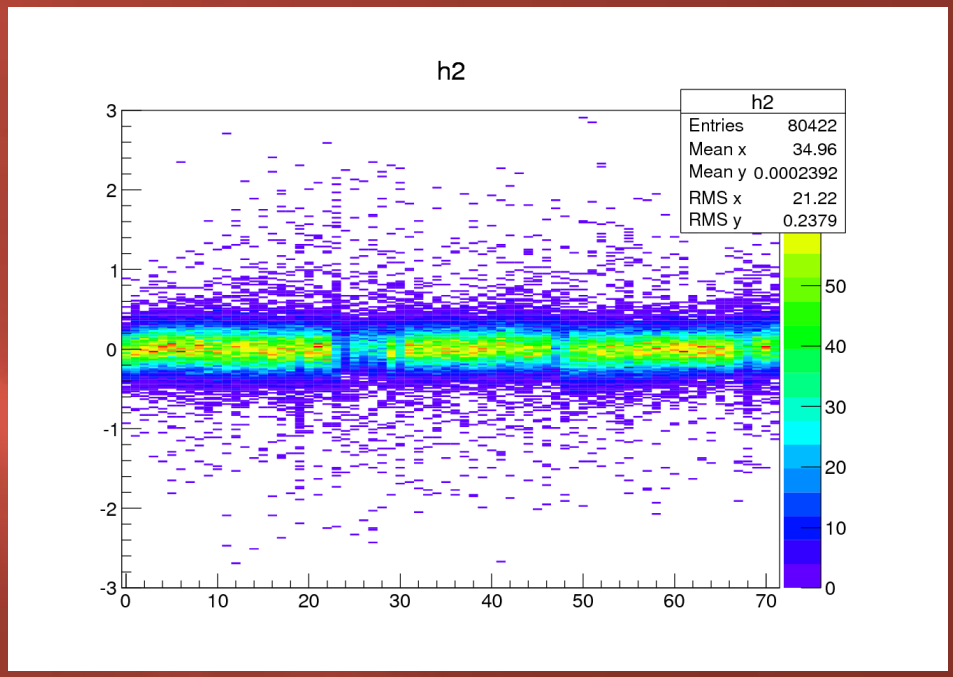


Number of hits vs x

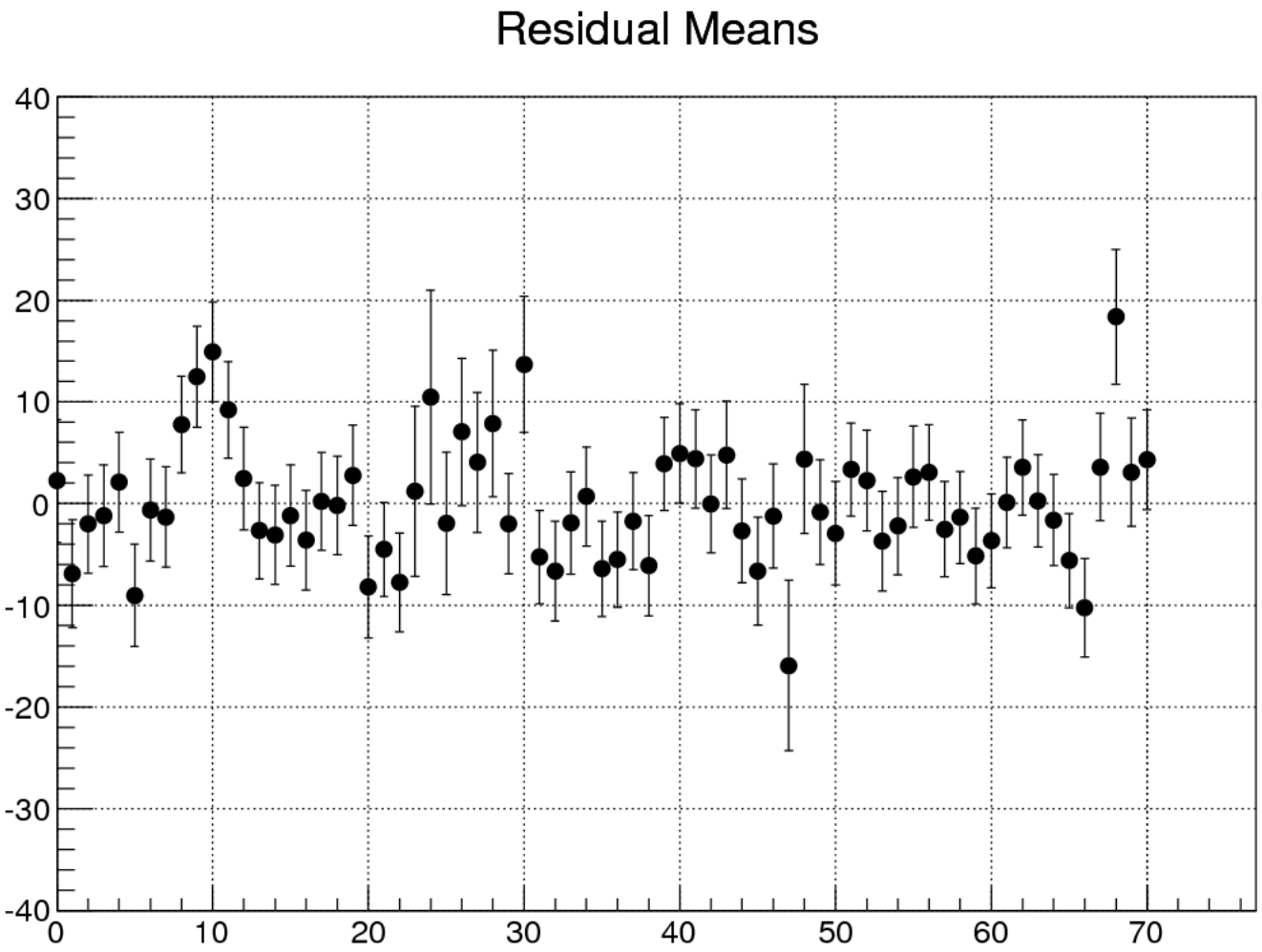
Effect of cracks is felt in an area ~1cm around.
In the worst case, 50% of the hits are lost

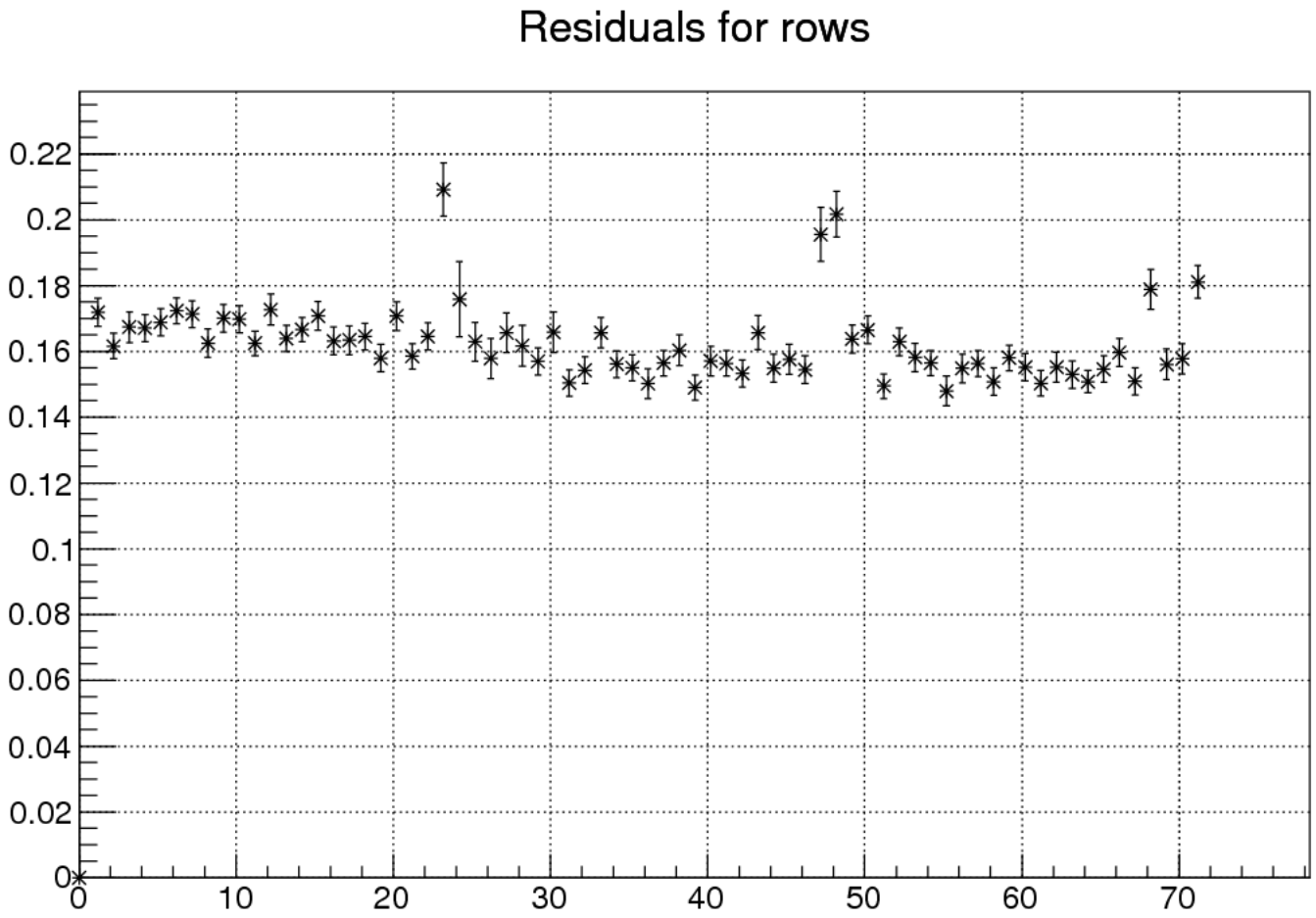
Brute force alignment





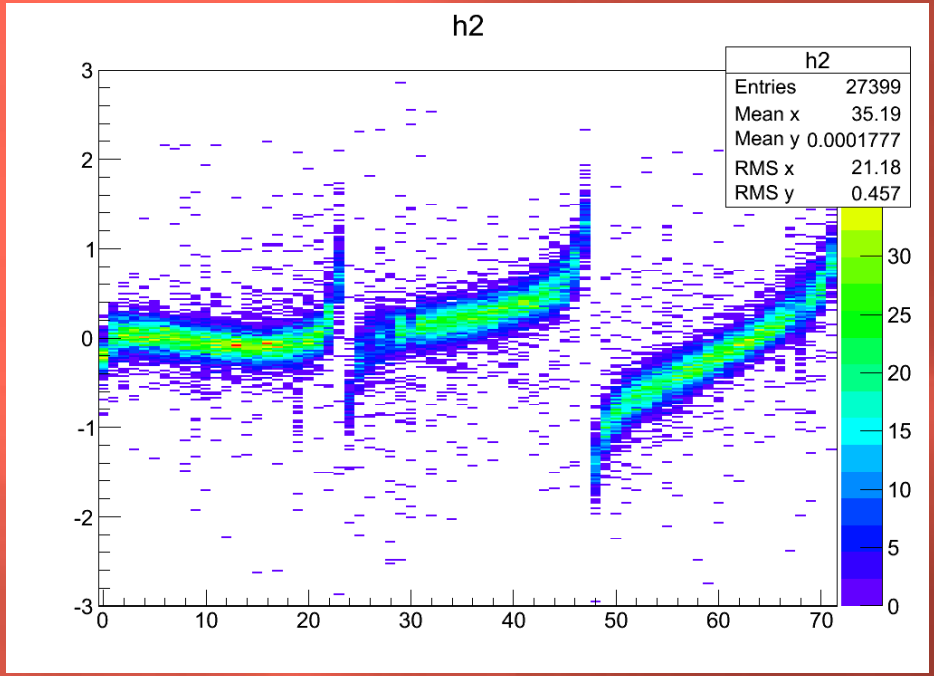
ROW NUMBER : 3x24 = 72
Displacement in mm

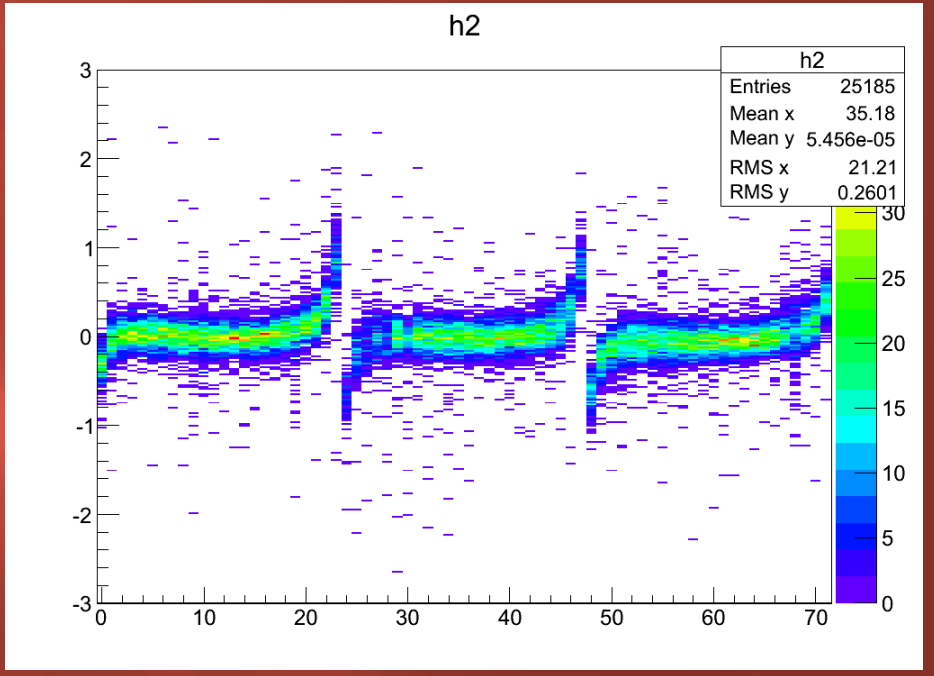

Residual Means
40
30
20
10
0
-10
-20
-30
-40
0
10
20
30
40
50
60
70


Residuals for rows
0.22
0.2
0.18
0.16
0.14
0.12
0.1
0.08
0.06
0.04
0.02
0
0
10
20
30
40
50
60
70

Alignment

Z=10cm





Fitted displacement :
Rotation :
$\delta\phi$ = -1.7 mrad, 3.7 mrad and 8.4 mrad
Translation:
δx = -54 µm, 180 µm and 278 µm

After alignment : only distortions remain (probably ExB effect)

Maximum effect of distortions 400µm

On-going electronics developments

GdSP : gaseous detector signal processing (or Go digital as Soon as Possible) CERN-based collaboration lead by Paul Aspell, including Saclay: F. Guilloux and E. Delagnes, continuing S-ALTRO evolution.

Common development for CMS GEM µ-chambers and LC TPC. Recently considering ALICE upgrade (GEM TPC and µ chambers).

Main developments : 130 nm technology, 64 or 128 channels, low noise and ultra-low consumption, many power domains to ease power switching

First Si test to be submitted in February 2013 (AIDA)

Goals for the FE: for 10 pF detector capacitance and 100 ns peaking time ENC<900 e- and power < 1mW/ch

Front End specifications

Parameter	VFAT2 (IBM 0.25)	SALTRO (IBM 0.13)	VFAT3 / GdSP (IBM 0.13)
Linear range	+- 12fC	150fC	Max 200fC
Input capacitance (pF)	20	0-20	5 – 10 – 30 – 60
Noise	~500e- ⊕ 40-60e-/pF @ 25ns	~ 650e- ⊕ 15e-/pF @ 120ns	< SAltro / VFAT

From Paul Aspell

Starting from data measured on ABCN (130nm design by Jan Kaplon for ATLAS SCT):

** 800 e- @ 5pF, tp=22ns, 100µW*

** assuming serie noise only + strong inversion for the input transistor*

➔ ***we can hope 530 e- @10pF, tp= 100ns, 200µW***

➔ ***Ultra Low power low noise design seems feasible*** *(cf slide 6)*

Parameter	VFAT2	SALTRO	VFAT3 / GdSP
Power (mW/channel)	1.5 (IBM 250nm) (incl. comparator)	10	<< 1

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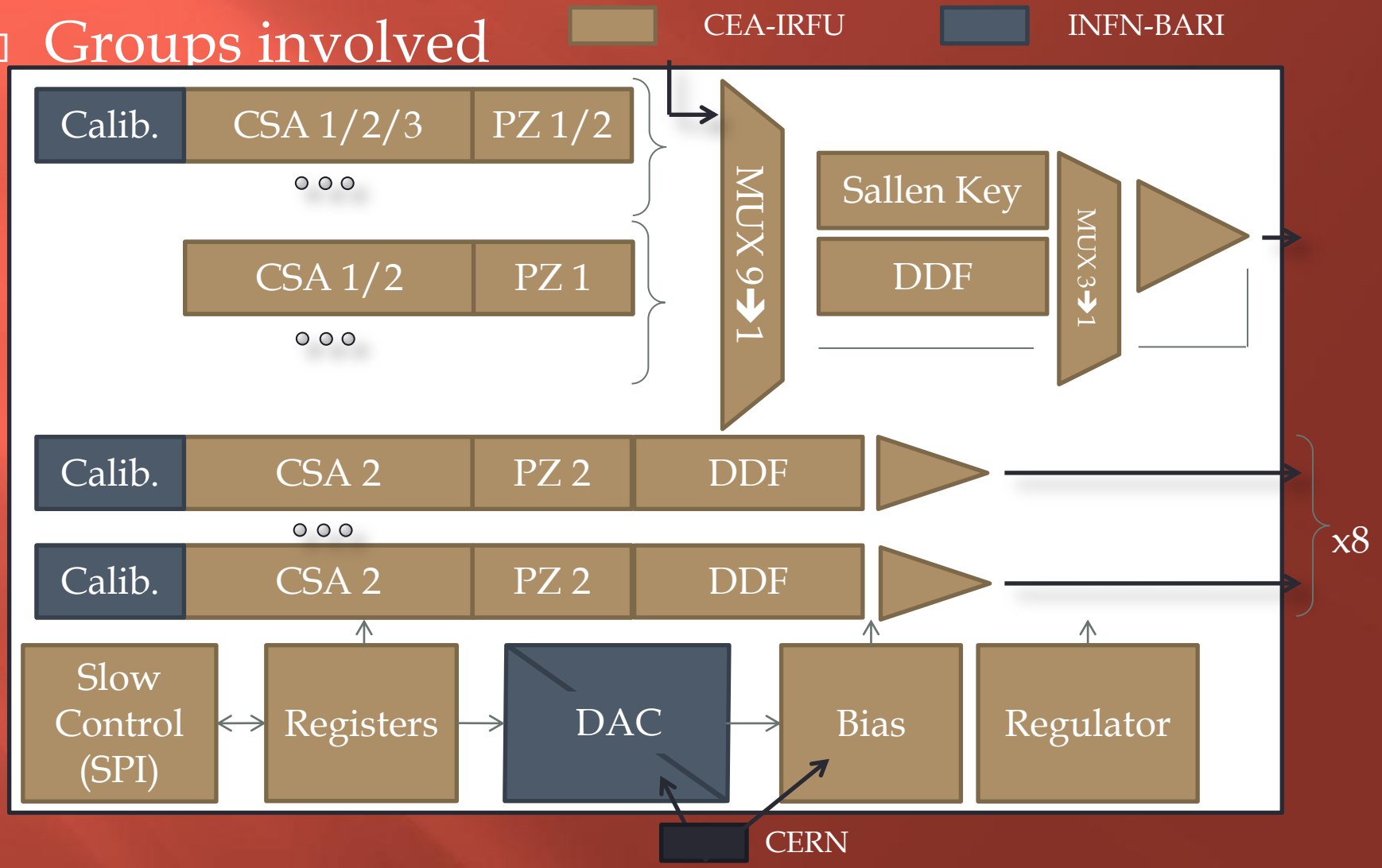
Proposal for CFE

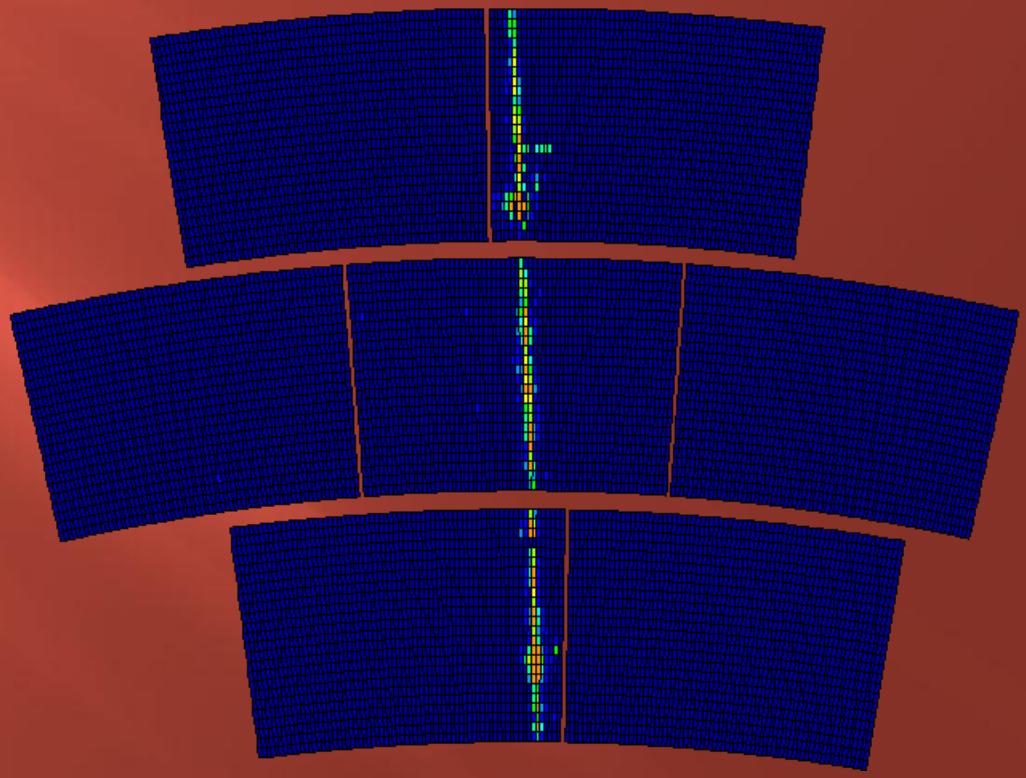
- Groups involved



Summary

Successful test of 6 modules at a time

- Most integration questions addressed
- Improvements needed in contacts of the flat connectors
- Multi-modules aspects addressed: alignment, reconstruction



Next step: 7 modules high quality test, full calibration on the test bench, detailed analysis in 2013-2014

R&D projects: thinner meshes, other charge dispersion devices (ceramic with ruthenium oxide).

Then a larger module with smaller pads for the inner wheel.

Thanks to our DESY colleagues, especially Ralf Diener, Christophe Rosemann and Felix Müller