So far So Good, but Certainly Some Issues

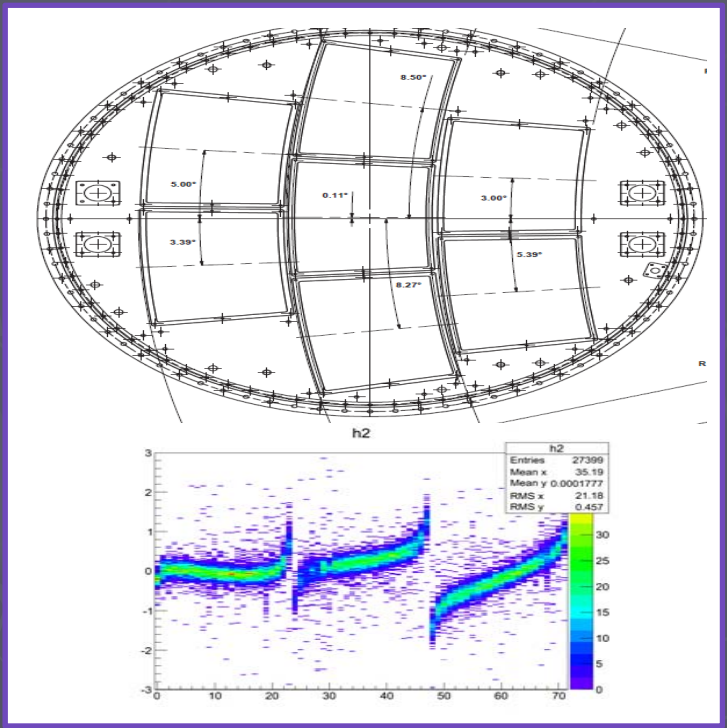
(Three slides for this monthly meeting)

1. Distortions at the module boundaries: "The traditional TPC Problem"

   Now a common issue for all GEM and Micromegas modules.

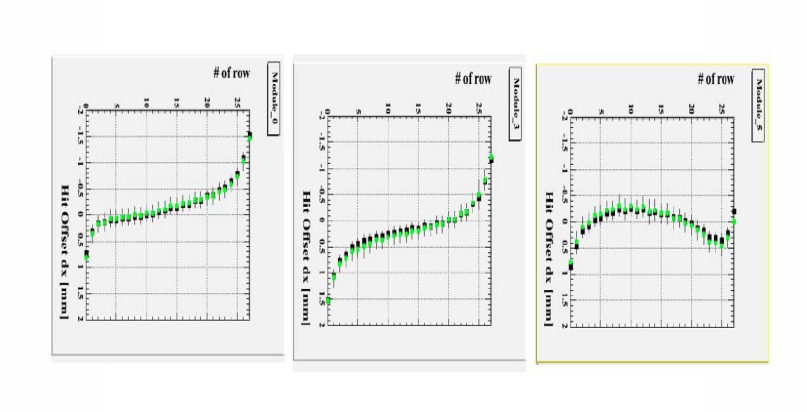
   Any structure/surface of module of O(1 few 100micrns) where E-potential not well-defined may cause the distortion.

   Need to control E-filed down to O(100-200microns) instead of a few mm!



Micromegas case

Non uniform B-field, and
Boundaries of modules



Asian GEM case

Non uniform B-field,
Boundaries of modules,
Wrong field shaper setting, and,
Metal structures on the module

Also for DESY module

Trying some measure with additional strips

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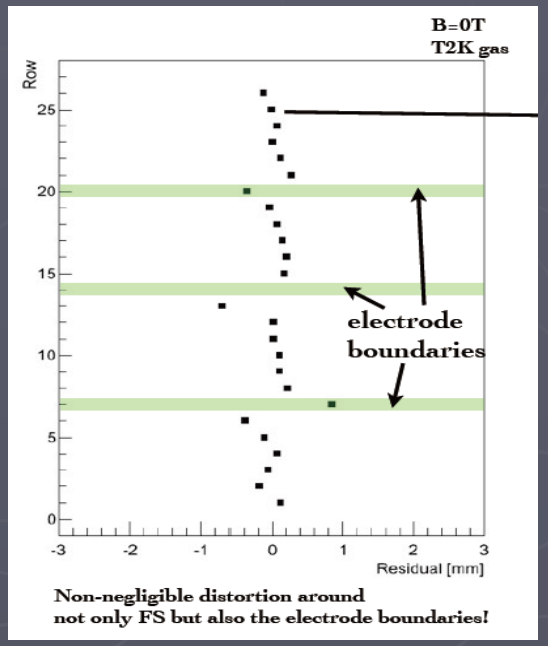
2. Distortions at the bounadairs of GEM electrodes:

The recent test of an Asian GEM module using a laser system shows a similar but smaller (B=0) distortion pattern at the boundaries of the GEM electrodes , which are divided into 4 sections to minimize the capacitance.

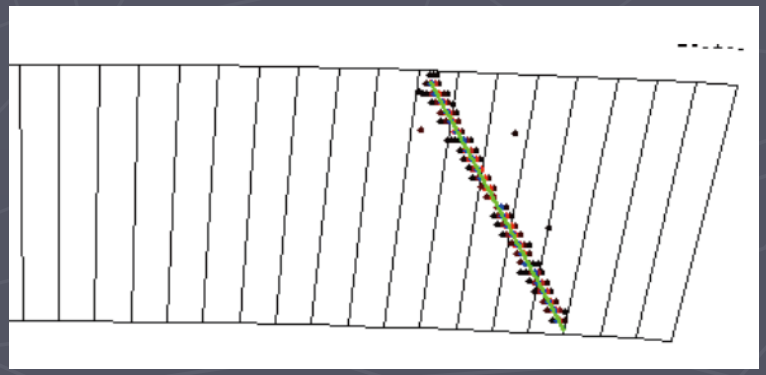
The problem is that the gaps between the electrodes are O(1mm) instead of O(100microns)!



Kurihara
Yatukawa
Kwaguchi
Yonamine

The real craftsmanship!

"3D alignment of the laser light", but Nice results with laser!



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3. Over-all dead time of the ILD TP due to the discharge: w/ or w/o RA

MWPC TPC had essentially no efficiency loss due to the discharge.
MPGD is the subject of discharge (Good GEM: 10^{-7}, Micromegas: 10^{-4}/track)

Micromegas with the Resistive Anode (RA) will be free from this problem:
The discharge is localized by RA and do not lead to a large voltage drop of the whole mesh. Though need to check the pile effect of signals due to the slow signal spread in RA if it might become a problem in high occupancies for 100microns resolution.

In the case of GEM, it depends on the discharge rate, total No. of GEM segment, the duration of discharge (voltage drop) etc. (while the response of GEM has no time dependence and very straight). RA is possible with the same issue.

4. An Ion gate:
Big impacts to the mechanical design of the module and TPC in the case of an wire gate

5. Detailed and careful (engineering) design of all components of ILD TPC