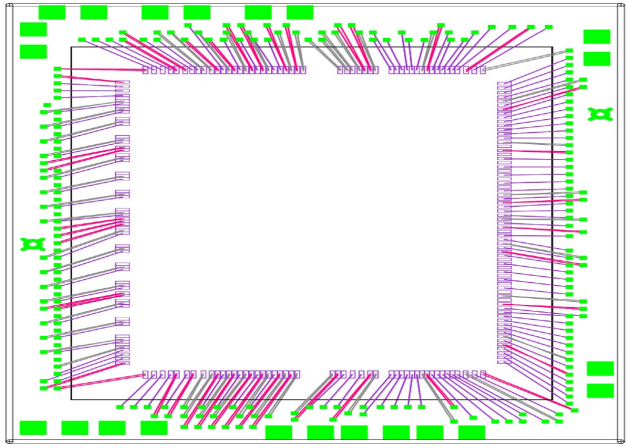
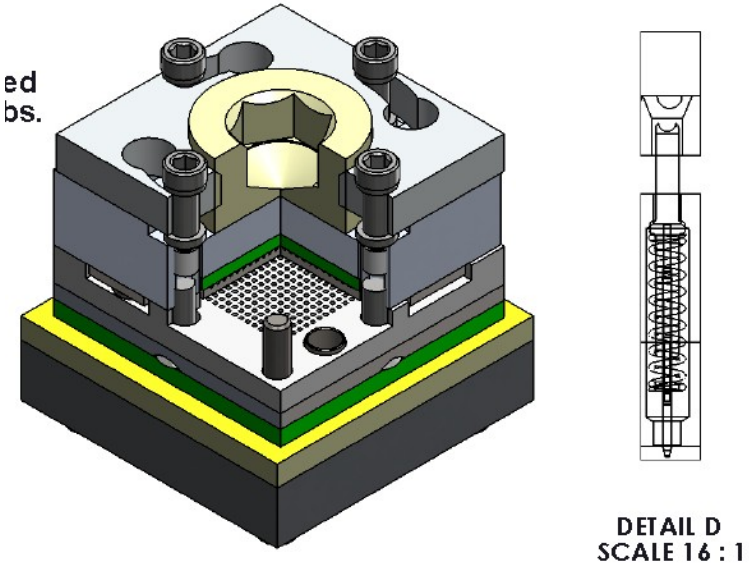
Status of the SALTRO-development in Lund

1) Carrier board



Size: 12.0 x 8.9 mm^2 (die; 8.7 x 6.2 mm^2)
Design ready, final modification due to power pulsing
Specification document ready
Contact with company for mounting components has been established and final discussions are ongoing
Bids for production of boards awaiting

2) Test socket for testing SALTRO-chips on carrier boards



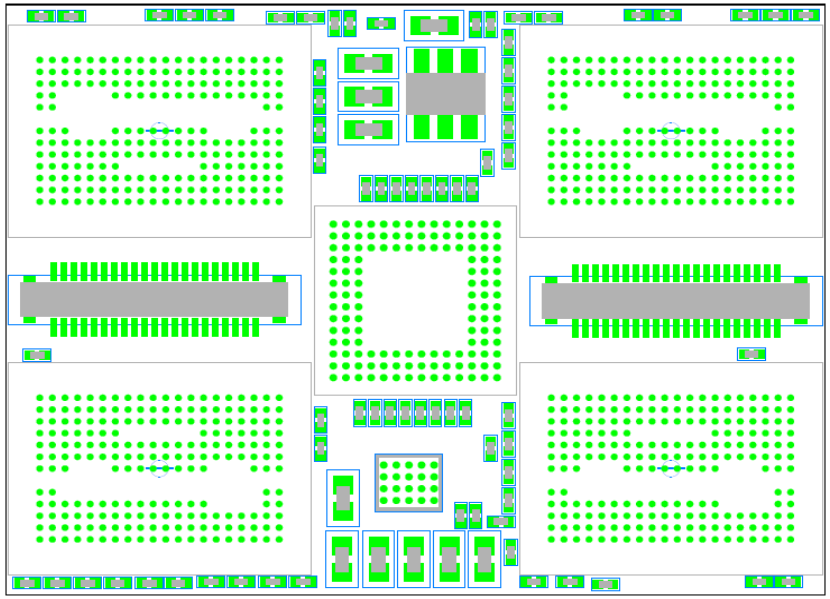
Contact with company established
Will be ordered as soon as we get green light from the company mounting the components on the carrier board

3) The MCM-board

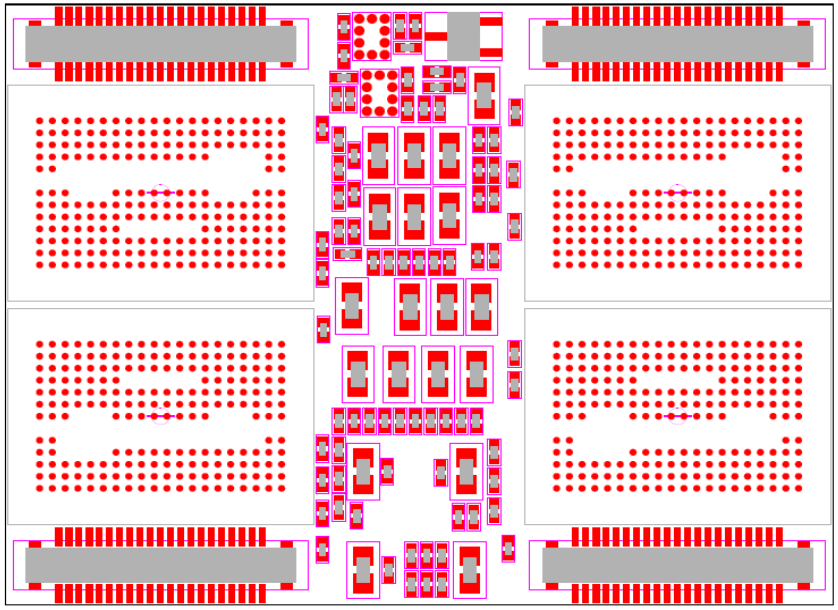
Size: 32.5 x 25 mm^2
The main components on this board are:
8 carrier boards, connectors to the pad plane, a CPLD, connectors for data transfer and LV-support

Layout almost ready; type of CPLD still to be decided as well as connectors for LV support and data transfer and how the power pulsing will be handled.
The power pulsing will only switch of the SALTRO chips
Power consumption 12mW at 5 Hz (compared to 757 mW by continuous running)

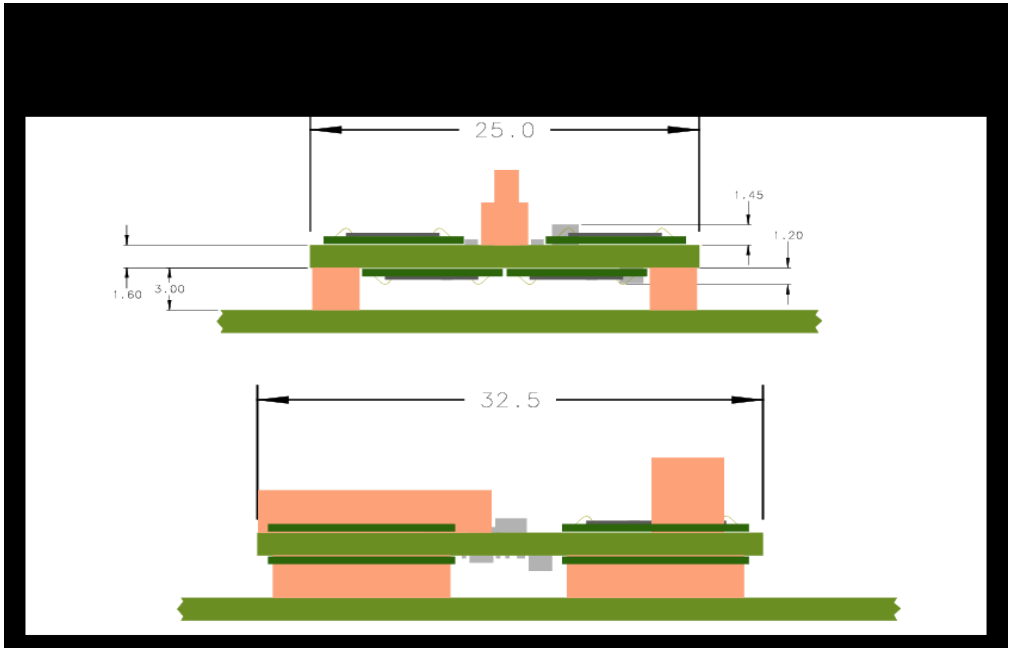
Top side



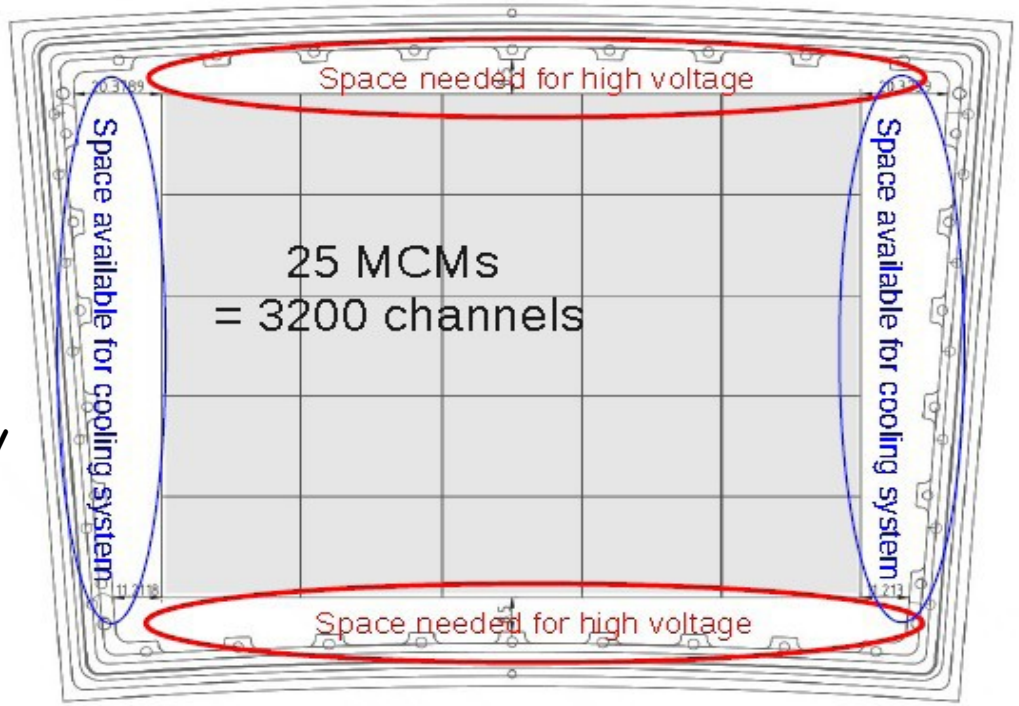
Below side



Side view of the board assembly
Since it was necessary to add two layers (8 instead of 6) the carrier board has become 0.2 mm thicker.
It means that the available space
For cooling planes between the MCM and the pad plane is 1.6 mm.



Organization of the MCM-boards within a module
3200 channels corresponds to a pad size of 1 x 8.5 mm if the whole area of the module is covered.
The construction of the pad plane and the cooling system is the responsibility of the Japanese groups



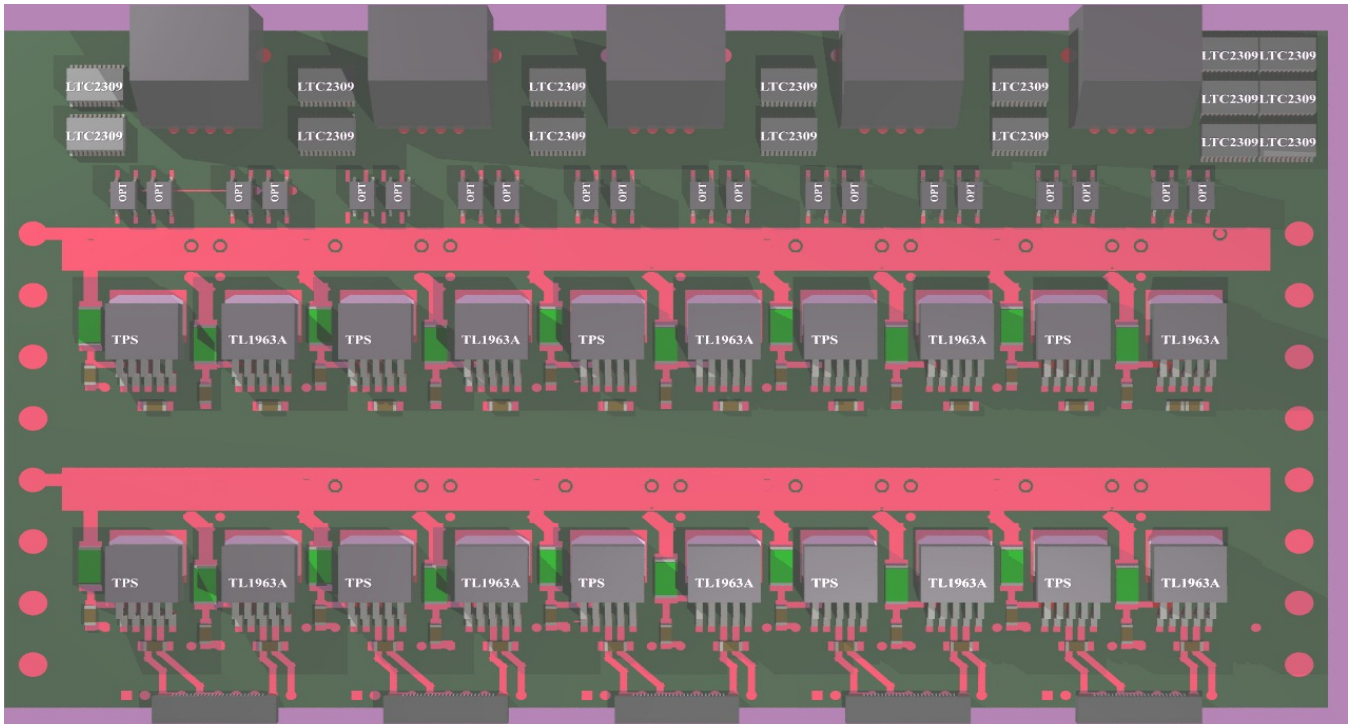
4) LV-board

1st design made. However the number of voltage regulators needed depends on which CPLD we decide to use
Voltage regulators are placed on both sides of the board
Size of the board 184 x 110 mm2

We will implement the following functions: switching on/off the voltage regulators dynamically, monitoring of the voltages and currents, monitoring of the temperature on the LV-board and the MCM-board

RJ45 connectors for serial readout

LV connection



LV connection

Towards MCM-board

Schematic view of the setup with serial readout using an SRU

In the solution shown below the SRU communicates directly with the MCM-board via the Data Trigger Control (DTC) link.
This requires however that the FPGA firmware on the SRU is modified
Depending on the type of CPLD we might need 8 or 9 different voltages