LCTPC (i.e. my) activities @ Nikhef

- 2nd Octopuce board for Saclay module: soon
- "engineering" study of LP module with Ingrids; optimisation of:
  - Geometrical coverage
  - Mechanical precision
  - Readout (Relaxed-like or Spider-like)
  - Room temperature CO2 cooling
  - Minimising material
  - If possible, compatibility with future Through-Silicon Vias connectivity

Rough “planning”

- Pre-study full-scale cooling (6 months?)
- Pre-module with full-scale bare chip readout (12 months?)
  - 1st daughter board with (6 or 8) bare chips (~6 m.)
  - Full module bare chips (6 m.)
- Full module with Ingrids (6-12 months?)