Projects at Bonn

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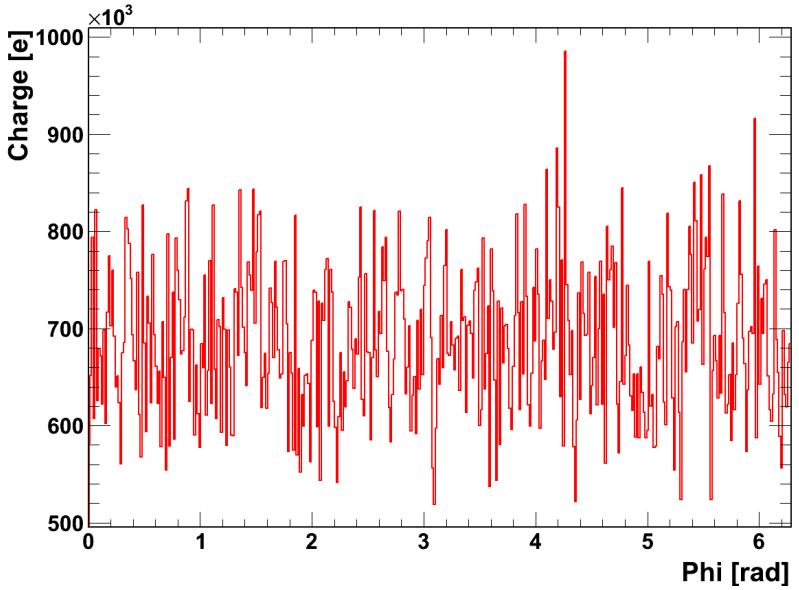
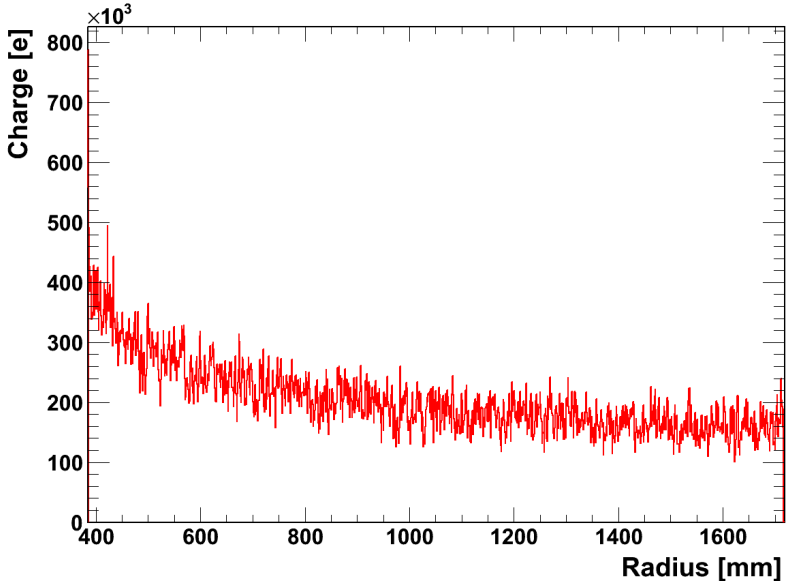
Simulation of Field Distortion

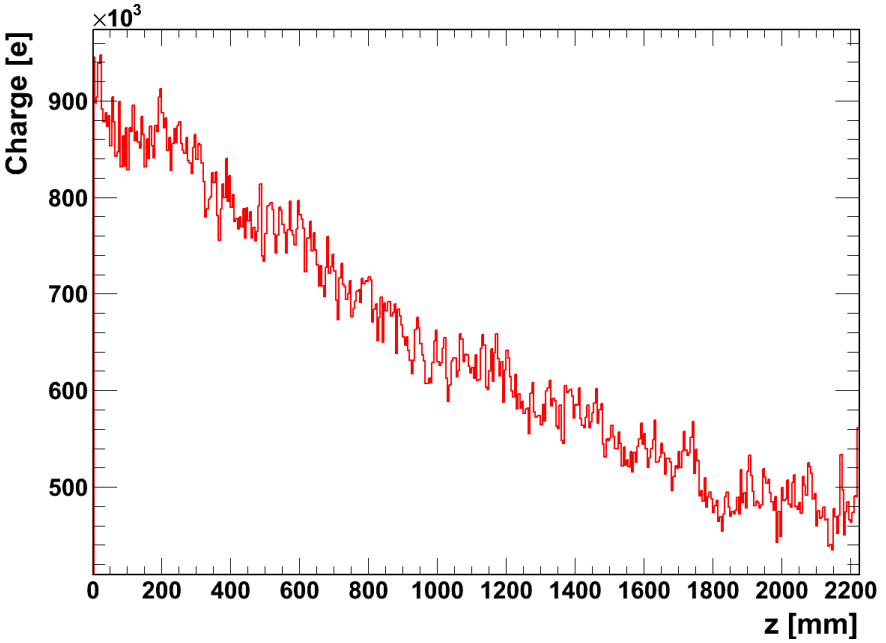
For Details see WP meeting 164
Simulation of charge created by background event

- Background on generator level (pairs and γγ→hadrons) => done
- Full simulation of background interaction with ILD (Mokka)
  - Pairs => done
  - γγ→hadrons => done
- Calculation of field distortions (our own package)
  - Implementation => done
  - Validation with Keisuke's method/code => done
  - Field calculations 2D => needs pair mixing
  - Field calculations 3D => work in progress
- Simulation of tracks in a distorted field for a pixelized readout (mainly MarlinTPC)
  - Implementation and validation => done
  - Simulation => to be done
- Reconstruction of tracks in a ILD scale TPC with a pixelized readout (MarlinTPC) => to be done
- Analysis of the resulting data (MarlinTPC/Root) => to be done

Charge Distribution







Available for pairs (500 GeV and 1 TeV)

Correct mixing of γγ→hadrons missing

- 4.1 evt/BX @ 1 TeV
- 1.7 evt/BX @ 500 GeV

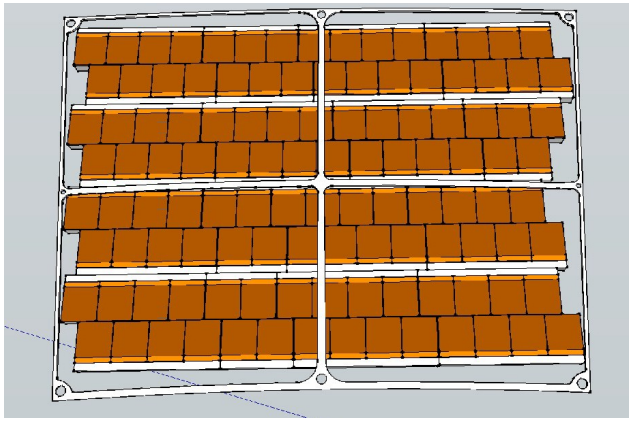
But <u>how to select events</u>?

Pixelized Readout

Near Goal: LCTPC module with one octoboard
one module with triple GEM stack and 8 Timepix chips
one module with 8 InGrid

- Testbeam at LP: 25.03.2013 – 07.04.2013
- Use new readout system: SRS
- Water cooling

- Todo for Testbeam:
  - Solve DAC setting problem with SRS
  - Get octoboard working (2 chips until now, with MUROS)
  - Readout octoboard with SRS
  - Construct mechanics for modules
  - And much more..

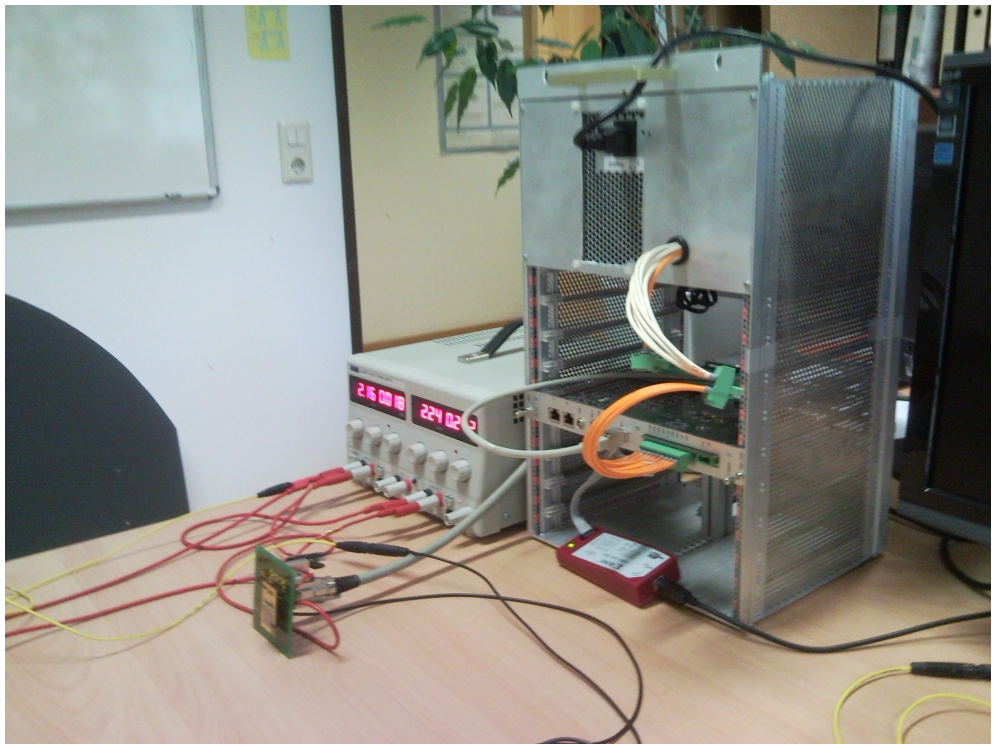


Far Goal: LCTPC module with 96 chips

Readout System based on SRS

The Scalable Readout System is designed by the RD51 collaboration with CERN as a main developer.

Idea: produce a flexible readout electronics, which can handle different chips (new FPGA code, chip carrier), which many groups can use.

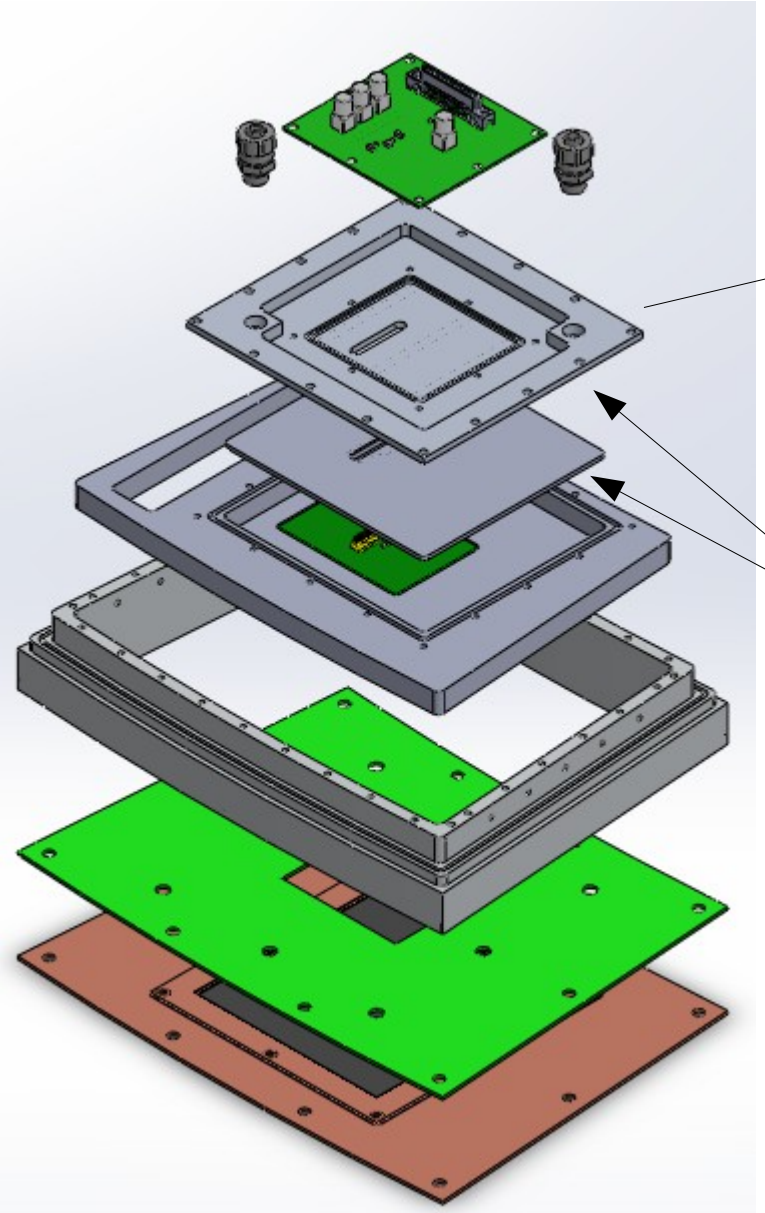


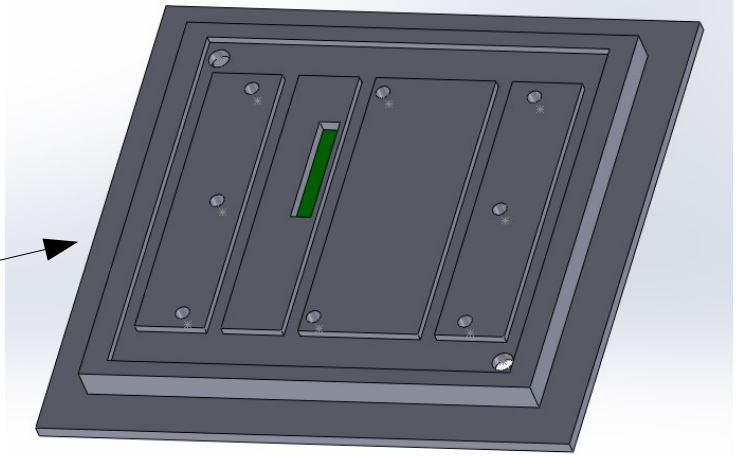
Most of the functionality for Timepix Readout (similar to of the Muros+ Pixelman system) is implemented

- Set matrix and DACs (FSR) (recently discovered bug – hard to fix)
- Read out matrix
- Reset, start/stop measurement, measure with certain shutter length
- DAC scan in Software + osci (no ADC jet)
- Threshold equalisation

Setup with one chip in operation

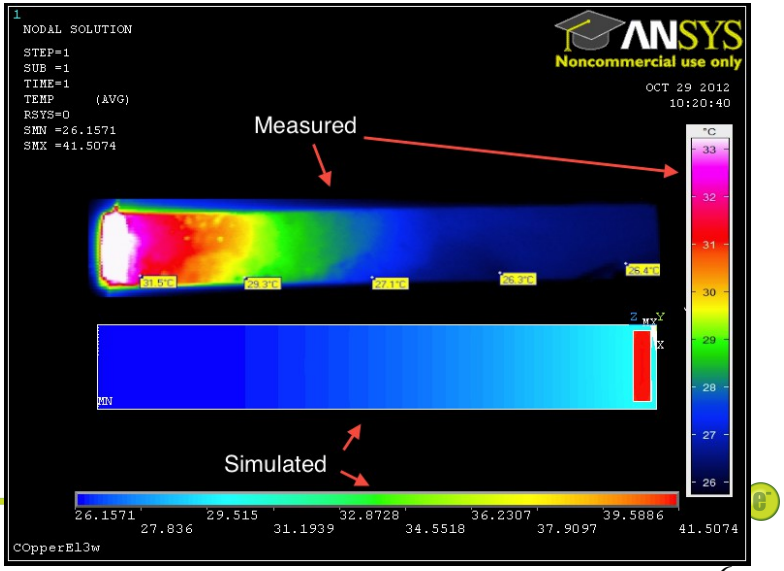
Design of the new Module





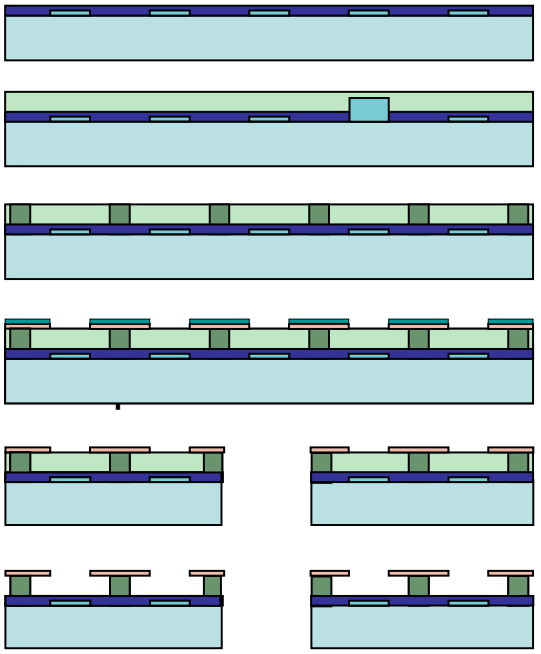
Diffusion welding at Jülich to make tight pipes for water/2PCO2-cooling

Some simple experiment and simulations to understand the heat flow



Wafer-based Production of InGrids

Production of a full wafer (107 chips) at a time.
3 batches have been done, more are planned.



1. Formation of Si_xN_y layer
2. Deposition of SU-8
3. Pillar structure formation
4. Formation of Al grid
5. Dicing of Wafer
6. Development of SU-8