GDCC status

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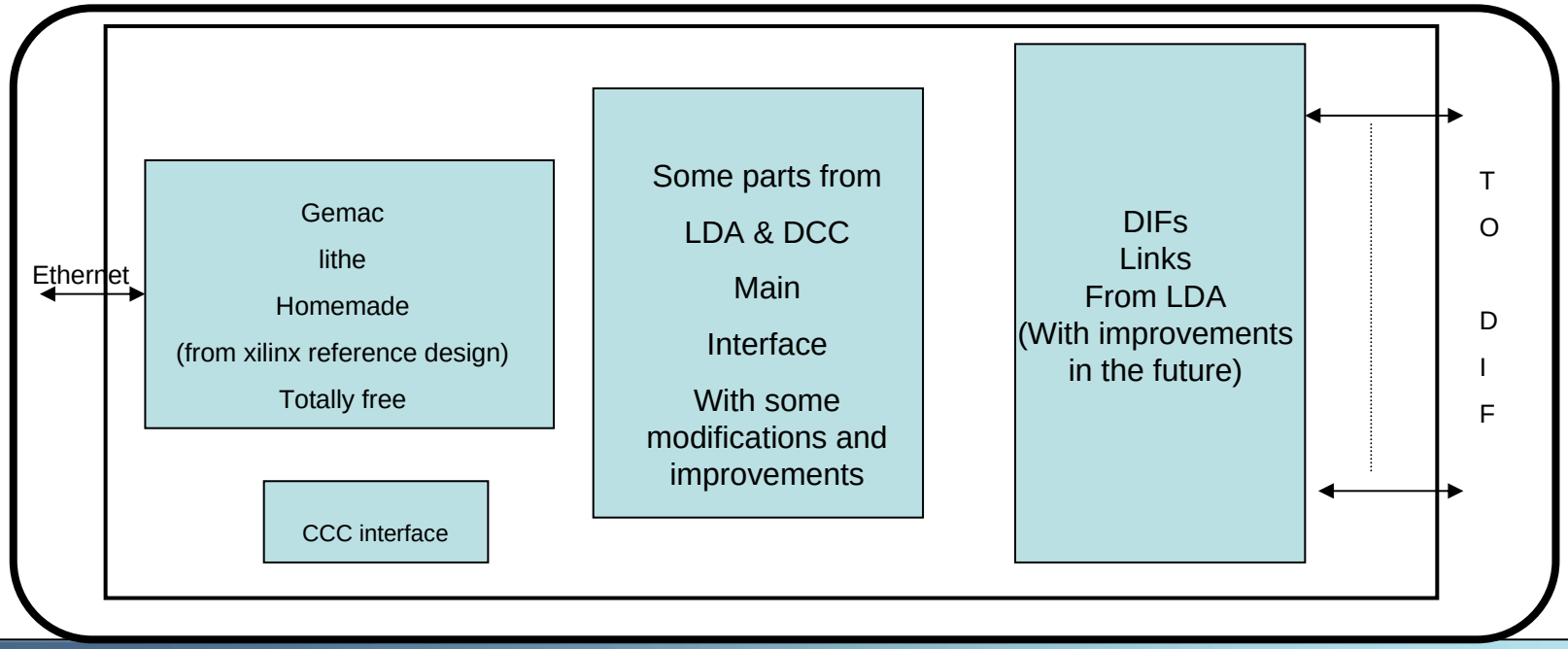
Outline

- GDCC specification
- The board
- The tests
- The improvements
- Planning

GDCC specification

- The behavior is equivalent at the LDA firmware (not modification for the software)
  - The main modification is the MAC interface
    - For the LDA, it's a XILINX IP who is obsolete and must be only used with a old version of XILINX tool
- Connection for the DIF and CCC are HDMI type
- The Clock and trigger signals are fan-out to the DIF from an external component and not the FPGA as the LDA
  - 90ps of deterministic and 1ps rms jitter added – 60ps max skew between channels



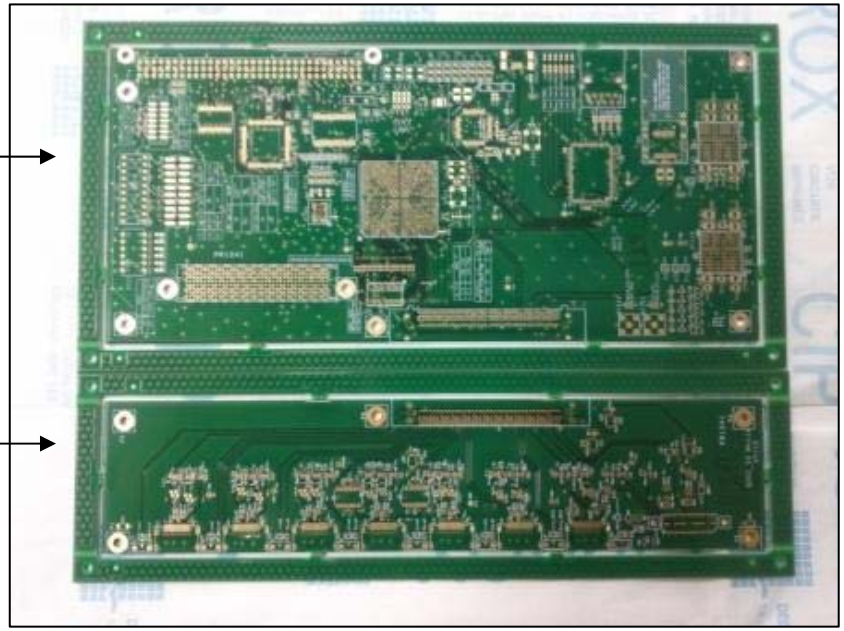
GDCC board

• 3 prototype boards have been received at the end of last year

•The PCB is shared in 2 parts : the main GDCC and the mezzanine part (HDMI connection)

Main part

Mezzanine part



GDCC

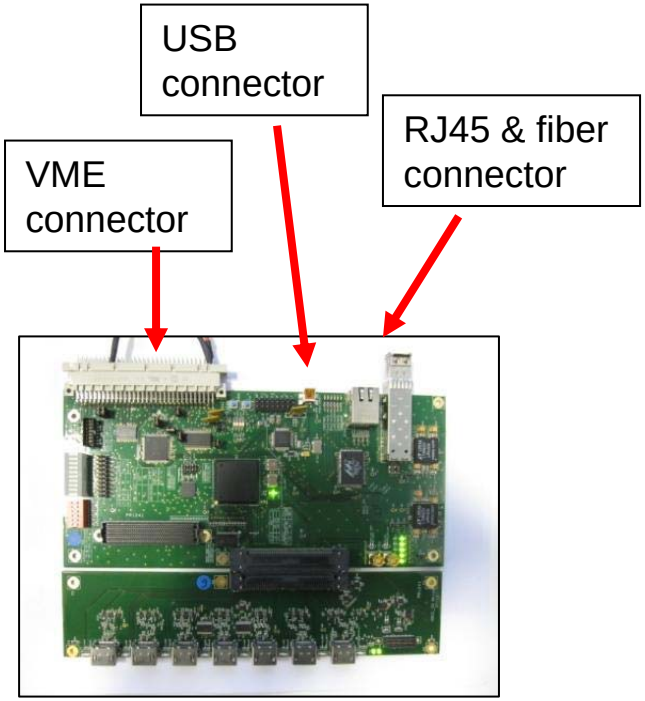
12 layers

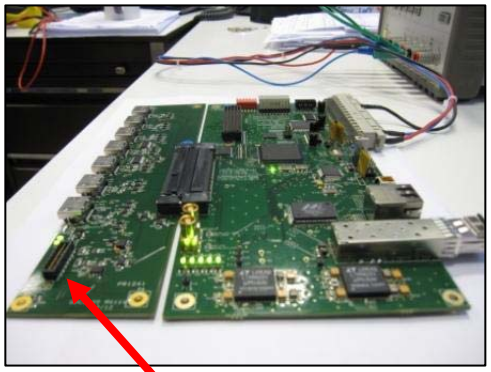
Size : 233 x 106.66 mm

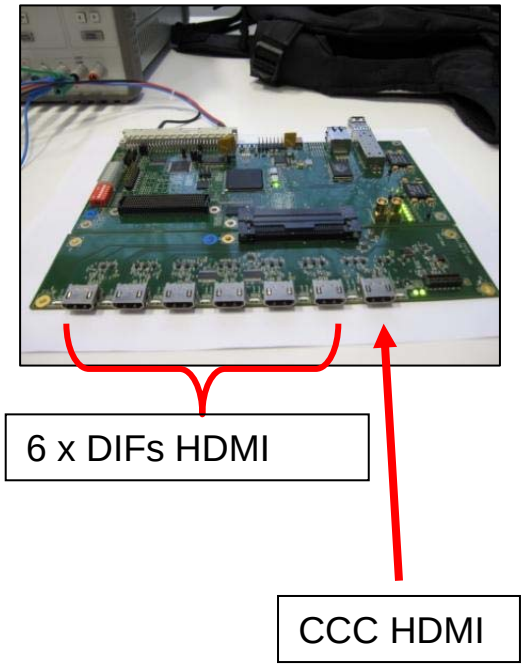
Thickness : 1.81 mm

Mezzanine
12 layers
Size : 233 x 52.8 mm
Thickness : 1.81 mm

GDCC after assembling



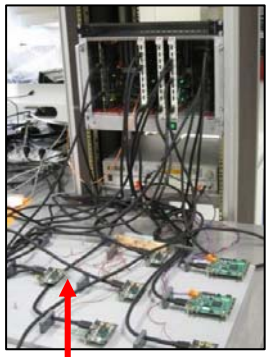


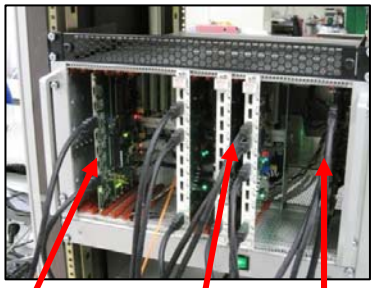


The tests (1/3)

- 2 setup of tests are used at LLR
  - Basic tests : based on Python – functional validation
  - "real" tests : based on Calicoes– GDCC connected to one slab
- Few bugs have been resolved during the basic tests
  - Mainly on PCB routing and no on firmware

Basis tests





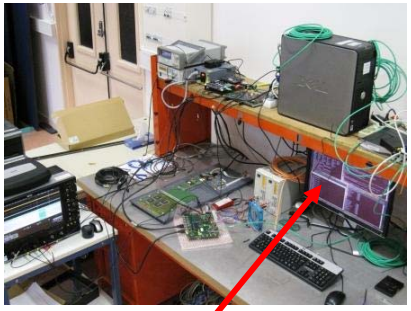
DIF

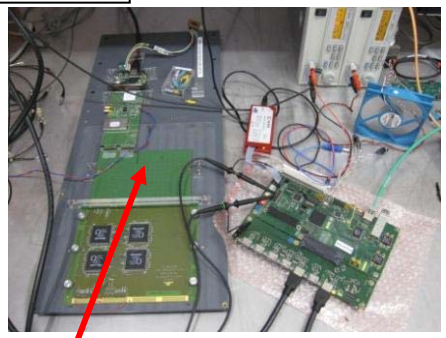
GDCC

DCC

CCC board

"Real" tests



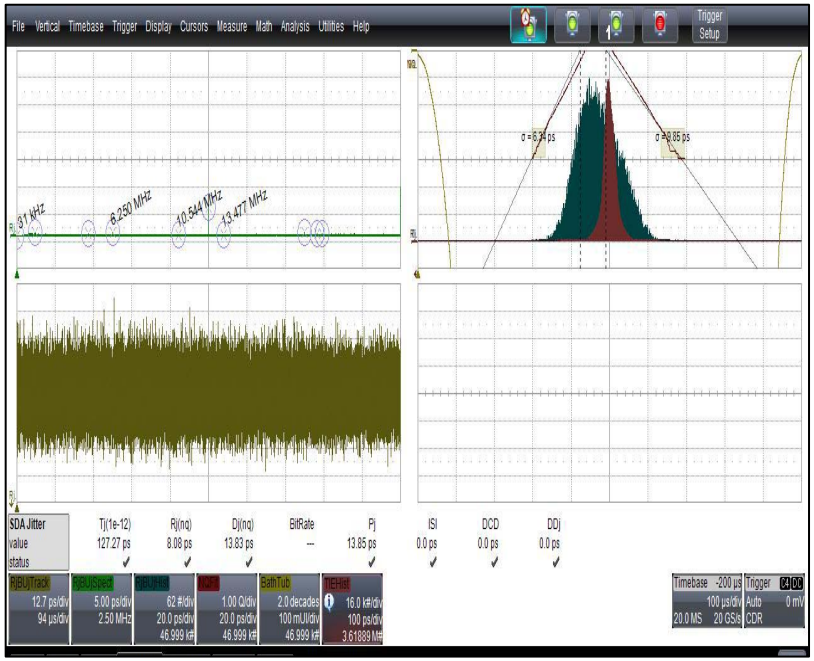


Calicoes software

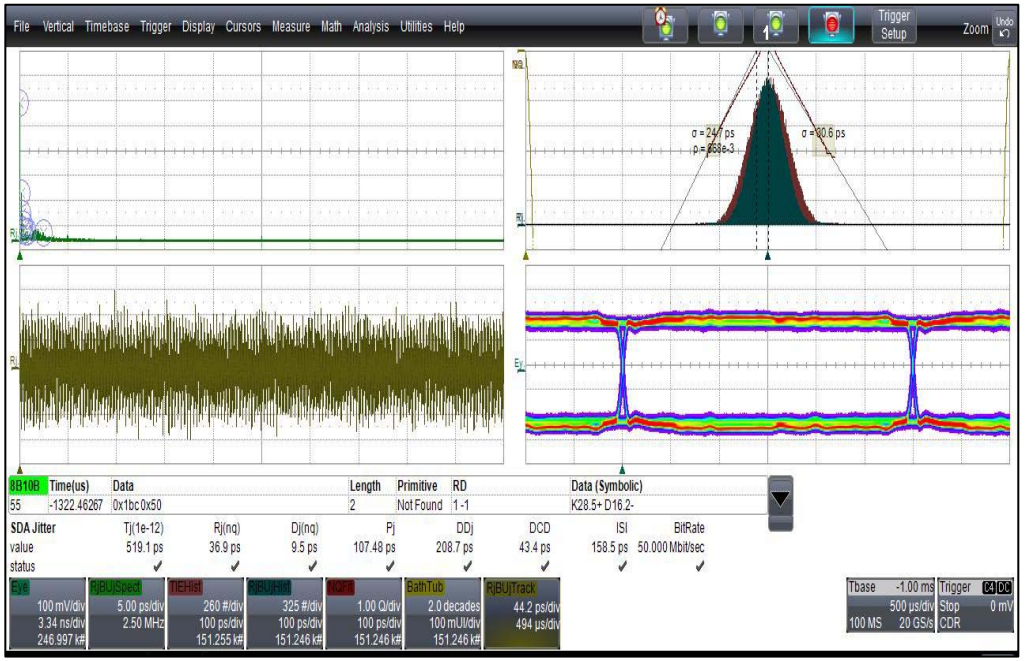
ECAL slab

The tests (2/3)

- Some results of signal integrity



Clock at the output of GDCC



Data at the input of GDCC (measure made with random gen implemented in the DIF

The test (3/3)

- Real tests
  - After several tests with a slab, we have observed a packet loss between 1 and 2 %
  - Rémi and me have put in place in our firmware some counter to identify the place of the loss. This investigation shown a loss in GEMAC block.
  - To try to understand, I changed my scenario on simulation tool and I seen the problem.
    - When a DIF packet close of the max lenght (1kB) is follow by small packet, we lose the Ethernet preamble part (0x55) and the 2 packets are merged.
  - Now, I try to implement a solution to avoid this problem.

Improvements

- During the tests, we have observed that some improvement are needs about the mechanical aspect.
  - Improvement of the HDMI connection with the cable (try to put in place a connection with a screw or a system like the ECAL chassis)
  - Improvement of the mezzanine connection (need to adjust the connection with the samtec connector)
- Improvements of the routing board
  - Minor modification to resolve the bugs
  - Minor Modification for improvement signal integrity.

Conclusion

- During the next days
  - Find a solution for the packet loss
- Make exhaustive tests
  - Add channel after channel
- Until May
  - Make the improvement of the board to launch a new fabrication
- Availbility of the new board
  - July for the tests
  - Foresee to take the decision for launch a production during the next Calice week